StretchSense™

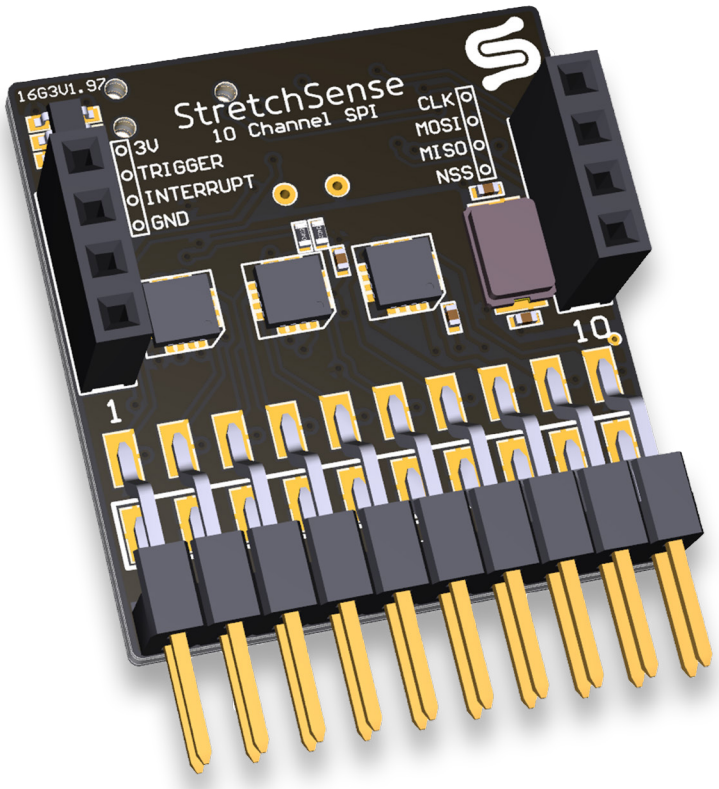
sales@stretchsense.com
support@stretchsense.com
www.stretchsense.com

NZ DDI +64 9 634 1927
US DDI +1 415 800 1003

10 Channel SPI Sensing Circuit

DATASHEET

VERSION 2.0 171016



Contents

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Terms

- Host – SPI master electronics (Designed by customer)
- StretchSense board – The 10 Channel SPI Sensing Circuit board (Designed by StretchSense)
- SSB – StretchSense board

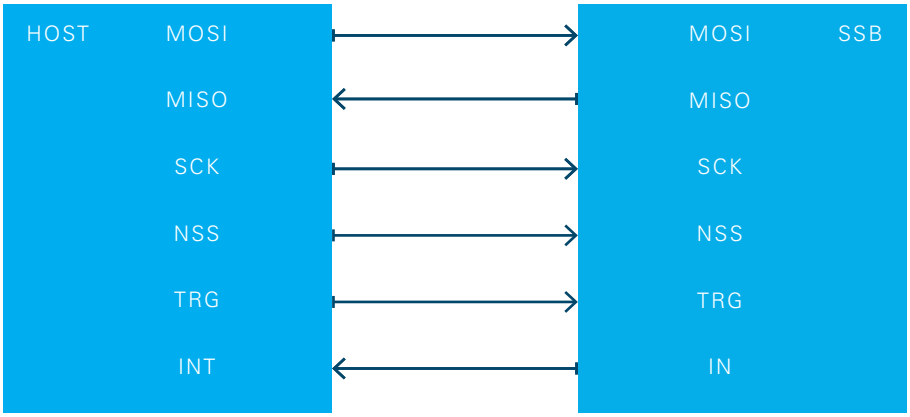
General Specifications

CHARACTERISTIC	VALUE
Name (ID)	16G3V1.97
Data Communication	SPI (Slave)
Sampling Rate per Channel Configuration	(5 ch - 1000Hz) (10 ch - 500Hz)
Sensing Channels	5 - 10
Power supply	External 3.3V supply required
*Range (max)	0 - 65535pF
*LSB Resolution (max)	0.001pF
Resolution / channel	16 bit

*These max specifications are not simultaneously available see configuration - resolution for details

SPI Communication Protocol

General



The diagram above represents the physical layer of the inter-processor communication.

This layer is implemented as a 4 wire SPI bus and a trigger line from slave device to master. The connections are Chip Select (NSS), Serial Clock (SCLK), Master Output Slave Input (MOSI), and Master Input Slave Output (MISO).

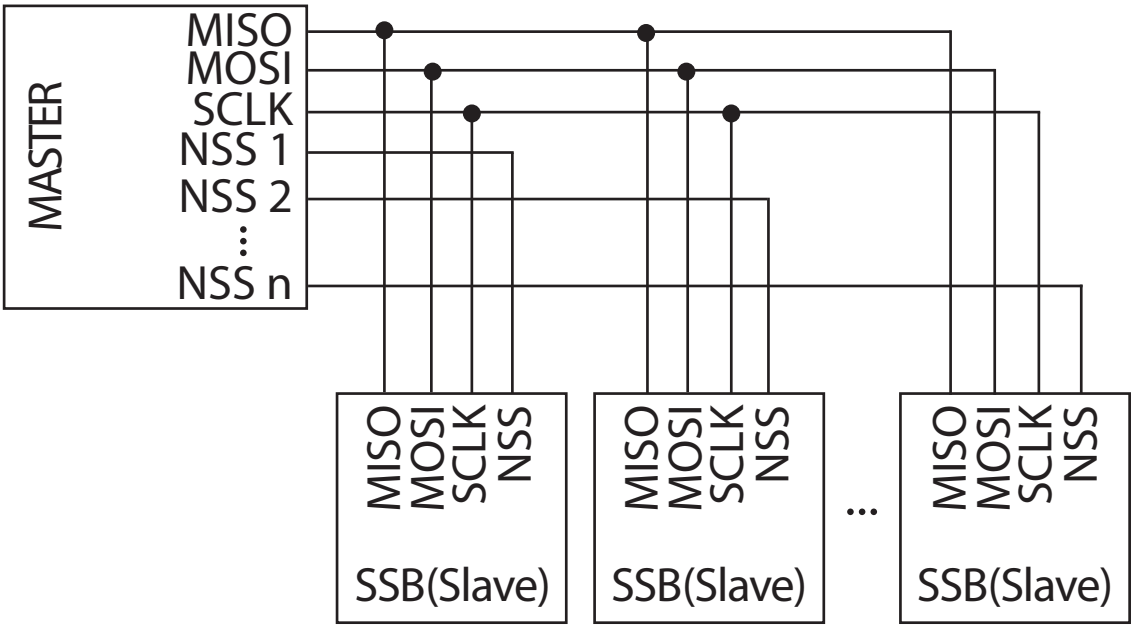
The SPI bus is configured for SCLK at a minimum clock rate of 1MHz, CPHA = 1, CPOL=0 and the word width is 8 bits. Additional TRG and INT lines are available.

Connecting Multiple SSB

The diagram above represents the physical layer of the inter-processor communication.

This layer is implemented as a 4 wire SPI bus and a trigger line from slave device to master. The connections are Chip Select (NSS), Serial Clock (SCLK), Master Output Slave Input (MOSI), and Master Input Slave Output (MISO).

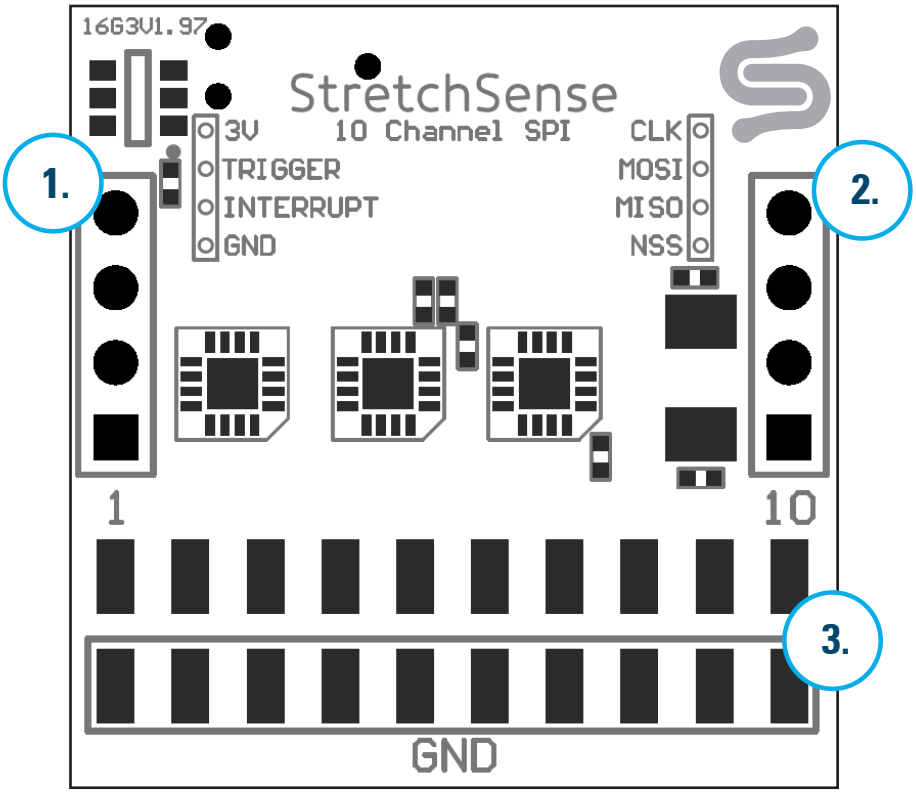
The SPI bus is configured for SCLK at a minimum clock rate of 1MHz, CPHA = 1, CPOL=0 and the word width is 8 bits. Additional TRG and INT lines are available.

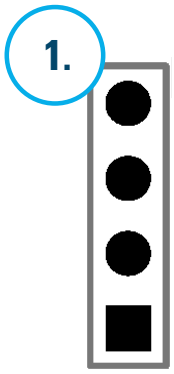


Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, MOSI, MISO, NSS)					
Input High Voltage	V_{ih}			Vdd -	V
Input Low Voltage	V_{il}	0.4			
POWER REQUIREMENTS					
Supply Voltage Range	V_{dd}		3.3		V
Supply Current	I_{dd}		20	25	mA
SPI CHARACTERISTICS (Vdd = 3V)					
Serial Clock Frequency	fclk	1		16	MHz
Clock Polarity	C_{pol}		0		
Clock Phase	C_{pal}		1		
NSS Active			LOW		
SCLK duty cycle	$DuCy_{CLK}$	50		60	%
NSS setup time	tSU_{NSS}	55.6			ns
NSS hold time	tH_{NSS}	27.8			
Data input setup time	t_{SU}	5			
Data input hold time	t_H	5			
Data output access time	ta_{SO}			41.7	
Data output valid time	t_v			37	
Data output hold time	t_h	32			
CAPACITANCE CHARACTERISTICS					
Capacitance low		0		0	pF
Capactiance high	C_{hi}	65.535		65535	
LSB Resolution		0.001		1	
$Noise_{pk\text{-}pk}$ (Filter = 1)			0.8		
Digital output resolution			16		bit
Sensing Channels	C_{ch}	5		10	
Conversion Rate (10 Channels)	C_{crate}			500	Hz
Conversion Rate (5 Channels)				1000	

Pinout on Board



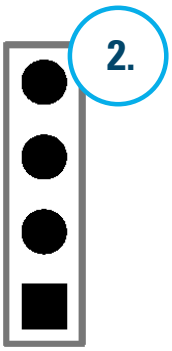


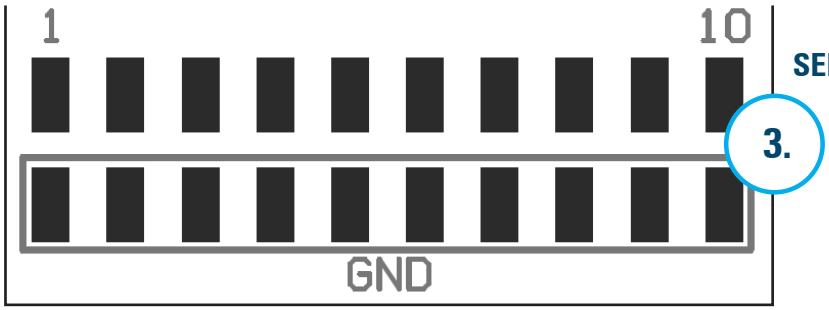
Power

I/O	ROLE
Input	3.3V
Input	Trigger
Output	Interrupt
-	Ground

SPI Bus Connection

I/O	ROLE
Input	SPI Clock
Input	SPI MOSI
Output	SPI MISO
Input	SPI Chip Select





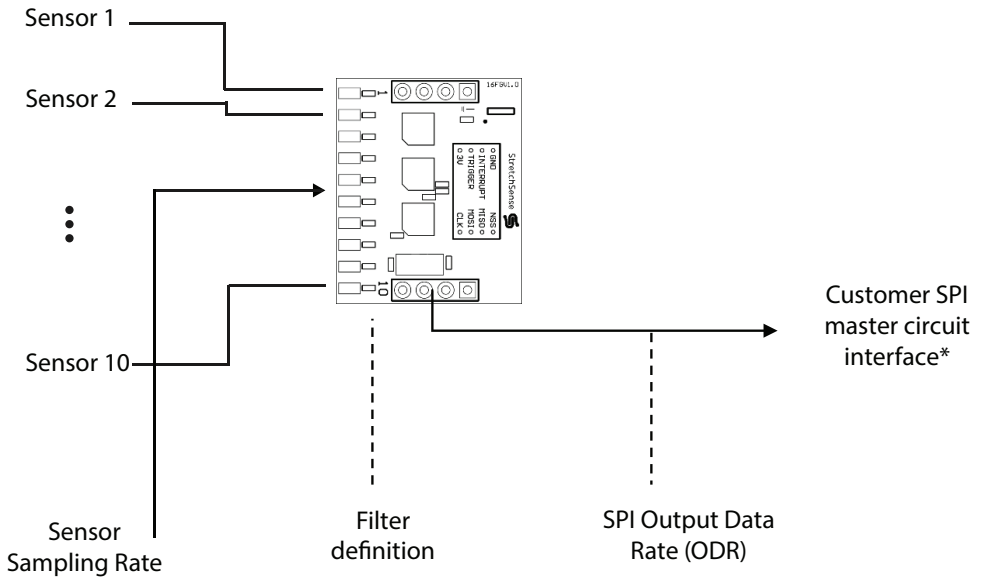
SENSOR CONNECTIONS

TOP	1	2	3	4	5	6	7	8	9	10
BOTTOM	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

*Total of 10 sensor connections, 10 signal lines are on the top side of the board (Numbers identifying 1 and 10) 10 ground/reference lines are on the bottom side of the board. Only channels 1-5 active in 1kHz mode.

Managing Data on the 10 Channel Circuit

A number of configuration options are available over the 10 Channel Sensing Circuit's SPI bus. The circuit samples 10 channels or 5 channels at higher speeds and is capable of outputting values continuously or via an external trigger over its SPI interface. In addition, the user can define a number of parameters on the board to trade off data rates and Signal-to-noise ratios. Configuration occurs via a user defined configuration message over SPI covered in the "Message Protocol" section.



Definition	The rate at which each sensor's capacitance is measured	The moving point filter will reduce the frequency of new data packets available to send over SPI in exchange for cleaner data (higher SNR)	The rate at which the last available data packet is sent over SPI
User configurable options	1) 500Hz/channel for 10 channels 2) 1000Hz/channel for 5 channels	Filter size A user defined 1-255 point moving filter.	1) Continuous (automated) or externally triggered sensor polling 2) 0 to 1000Hz ** in continuous mode operation.

* note that StretchSense also provides a battery operated plug in SPI-to-Bluetooth® low energy interface for mobile demo purposes with the majority of 10 channel circuits shipped.
**In order to operate the circuit at 1000Hz sampling rate, channels 6-10 will be disabled. This is required due to the need to reduce processing time to meet these higher data rates.

Message Protocol

The message protocol consists of 22-byte fixed length messages, with 1-byte header that identifies the message type.

Byte	0	1..21
Field	Header	Payload

Currently only two messages are defined as

HEADER	MESSAGE TYPE
0x00	Data
0x01	Config

Configuration Message

The host can configure the StretchSense board using the Configuration message, which is described below.

Byte	0	1	2	3	4	5	6-21
Field	CONFIG	ODR	INT	TRG	Filter	RES	0

ODR — Output Data Rate

Default: 0 = OFF

ODR, is the Output Data Rate of the StretchSense board. This is same as the sampling rate of all the five sensors. The default ODR is 0Hz (Off) upon power-up, the StretchSense board is not sampling the sensors. Currently the following sampling/output rates are supported:

INPUT	ODR (HZ)
00	OFF
01	25
02	50
03	100
04	167
05	200
06	250
07	500
08*	1000

*In order to operate the circuit at 1000Hz sampling rate, channels 6-10 will be disabled. This is required due to the need to reduce processing time to meet these higher data rates.

INT — Interrupt Enable

Default: 0 = OFF

INPUT	MODE
0	Disabled
1	Enabled

Enable or disable the Interrupt output.

This Output pin can be used to notify external circuitry of events. (See Interrupt Mode)

TRG — Externally Triggered Sampling

Default: 0 = Continuous Sampling

INPUT	MODE
0	Continuous Sampling
1	Triggered Sampling

In continuous sampling mode, the host will periodically poll the StretchSense board, and the latest set of sampled values are returned to the host over SPI using the data message.

In external trigger mode, the StretchSense circuit will wait until it receives a rising edge trigger on the TRIGGER input. This will trigger the start of a sampling cycle on the StretchSense circuit. This sampling window will take approximately 2-3ms to complete, at which stage the new sensor values are loaded into the Buffer ready for a read from the host.

Filter

Default: 1 = 1pt filter

INPUT	FUNCTION
1-255	Filter length

Where the Filter value is used to specify the length of a moving average filter. This ranges from a single point (no filter) up to 255 point filter.

RES — LSB Resolution

Default: 1 = 0.1pF

INPUT	LSB RESOLUTION	RANGE (16bit)
0	9.5F	0 - 65535pF
1	0.1pF	0 – 6553.5pF
2	0.01pF	0 – 655.35pF
3	0.001pF	0 – 65.535pF

The capacitance output of the circuit is a 16 bit value where the LSB is adjustable between 0.001pF – 1pF. This allows the user to define the most appropriate resolution for the expected capacitance range.

Data Message

After the host configures the StretchSense board, the StretchSense board starts sampling the sensors and sends the data message over the SPI bus to the host in the following format.

Byte	0	1	2	3	4	5	6	7	8	9	10	11
Field	Data	SQN	S1-H	S1-L	S2-H	S2-L	S3-H	S3-L	S4-H	S4-L	S5-H	S5-L
Byte	12	13	14	15	16	17	18	19	20	21		
Field	S6-H	S6-L	S7-H	S7-L	S8-H	S8-L	S9-H	S9-L	S10-H	S10-L		

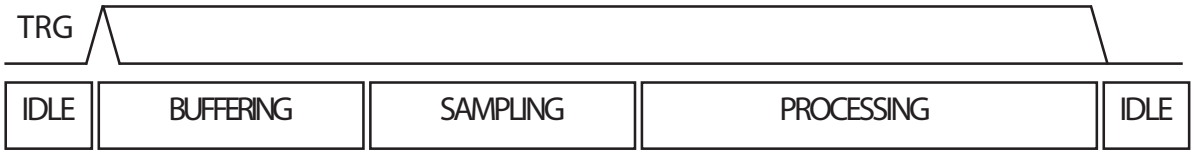
Where SQN is the Sequence number of the data message. SQN is a number in the range 0 and 255. It is incremented every time a new set of samples are available and ready to be read by the host.

Where S1-H and S1-L specify the High and Low byte for 16-bit 1 sensor value. Bytes 4 to 21 specify similar format for the remaining 9 sensors.

Trigger Mode

When the circuit is configured in trigger mode the start of a sampling event can be externally triggered by a rising edge signal on the TGR input line. This allows for the synchronising of sensing events to external devices.

The diagram below provides a representative view of this process.



The SSB is in an idle state waiting for the TRG input. When the trigger line rises high the circuit enters a buffering state, at this stage the trigger input is disabled. Once buffered, there is a sampling window where capacitance data is captured. The end of the sampling window the trigger line is re-enabled. The capacitance data captured goes through data processing at the end of which the new data packet is ready to be read from the circuit.

Timing Characteristics

NAME	SYMBOL	TYPICAL	UNITS
Buffering Time	$t_{buffering}$	1.00	ms
Sampling Time	$t_{sampling}$	1.00	
Processing Time	$t_{processing}$	1.91*	

*10channel mode processing

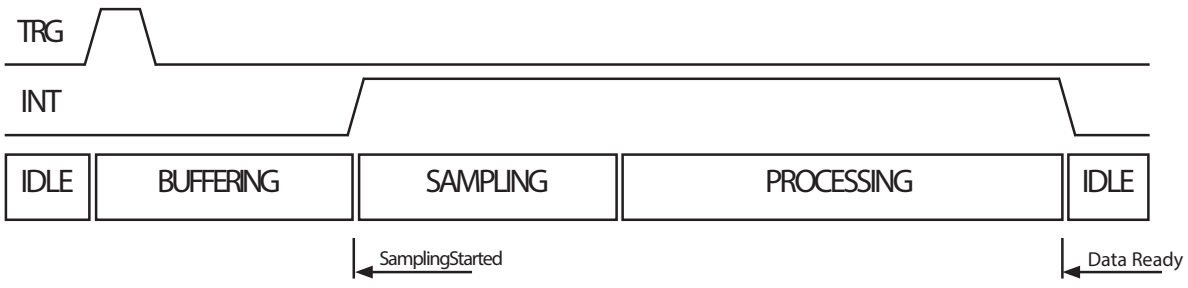
Trigger available (After previous edge) = $t_{buffering} + t_{sampling}$

Data Ready (After previous edge) = $t_{buffering} + t_{sampling} + t_{processing}$

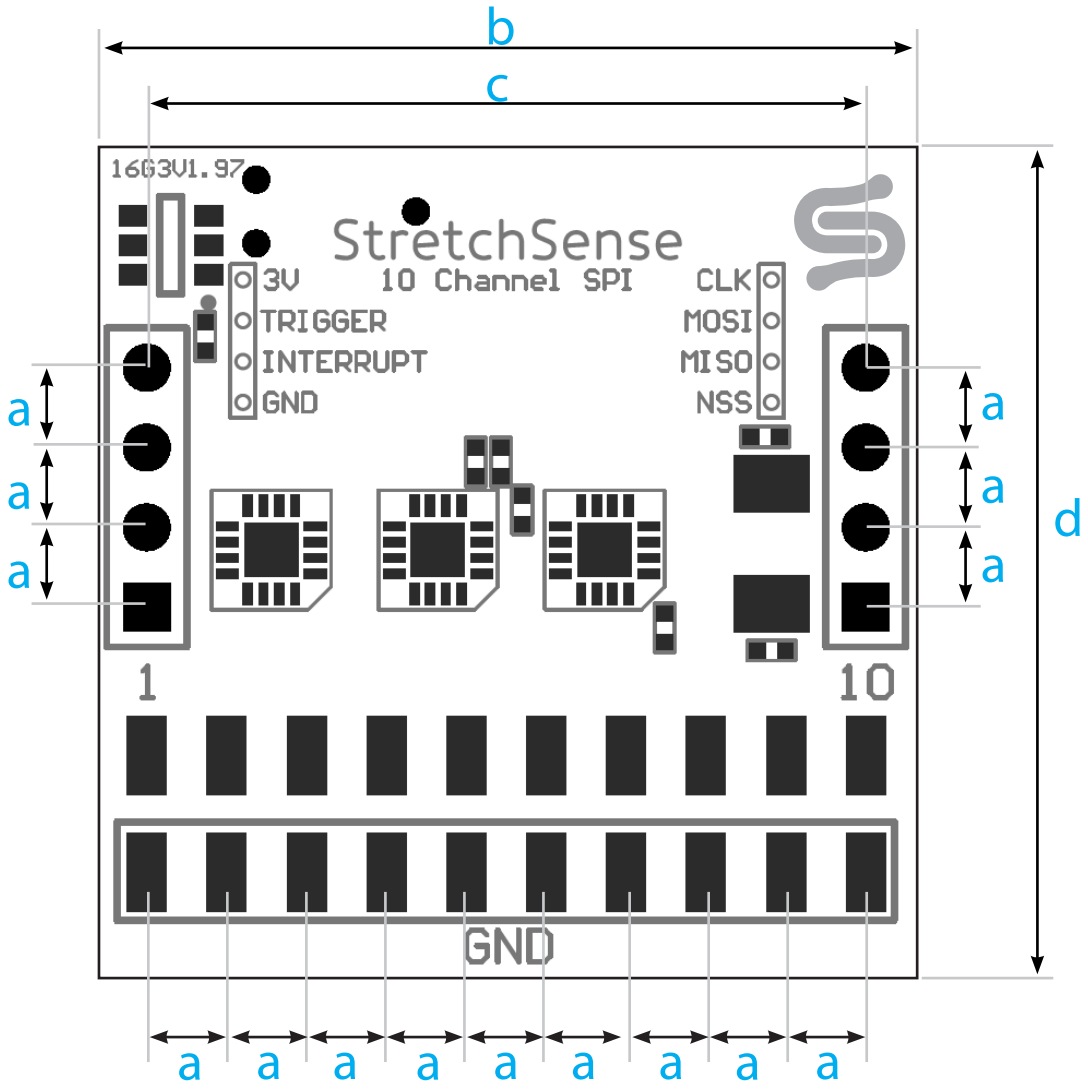
Interrupt Mode

When the circuit is configured in interrupt mode the INT output line will toggle to indicate two events. The start of a sampling period is indicated by a rising edge on the INT line and the availability of new data packets is indicated by a falling edge.

The diagram below provides a representative view of this process. (Diagram demonstates system in triggered mode)



Circuit Dimensions



DIMENSIONS		
a	2.54mm	0.100”
b	26.28	1.035”
c	22.86mm	0.900”
d	29mm	0.854”
Board thickness	1.6mm	0.630”

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