Lab #4: Basic Computer Organization

CEG 2136 – Computer Architecture

Fall 2022

School of Electrical Engineering and Computer Science

University of Ottawa

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Experiment Date: November 9, 2022

Submission Date: December 7, 2022

Objective:

- The point of this lab is to analyze the structure of a basic computer, we will devis design, implement, simulate and test the control unit on Altera platform. The design should function in simulation and on the board if everything is well done.

Equipment and Components

- Quartus II
- Altera DE2-115 board with USB-Blaster cable and Power supply 12 VDC, 2A

Theory

The first part of the lab was analyzing the design of the basic computer that was given to us. To properly understand the lab, we had to complete the prelab questions. The prelab questions tested our knowledge of the basic background information of the basic computer. The second part tested our ability to formulate equations using tables of values.

Design

- **Presentation of Design:**

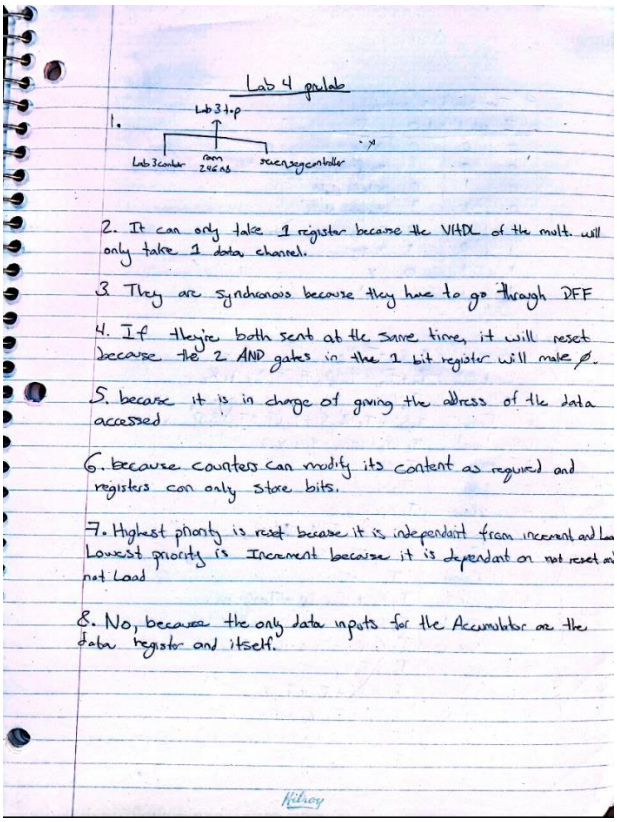
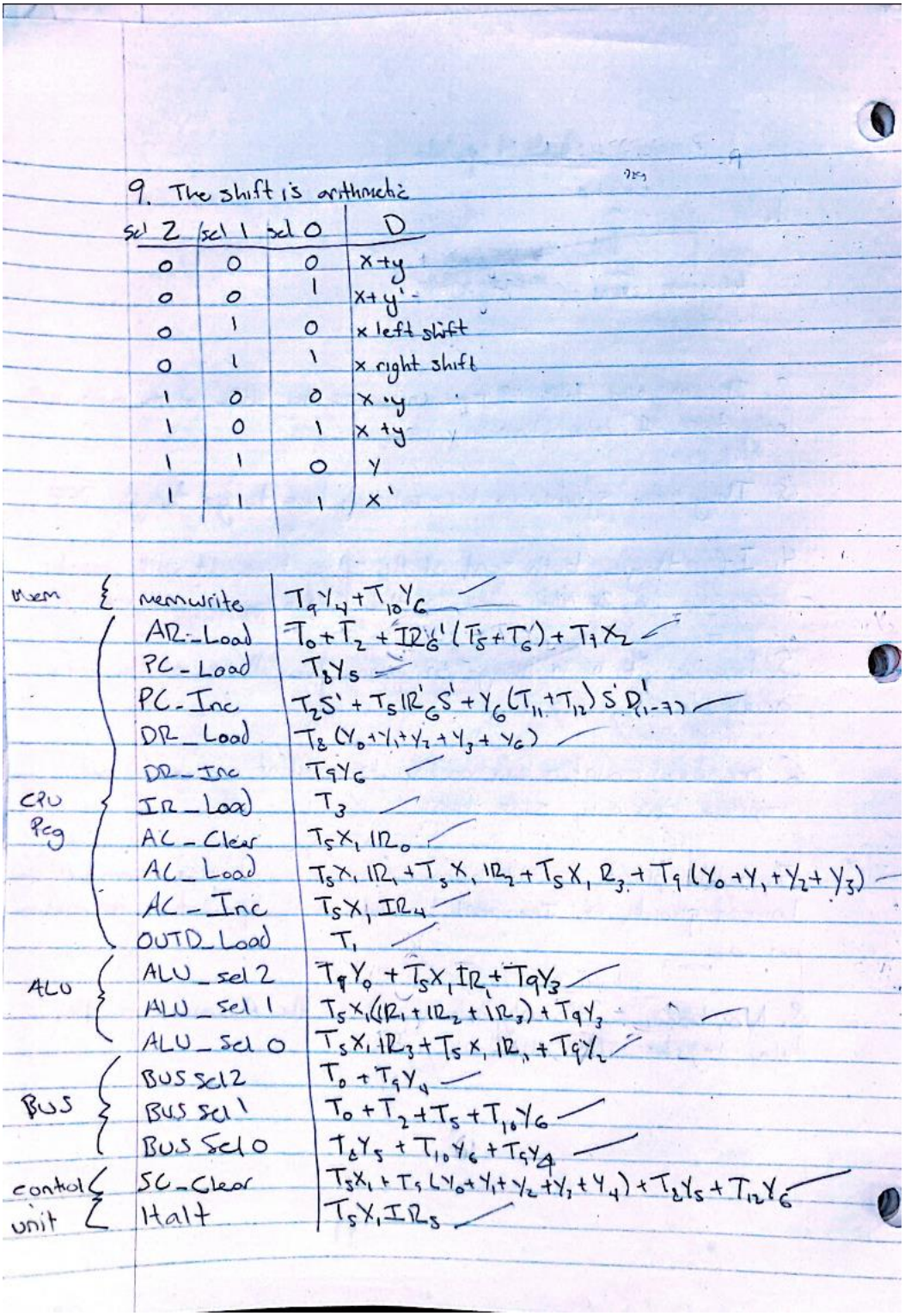


Figure 1: Pre-Lab for the Hardware Section

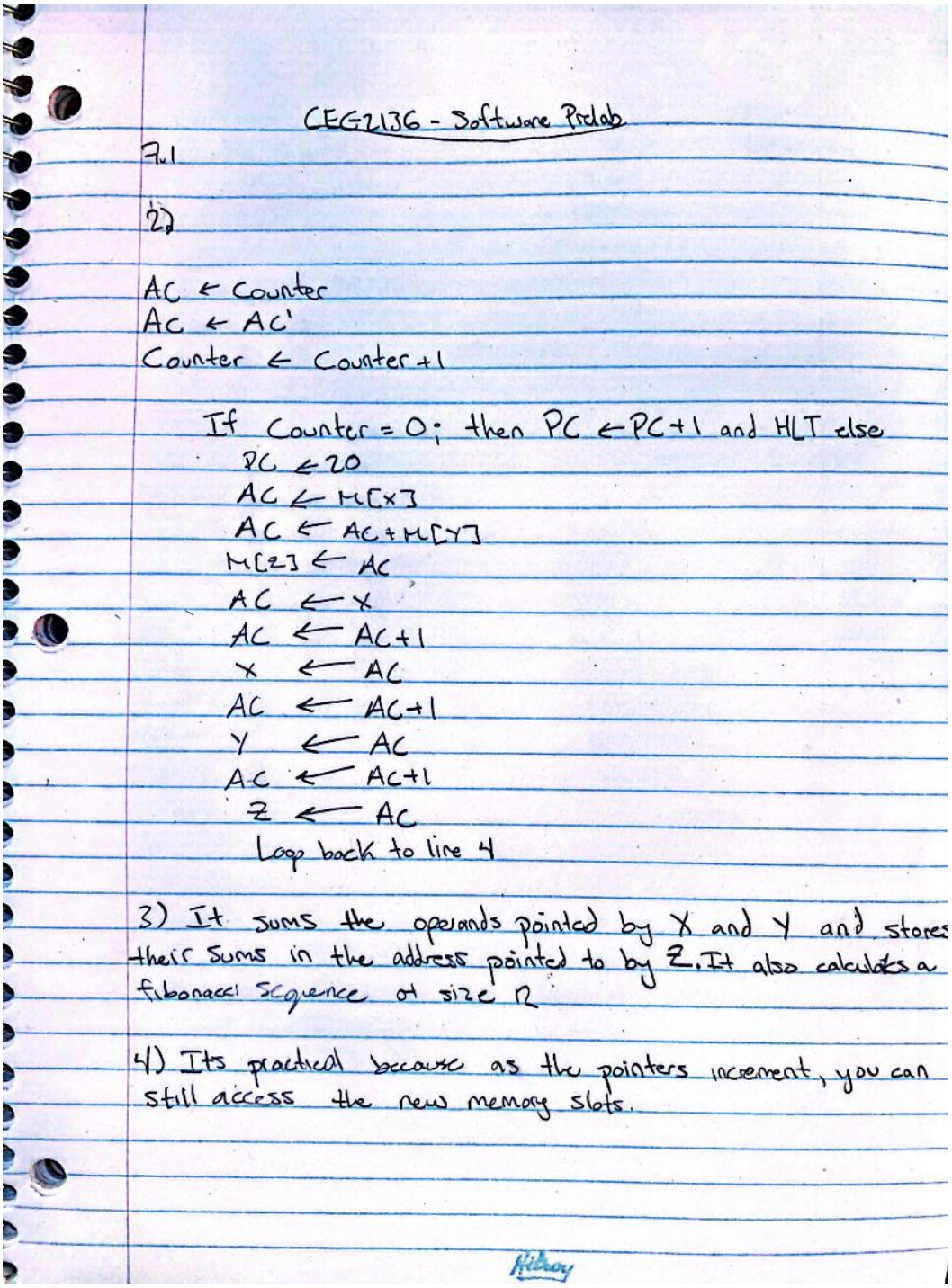


9. The shift is arithmetic

sel 2	sel 1	sel 0	D
0	0	0	x+y
0	0	1	x+y'
0	1	0	x left shift
0	1	1	x right shift
1	0	0	x·y
1	0	1	x+y
1	1	0	y
1	1	1	x'

Mem	memwrite	$T_4Y_4 + T_{10}Y_6$
	AR_Load	$T_0 + T_2 + IR_6'(T_5 + T_6') + T_1X_2$
	PC_Load	T_8Y_5
	PC_Inc	$T_2S' + T_5IR_6'S' + Y_6(T_{11}+T_{12})S'D_{(1-7)}'$
	DR_Load	$T_8(Y_0+Y_1+Y_2+Y_3+Y_6)$
	DR_Inc	T_4Y_6
CPU Reg	IR_Load	T_3
	AC_Clear	$T_5X_1IR_0$
	AC_Load	$T_5X_1IR_1 + T_5X_1IR_2 + T_5X_1R_3 + T_4(Y_0+Y_1+Y_2+Y_3)$
	AC_Inc	$T_5X_1IR_4$
	OUTD_Load	T_1
ALU	ALU_sel 2	$T_4Y_0 + T_5X_1IR_1 + T_4Y_3$
	ALU_sel 1	$T_5X_1(IR_1+IR_2+IR_3) + T_4Y_3$
	ALU_sel 0	$T_5X_1IR_3 + T_5X_1IR_1 + T_4Y_2$
BUS	BUS sel2	$T_0 + T_4Y_4$
	BUS sel1	$T_0 + T_2 + T_5 + T_{10}Y_6$
	BUS sel0	$T_8Y_5 + T_{10}Y_6 + T_4Y_4$
control unit	SC_Clear	$T_5X_1 + T_5(Y_0+Y_1+Y_2+Y_3+Y_4) + T_8Y_5 + T_{12}Y_6$
	Halt	$T_5X_1IR_5$

Figure 2: Pre-Lab for the Hardware Section (Equations)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7.1

2)

AC ← Counter
AC ← AC'
Counter ← Counter+1

If Counter = 0; then PC ← PC+1 and HLT else
PC ← 20
AC ← M[X]
AC ← AC+M[Y]
M[Z] ← AC
AC ← X
AC ← AC+1
X ← AC
AC ← AC+1
Y ← AC
AC ← AC+1
Z ← AC
Loop back to line 4

3) It sums the operands pointed by X and Y and stores their sums in the address pointed to by Z. It also calculates a fibonacci sequence of size N

4) Its practical because as the pointers increment, you can still access the new memory slots.

Kilroy

Figure 3: Pre-Lab for the Software Section

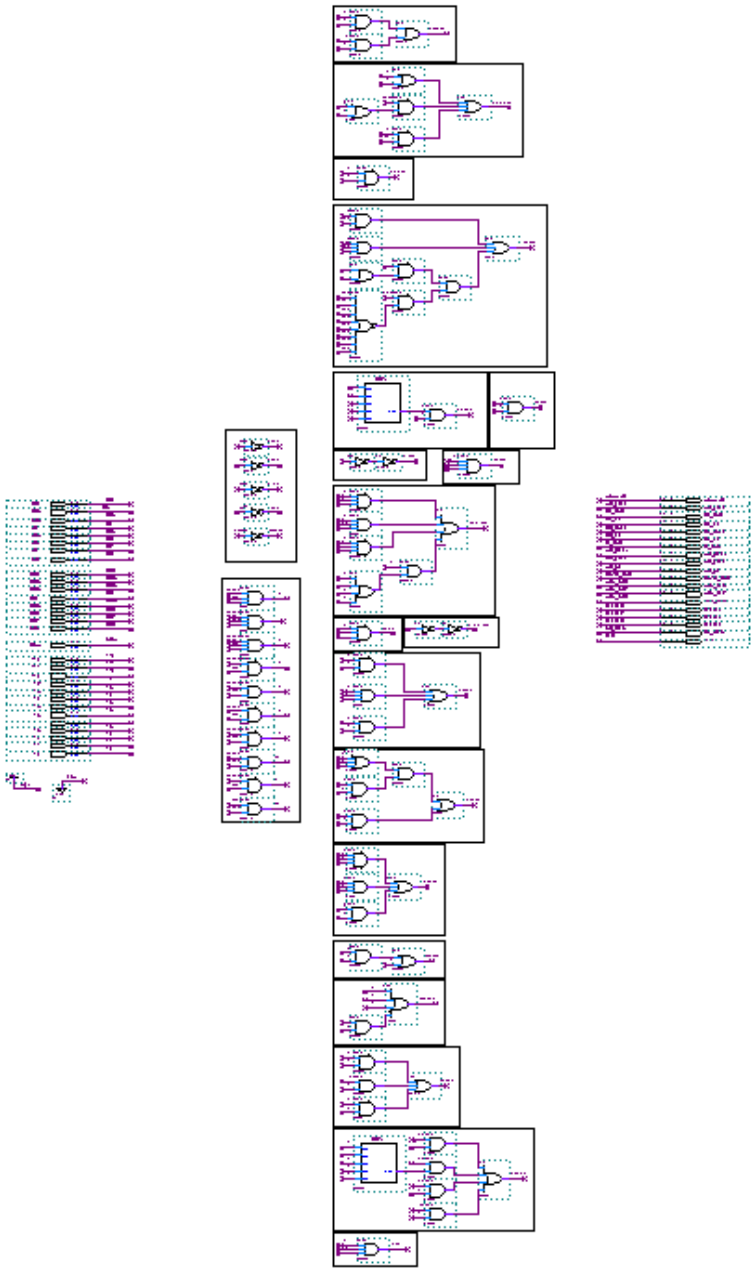

Figure 4: Logic Diagram for the Lab3controller constructed on Quartus

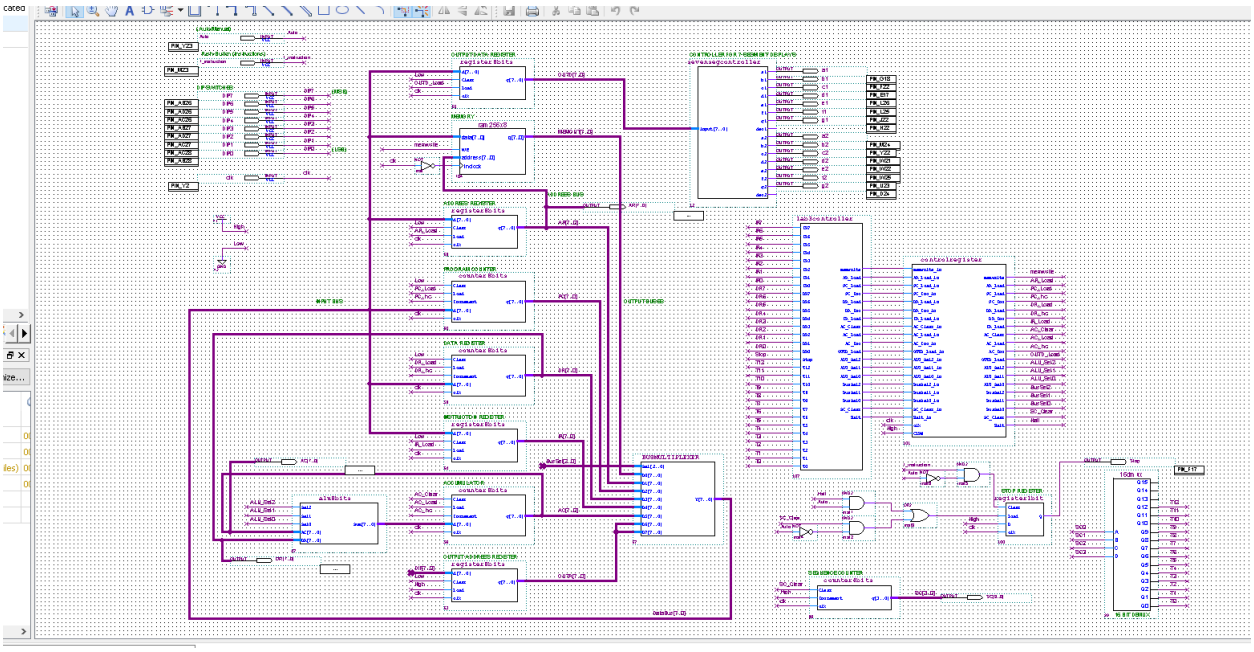

Figure 5: Logic Diagram for the Lab3top constructed on Quartus

- **Discussion of used components:** In order to understand how to construct the lab3controller circuit, we had to complete the pre-lab work for hardware. Utilizing the given table of values attached to our lab instructions, we were able to formulate the required equations to create their corresponding circuits (see fig. 4). We then constructed the whole circuit and assigned the pins with their respective input and output values After compilation and simulation of our waveform diagrams (see fig. 7), we utilized the Altera DE2-115 board to analyze our results and compare them to the expected results.

- **Discussion of actual solution:** Upon implementation of the lab3top circuit, we utilized various gates and multiplexers in our designs. We learned how to wirelessly connect input and output values which made construction a lot simpler and more efficient. We utilized box outliners to organize all our designs efficiently. We constructed them in order as listed from top to bottom. We started with all the x and y values and utilized them to construct the actual circuits. Our design proved to be successful after compilation and further simulation analysis.

- **Discussion of challenging problems:** During implementation and simulation we did not encounter any serious issues but rather just naming issues. Our compilation was successful, and we were able to successfully assign all the required input and output values their pin assignments. We also did not encounter any problems with our mif file. Our issues appeared in our waveform simulation diagram and prevented us from progressing any further in our laboratory experiment.

Simulation and Verification of Real Implementation

- **Simulation and Synthesis results:**

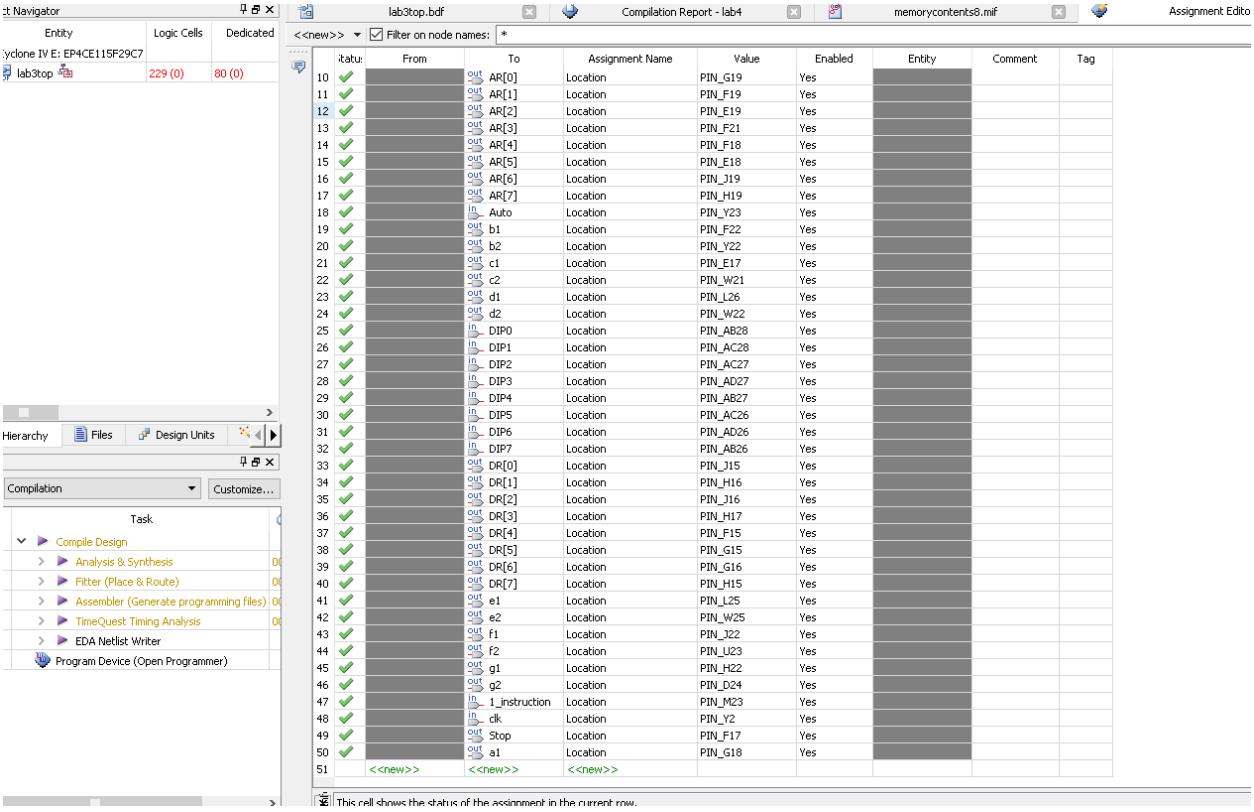

Figure 6: Pin Assignment of the circuit constructed on Quartus

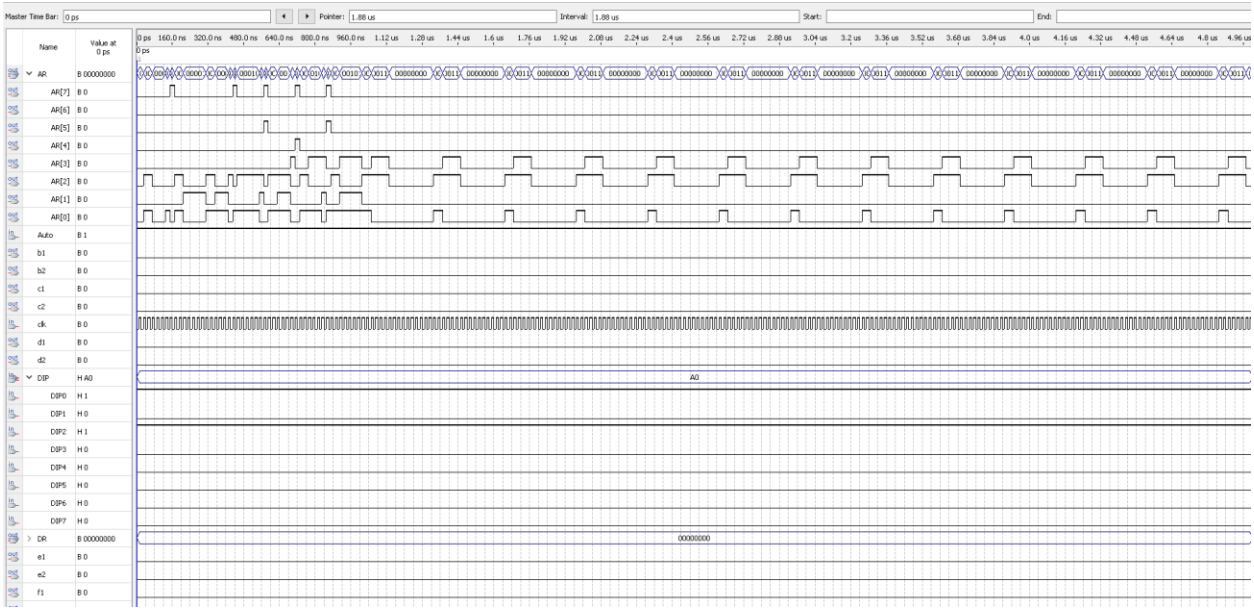

Figure 7: Waveform simulation of the circuit constructed on Quartus

- **Experimental Verification of Circuit Operation:** After successfully simulating our Quartus design, we successfully completed our pin assignment and mif file creation. Our lab could not progress any further as our waveform diagram was not displaying accurate results and we could not find the root of the issue. We inspected all of the values in our design (circuit diagram and mif file) and we were not able to find any mistakes. We refreshed our program, and we still received the same results. We were not able to continue any further in our experiment.

Discussion and Conclusions

We encountered a couple of very miniscule issues and one major issue that prevented us from progressing any further in our lab experiment. We were able to successfully create our circuit design for the hardware portion. This was verified by the successful compilation and TA verification of our equations which we used to construct the circuits. Our pin assignments and mif file were also correct. Our waveform diagram however, would not show the correct values when compiled and simulated. We followed the instructions in the lab manual with the respective end times and time periods. We grouped the required values and assigned their values, but we were not able to acquire the intended results of this experiment. We inspected all the values of the mif file, and circuit construction but found no errors in our implementation. That was the furthest we were able to advance in this experiment.

In this lab experiment we also learned various new things and techniques on the Quartus platform such as being able to wirelessly connect input and output values. This technique helped us organize our circuits as efficiently as possible. The box outliner helped to achieve that as well. We also learned how to utilize a mif file and construct a proper one. In the prelab we also practiced and mastered the ability to formulate proper equations using Boolean algebra laws.

General Conclusion:

Over the course of the 4 lab sessions, we learned various efficient new techniques when utilizing the Quartus II platform. We were able to successfully complete most of the tasks in this laboratory experiment including construction and compilation of our designs. We did however encounter an unsolvable problem with regards to our waveform simulation that halted any further progression in our experiment for this lab.