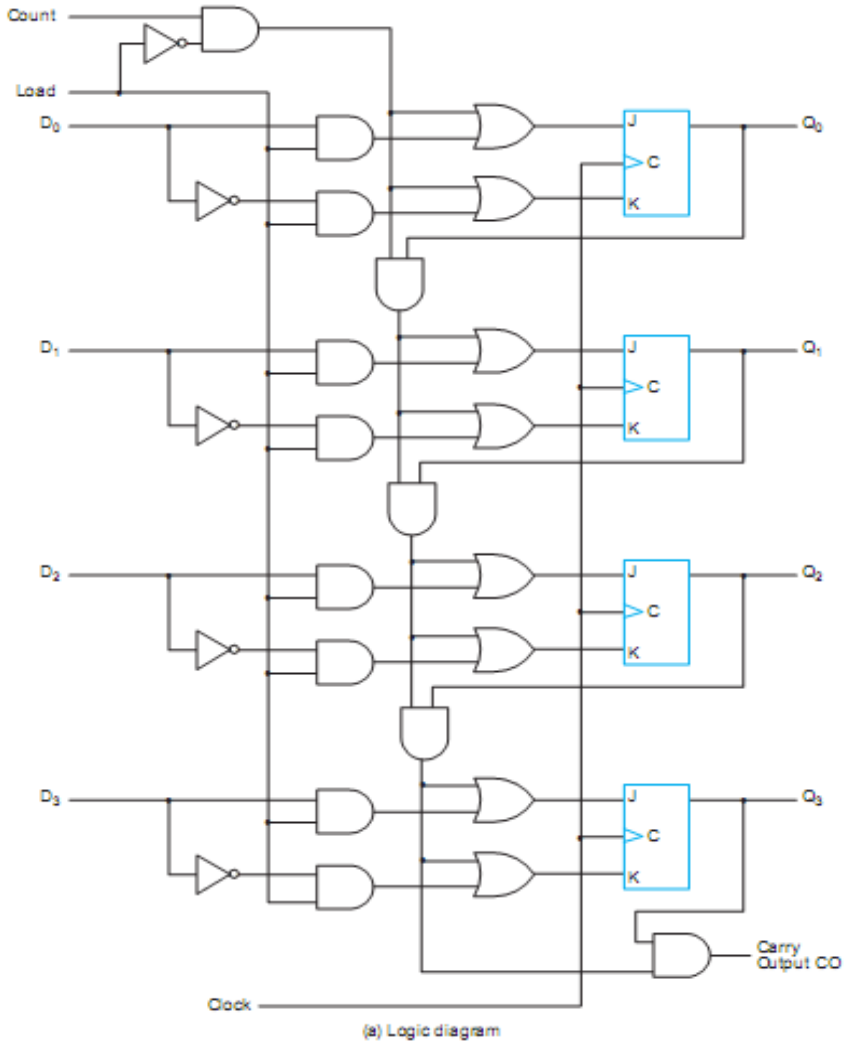
CME 2206 Computer Architecture

Lab 1

4-Bit Binary Counter with Parallel Load

Experiment 1

Design a 4 bit Binary Counter with parallel load in Quartus II by using J-K flip flops and necessary logic gates as shown in the figure below.



(a) Logic diagram

Experiment 2

Design a ***4 bit Binary Counter with parallel load*** in Quartus II by using ***lpm_counter.***