



# Cyclone V Signaling Sys.

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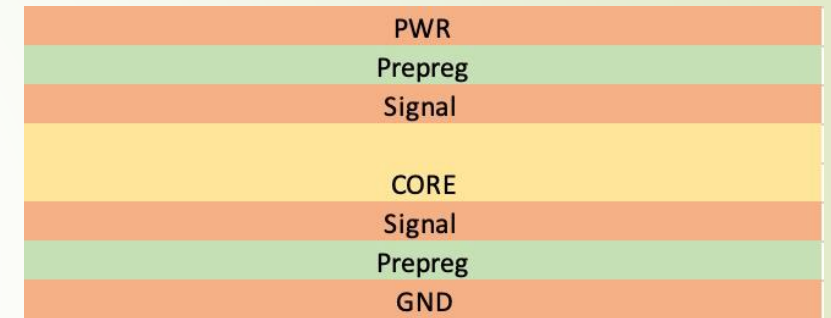


# Cyclone V Chip (5CGXFC5C6F23C6N)

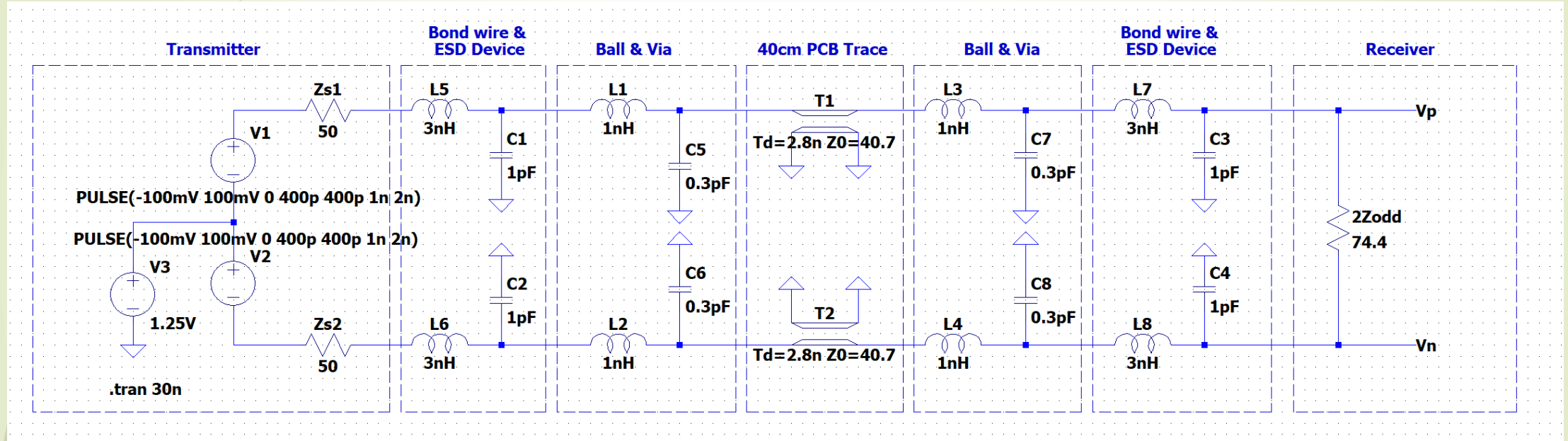
- Bipolar differential signaling system (LVDS)
- Receiver voltage: 1.0V to 1.6V ( > 700Mbps), 0V to 1.85V ( < 700Mbps)
- Common mode voltage: 1.25V
- 484 Pin FBGA Package
  - Top RX, TX pins: 28
  - Right RX, TX pins: 8
  - Bottom RX, TX pins: 24
- Ball Diameter: 0.34mm
- Ball Pitch: 0.80mm

# Board Stack-up and Parameters

- Layer stack-up: 4 layers
- Width: 3.5mil (0.09mm)
- Spacing (per line): 3.5mil (0.09mm)
- Spacing (per pair): 20.5mil (0.52mm)
- Material: FR-4, Copper Core
- 7628 Prepreg (Dielectric constant = 4.4)
- PCB Thickness = 78.7mil (2mm)
- 35 differential signals on layer 1 and 35 differential signals on layer 2



# Overall Design



# Noise Budget

|                           | K     | mV                     |
|---------------------------|-------|------------------------|
| Signal Swing (dp-dn)      |       | 400                    |
| Gross Margin              |       | 200                    |
| Crosstalk                 | 0.045 | 18                     |
| Reflections               | 0.045 | 18                     |
| Kn                        | 0.215 | 86                     |
| Receiver offset           |       | 40                     |
| Gaussian Noise (Vrms)     |       | 5                      |
| Net Margin                |       | 38                     |
| V <sub>SNR</sub>          |       | 7.6                    |
| Bit Error Rate            |       | $2.86 \times 10^{-13}$ |
| Mean Time Between Failure |       | 0.222 yrs              |

# Timing System and Budget

- Closed-loop timing system
- Removes skew, still take jitter into consideration

| Timing Parameter | Time  |
|------------------|-------|
| Skew             | 0s    |
| Rise time        | 400ps |
| Aperture         | 20ps  |
| Cycle time       | 2ns   |
| Delay            | 1ns   |
| Uncertainty      |       |

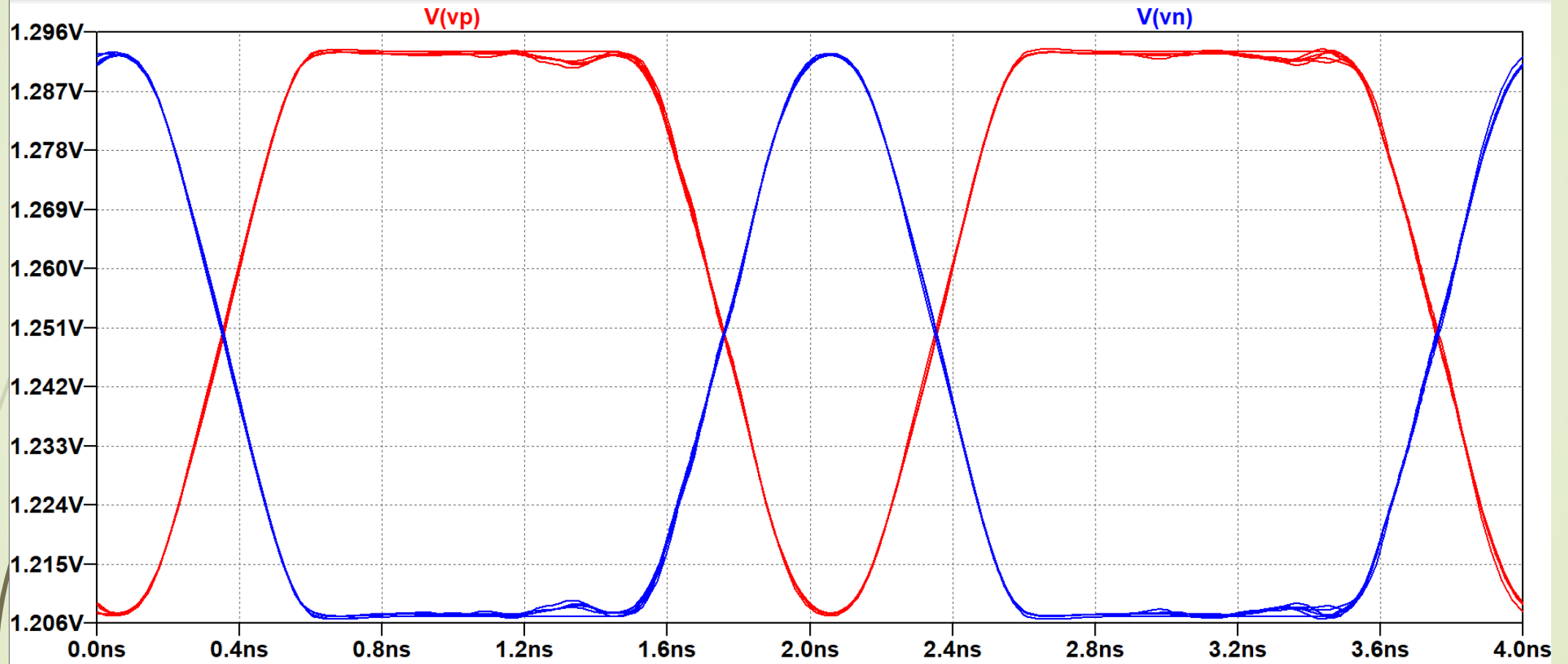
$$T_{bit} > t_a + t_r + t_u = 420ps$$

# Calculated Parameters

|   | Value                | Equation   |
|---|----------------------|--|
| Stray Capacitance ( $C_c$ )                   | 172pF/m              | $C = \frac{we}{d} + \left( \frac{2\pi e}{\ln\left(\frac{s}{h}\right)} \right)$ |
| Coupling Capacitance ( $C_d$ )                | 15pF/m               | $C = \frac{8.554pF/m\epsilon_r A}{d}$  |
| Inductance of Line (L)                        | 285nH/m              | $L = \frac{\epsilon\mu}{C}$  |
| Mutual Inductance (M)                         | 25.83nH/m            | $\frac{C_d}{C} = \frac{M}{L}$  |
| Characteristic Impedance ( $Z_0$ )            | 40.7 $\Omega$        | $Z_0 = \sqrt{\frac{L}{C}}$   |
| Resistance of Line (R)                        | 1.25 $\Omega$ /m     | $R = \frac{\rho L}{A}$   |
| $Z_{odd}$                                     | 37.18 $\Omega$       | $Z_{odd} = \sqrt{\frac{M-L}{C_d+C}}$   |
| Velocity (v)                                  | 1.4x10 <sup>-8</sup> | $v = \frac{1}{\sqrt{LC}}$  |
| Transmission Line Delay (t)                   | 2.8ns                | $t = \frac{d}{v}$  |
| Inductive Crosstalk Coefficient ( $k_{lx}$ )  | 0.09                 | $\frac{M}{L}$  |
| Capacitive Crosstalk Coefficient ( $k_{cx}$ ) | 0.09                 | $\frac{C_d}{C}$  |
| Near end Cross Talk ( $k_{rx}$ )              | 0.045                | $k_{rx} = \frac{kcx - klx}{4}$   |
| Far-end Cross Talk ( $k_{fx}$ )               | 0                    | $k_{rx} = \frac{kcx - klx}{3}$   |



# Performance Results

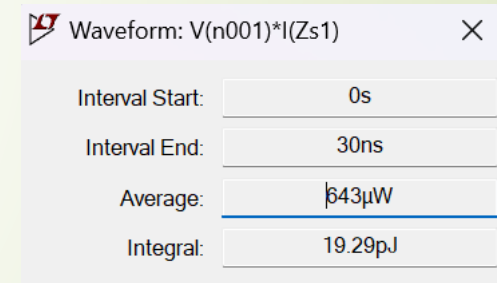
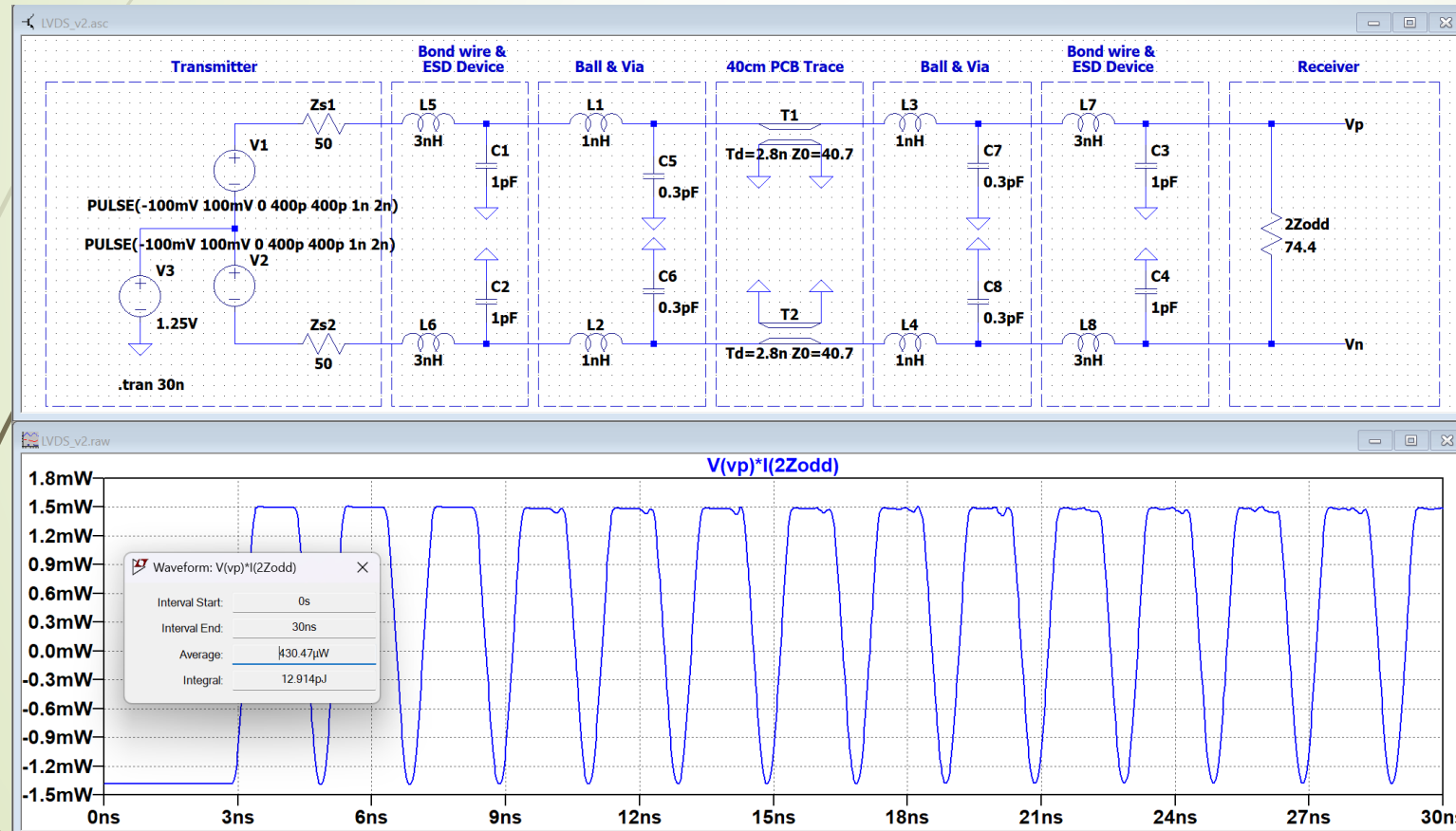


Aperture time = 1.5ns – 0.6ns = 900ps



# Power & Cost

- Cyclone V 5CGXFC5C6F23C6N: \$244.00
- PCB Cost: \$25.40 (\$0.37/in<sup>2</sup>)





# Future Improvements