

# ICACHE MAS

## ICACHE Features

- Memory only writes to icache and cpu only reads from icache.
- Cache line 128bit.
- Number of sets = 16.
- Number of ways = 4.
- Each cache line contains 4 word (32bits).
- FSM state = IDLE, MISS, REFILL.

## ICACHE Interface

NAME	I/O	WIDTH	DESCRIPTION
clk	Input	1	Clock
rst_n	Input	1	Asynchronous reset
cpu_addr_i	Input	ADDR_WIDTH	Address of next instruction from cpu
cpu_inst_o	Output	WORD_WIDTH	Instruction from cache line
cpu_valid_o	Output	1	Valid instruction
cpu_req_i	Input	1	Request from cpu
mem_req_o	Output	1	Request for new cache line
mem_valid_i	Input	1	Valid cache line from memory
mem_addr_o	Output	ADDR_WIDTH	Address from which to get new cache line
mem_inst_i	Input	LINE_WIDTH	New cache line from memory.