TED UNIVERSITY

EE207 DIGITAL DESIGN LABORATORY

PreLab Report For Experiment 3

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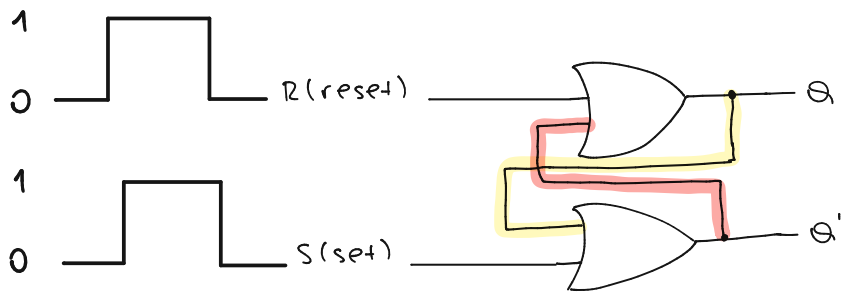
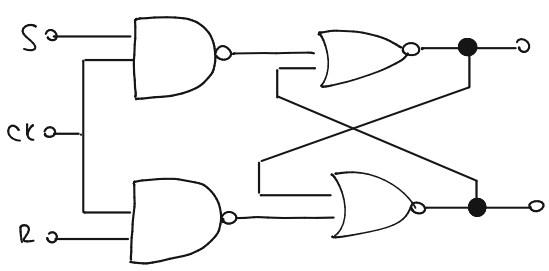
2.1) active-high input SR latch;



S	R	Q	Q'	
0	1	1	0	
0	0	1	0	→ after (S=1, R=0)
1	0	0	1	
0	0	0	1	→ after (S=0, R=1)
1	1	0	0	→ forbidden

2.2) active-high SR flip-flop;



S	R	Q	Q(T+1)
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	?
0	0	1	1
0	1	1	0
1	0	1	1
1	1	1	?

b)

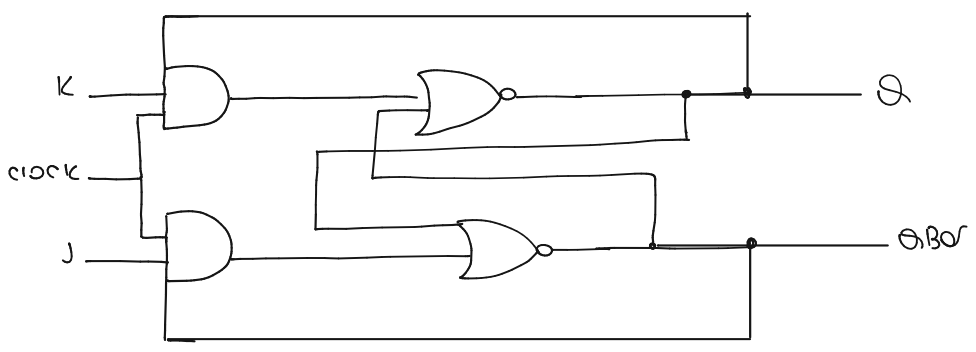
```
library ieee;
use ieee. std_logic_1164.all;

entity SR_FF is
PORT( S,R,CLOCK: in std_logic;
Q, QBAR: out std_logic);
end SR_FF;

Architecture behavioral of SR_FF is
begin
PROCESS(CLOCK)
variable tmp: std_logic;
begin
if(CLOCK='1' and CLOCK'EVENT) then
        if(S='0' and R='0')then
                tmp:=tmp;
        elsif(S='1' and R='1')then
                tmp:='Z';
        elsif(S='0' and R='1')then
                tmp:='0';
        else
                tmp:='1';
        end if;
end if;
Q <= tmp;
QBAR <= not tmp;
end PROCESS;
end behavioral;
```

SR flip-flop has 4 std-logic inputs. they are; reset signal, clock, SR inputs. And 2 outputs; Q and Q'. Since we are using the behavior modeling style, we have a process statement too. It's behavior gets affected by all inputs signals.

When the reset signal is active, the output will be 0. When it's inactive, and rising edge of the clock is present, the behavior shown in the truth table will be activated.

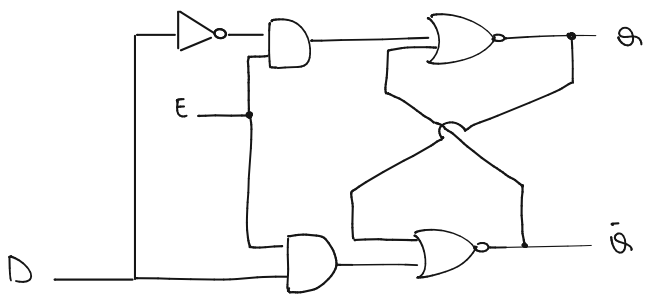
at the end we are closing off the process, the if statements and the architecture.

c) JK flip-flop truth table.



Q	J	K	Q(T+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

d) D latch + truth table;



E	D	Q	$\bar{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

e) Difference between;

It is that latch does not have a clock signal to change state whereas a flip-flop always does. The D flip-flop is an edge triggered device which transfers input data to $\bar{Q}$ on clock rising or falling edge. Data latches are level sensetive devices such as the data latch and the transparent latch.