TECHNICAL DATA

LeCroy

365AL QUAD MAJORITY LOGIC UNIT
465 TRIPLE 4-FOLD LOGIC UNIT
622 QUAD 2 INPUT LOGIC UNIT

- NIM Packaging
- High Speed
- Multiple Input
- Multiple Output
- Selectable Number of Coincident Inputs

FOR HIGH SPEED OPERATIONS

A logic unit generates a precise standard pulse when the inputs correspond to preset logical conditions. The inputs to the logic modules are standard NIM logic levels typically generated by a discriminator or another logic module. The inputs are restandardized and then compared to the setting of the module.

The logical conditions which can be selected are 4-fold, 3-fold (Model 365AL and Model 465), AND (all units) and an OR (Model 365AL and Model 622). If only one input is selected, then the units will act as a logic fan-out. The output of the logic module has a duration that is either the same period as the coincidence of the inputs (465) or is adjustable via a front-panel potentiometer for maximum flexibility. The output of a logic module is typically part of a trigger system which triggers, gates or disables a data acquisition system.

LeCroy's family of NIM logic modules are flexible and versatile. They offer a number of features and can be easily configured.

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Innovations in Instrumentation

FEATURES

Multiple Channels - Each module has up to 3 channels and has 2 or 4 inputs per channel. A minimum of 5 outputs are available.

High Speed - All modules have greater than 110 MHz operation. In addition, all channels have adjustable output pulse widths.

Selectable Logic Function - Each unit has a switch selectable logic function from 4-fold coincidence (365AL and 465), to majority logic (365AL) to AND/OR (622).

High Performance - All three modules experience no multiple pulsing, have good output width stability and as low as 5 nsec double pulse resolution.

FUNCTIONAL DESCRIPTION

LeCroy's NIM logic units offer flexibility, versatility, high speed and performance packaged in a single width NIM module. All together they provide the functions of majority logic, up to 4-fold coincidence, fan-in and fan-out and AND/OR Logic along with > 110 MHz operation. Each of the channels accept up to 2, Model 622, or 4, Model 365AL and Model 465, standard NIM logic signals.

Both the 365AL and the 465 have inputs which maybe individually enabled or disabled without altering cabling or termination by means of front-panel switches. In the 465, with all inputs enabled, four inputs are required. Disabling the logic inputs is equivalent to reducing the number of simultaneous negative input signals required for an output. Thus, each channel may be programmed for 4-fold, 3-fold or 2-fold logic decisions. With only one input enabled, each channel operates as a logic fan-out.

The 365AL, however, has a selectable number of coincidence values to allow programming of one to four simultaneous input signals required for an output. Thus, it can operate similar to the 465 or can be used for the majority logic as well as a logic fan-in. Alternatively, the 622 features 4 channels with switch selectable AND or an OR output condition of the two inputs.

All three units offer at least 2 sets of bridged outputs and at least one complementary output as well as continuously adjustable output pulse duration. The output pulse width is set via a front-panel screwdriver control pot from 5 nsec to 600 nsec for the 622. The outputs are highly stable and independent of input amplitude, duration and rate. All units are updating and can be retriggered before the end of an output pulse. The 465 also has bridged overlap outputs (-32 mA) whose output pulse width is equal in duration to the coincidence overlap.

Note that each unit can be used in a CAMAC crate with the Model 4501A NIM-to-CAMAC adapter.

SPECIFICATIONS

Model 365AL

INPUT

Logic Inputs: 4 Lemo-type connectors; 50 Ω impedance; negative NIM level input requirements; each input can be separately enabled or disabled.
Veto Input: Lemo-type connector; 50 Ω impedance; negative NIM level input requirements. Requires 3 nsec minimum width delayed 3 nsec from leading edge of input.
Bin Gate: Via rear connector; clamp to ground from +4 V inhibit; rise times and fall times < 50 nsec.

OUTPUT

Outputs: 3 pairs; 2 negative (quiescently 0 mA, -32 mA during output), one complementary (quiescently -32 mA, 0 mA during output).
Fan-out: 6-fold, if each output drives two 50 Ω loads. (Any used output pair should drive 25 Ω for proper amplitude and shape.)
Duration: Continuously adjustable from less than 4 nsec to greater than 50 nsec by means of front-panel screwdriver-adjustable potentiometer. Updating.
Output Rise and Fall Times: 1.2 nsec typical. Fall time is 2.2 nsec maximum at 10 nsec pulse width and longer.

GENERAL

Functions: AND; OR; Majority Logic; Leading Edge Inhibit; Complement; Pulse standardization without multiple pulsing; coincidence level determined by front-panel selector.
Coincidence Width: 1 nsec and up, determined by input pulse durations.
Rate: 150 MHz minimum.

Input-Output Delay: Approximately 10 nsec.
Double Pulse Resolution: Typical 5 nsec; (6.5 nsec for triple pulses).
Packaging: NIM single-width module; Lemo-type connectors used for all inputs and outputs.
Power Requirements: 55 mA at +12 V (increases to 120 mA if both channels in 4-fold coincidence), 165 mA at -12 V, 22 mA at -24 V.

Model 465

INPUT

Logic Inputs: 4; Lemo connectors; 50 Ω impedance; negative NIM-level input requirements; each input can be separately enabled or disabled by front-panel push-buttons.
Veto Input: Standard negative NIM-level signal, 3.5 nsec minimum width. Requires complete overlap of input coincidence for linear outputs and prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition for the preset outputs. (Veto should precede this leading edge by approximately 5 nsec in this case.)
Bin Gate: Via rear connector; clamp to ground from +4 V inhibits; rise times and fall times < 50 nsec.

OUTPUT

Preset: 3; one bridged negative (quiescently 0 mA, -32 mA during output) one complementary (quiescently -16 mA, 0 mA during output). Updating.
Overlap: One bridged negative; quiescently 0 V, -32 mA during output; duration equal to coincidence overlap. Non-updating.
Fan-Out: 5 fold, if each output drives a 50 Ω load.
Duration: Continuously adjustable from less than 5 nsec to greater than 500 nsec by means of front-panel screwdriver-adjustable potentiometer. Width stability better than ±0.2%/°C.
Output Rise Times: OUT: 2.0 nsec typical (maximum 2.5 nsec). $\overline{OUT}$: 2.2 nsec typical (maximum 2.5 nsec; 3.0 nsec with negative output unterminated).
Output Fall Times: OUT: 2.0 nsec typical (maximum 2.5 nsec). $\overline{OUT}$: 2.2 nsec typical (maximum 2.5 nsec). Both are slightly longer on wide output durations.

GENERAL

Functions: 2-fold, 3-fold, or 4-fold coincidences plus fan-out determined by selectively disabling logic input.
Coincidence Width: ≥ 1 nsec, determined by input pulse durations.
Rate: 0 to > 120 MHz.
Input-Output Delay: 13 nsec for preset outputs; 8.5 nsec for overlap output.
Double Pulse Resolution: 8 nsec.
Multiple Pulsing: None; one and only one output pulse of preset duration is produced each time the input conditions are satisfied regardless of the duration of the input pulses or their overlap.
Packaging: Single-width AEC/NIM module; in conformance with AEC standard; Lemo connectors used for all inputs and outputs.
Power Requirements: 65 mA at +12 V, 135 mA at -12 V, 125 mA at +6 V, 640 mA at -6 V, 5 mA at -24 V.

Model 622

INPUT

No. of Channels: 4, all identical.
Logic Inputs: 2, 50 Ω direct-coupled; reflections < 7% for standard negative NIM of 2 nsec rise time.
Veto Input: Front-panel connector permits simultaneous inhibiting of all channels; 50 Ω; requires negative NIM-level signal; direct-coupled; must overlap leading edge of input signal that would otherwise cause the coincidence condition; must precede input by approximately 5 nsec.
Bin Gate: Via rear connector, with rear-panel ON/OFF switch; quiescently +4 V, clamping to ground inhibits logic unit; direct-coupled; rise times and fall times approximately 50 nsec.

OUTPUT

Bridged Negative: 2 pairs; NIM (quiescently 0 mA, -32 mA during output), duration, 5 nsec to 1 μsec, continuously variable up to 600 nsec via front-panel screwdriver control (narrower widths possible at slight expense of amplitude); rise times and fall times (all outputs terminated in 50 Ω) typically 2.0 nsec (maximum 2.5 nsec). Output fall times slightly longer on wide output durations. Width stability better than ±0.2%/°C maximum. Updating.
Fast Negative Timing: One NIM (quiescently 0 mA, -16 mA during output). Other characteristics same as above, except rise times are typically 1.5 nsec (maximum 2.0 nsec) and minimum width is ≤ 6 nsec.
Complementary: One NIM (quiescently, -16 mA, 0 mA during output). Other characteristics same as for Fast Negative Timing Output.

GENERAL

Functions: Fan-in (2-fold); coincidence; inhibit.
Coincidence Width: Determined by input pulse durations; total widths approximately 1.0 nsec and up.
Rate: 110 MHz typical, input and output.
Input-Output Delay: 9.5 nsec typical.
Double Pulse Resolution: < 9 nsec at minimum output width setting.
Multiple Pulsing: None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.
Packaging: In RF-shielded, AEC/NIM #1 module (AEC Report #TID-20893); Lemo-type connectors.
Power Requirements: 450 mA at -6 V, 215 mA at +6 V, 165 mA at -12 V, 20 mA at +12 V, 85 mA at -24 V.

NIM LOGIC UNIT SELECTION CHART

Model	365AL	465	622
INPUT			
No. of Channels	2	3	4
No. of Inputs	4	4	2
FUNCTION			
Logic	Majority 4-fold selectable coincidence level	Up to 4-fold	AND/OR
GENERAL			
Packaging	Single-width NIM	Single-width NIM	Single-width NIM
Maximum Rate	150 MHz	120 MHz	110 MHz
D.P.R.	5 nsec (6.5 nsec for triple pulses)	8 nsec	< 9 nsec
OUTPUT			
No. of Outputs	4 NIM, 2 $\overline{\text{NIM}}$	Preset: 2 NIM, 1 $\overline{\text{NIM}}$ Overlap: 2 NIM	4 NIM, 1 Fast NIM Timing, 1 $\overline{\text{NIM}}$
Width	4 nsec to 50 nsec	5 nsec to 500 nsec (preset only)	5 nsec to 1 µsec
POWER			
-24 V	22 mA	5 mA	85 mA
-12 V	165 mA	135 mA	165 mA
-6 V	600 mA	640 mA	450 mA
+6 V	425 mA	125 mA	215 mA
+12 V	55 mA (120 mA if both in 4 fold coincidence)	65 mA	20 mA

SPECIFICATIONS

Logic Inputs

The Model 622 has direct-coupled, 50 Ω impedance inputs which accept fast NIM logic signals. These inputs, typically driven from a discriminator or other logic unit, are protected both for transient and DC signals up to ±5 V. Since the input reflections are less than 7% for signals of as little as 2 nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e., -1.8 V) will reflect only approximately 125 mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

1.3 Common Inhibit Input

The common inhibit input of the 622 requires NIM logical one input signals. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the entire input signal that would otherwise cause the coincidence condition. Due to internal delays, the leading edge of the veto signal should precede the coincidence by at least ≤5 nsec (see Figure 1.1).

To veto signals when the 622 is set in the "OR" condition, the inhibit signal must merely overlap the pulse it is to inhibit, subject to the ±5 nsec delay mentioned above.

Bridged Output

The Model 622 has two pairs of current source 50 Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. These outputs are of the switched current source type, requiring no quiescent current and permitting extremely low power dissipation in the total circuit. The standard switched current outputs maintain a risetime of 2.5 nsec and a reasonably clean shape, as long as care is taken to terminate at least one-half of the other bridged output in that channel.

The shape of typical outputs from a 622 are shown in Figure 1.2.

Using the typical output pulse shape in Figure 1.2 as a visual reference, LRS output shapes for current switched outputs (such as on Models 622, 621L, 621AL, 621BL, 621BLP) are set up to adhere to the restrictions in Figure 1.3, with adjacent output pair terminated into 50 Ω.

In applications where it is necessary to drive very long cable lengths from a logic unit output it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively sends all 32 mA into the one cable, giving nearly a double amplitude output. It is important to know that the 622 has clamp diodes that limit the output amplitude so as not to saturate

the output transistors. This limit is approximately -1.4 V. It cannot be assumed, therefore, that the 32 mA into one 50 Ω cable will give a 1.6 volt output signal.

1.5 Fast Negative Timing Output

The fast negative timing output on the 622 is a full differential type current source output. Its name originates from the shorter risetime (1.3 nsec vs. 2.5 nsec) compared with the other 4 negative outputs on the 622. Because the risetime is much faster, there is less timing inaccuracy created by differing "threshold" levels of subsequent circuits.

1 6 Complementary Output

The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to the fast negative timing output. It is a 50 Ω output with quiescent level at -16 mA, and logical 1 at 0 mA. Risetime and other characteristics are similar to that of the fast negative timing output.

1.7 Output Width

The output range of the Model 622 is 5.0 nsec to 1 μsec, continuously adjustable via front-panel potentiometer. Because the potentiometer is very sensitive beyond 600 nsec, it is actually almost impossible to set the width between 600 nsec and 1 μsec. As a result, the specifications indicate continuous adjustment up to 600 nsec, with a = 1 μsec setting at the far end of the pot.

1.8 Output Width Uncertainty

External conditions are the main contributions to output uncertainty in the Model 622. Variations in both temperature and NIM bin voltage can cause slight changes in output width with consequences that may be adverse to subsequent coincidence measurements. If the output pulses are to be simply counted, then the leading edge is the important factor and width variations are unimportant.

Figure 1.4 indicates the uncertainty in output width of the 622 as a function of reasonable variations in temperature and supply voltage. Since the 622 has power supply regulation in it and is very well temperature compensated, the width variations are small.

1.9 Coincidence Characteristics

Minimum Coincidence Overlap (Coincidence Resolving Time): The required coincidence overlap time of two input signals with the 622 set in the "AND" mode is approximately 1.1 nsec. Although this measurement should be made with two pulses of zero risetime for an absolute result, functionally, no discriminator or other logic unit driving the 622 could output such fast pulses. The measurements on the 622 were therefore made with an LRS Model 161 Dual Discriminator

of 1.5 nsec risetime and falltime.

One method used at LRS is to measure the overlap time is as follows. Two 10 nsec FWHM pulses from a single source are initially separated in time and fed into the inputs of the Model 622. The output of the 622 is displayed on an oscilloscope which is being externally triggered by the source (see Figure 1.5). One pulse is then moved in time until it begins to overlap the other pulse. Initially, no output will appear from the 622 (see Figure 1.6). At some duration of overlap, output pulses will always appear. The minimum coincidence overlap is defined in LRS terminology as that amount of overlap which produces one output on the average for every two sets of inputs (i.e., 50% point). From the waveforms below this is equal to T_2-T_0. The 50% point can be quite accurately estimated on the oscilloscope (externally triggered) by adjusting the second pulse delay for equal intensity of trace (of the output states) for the duration of the output pulse. The minimum resolving time for the Model 622 is 1.1 nsec. The resolving time jitter can also be measured by taking the difference between the 0% limit and the 100% limit (T_3-T_1). The resolving time jitter for the Model 622 is ± 20 psec.

1.10 Coincidence Curve Method of Measuring Resolving Time

An alternate method used at LRS to measure the resolving time and time jitter involves making a coincidence curve and then measuring its "risetime" and "falltime". Two pulses from a single source are initially separated in time and fed into the inputs of the 622, at the same time being collectively counted in a scaler (see Figure 1.7). The 622 output is also counted into another scaler channel.

As the variable delay is adjusted, the two pulses become more coincident. By comparing the counts in the two scaler channels at different delay amounts, a curve can be made representing Rate Out/Rate In vs. Time Delay where the time delay is measured from the trailing edge of Pulse A to the leading edge of Pulse B. (The previous waveform diagram is valid for this measurement also, except Pulse A delay should be continued until its leading edge is past the trailing edge of Pulse B).

The resultant coincidence curve for this measurement appears in Figure 1.8.

The minimum coincidence overlap or minimum resolving time of the logic unit is defined as one-half the difference between the sum of the input pulse widths and the coincidence width measured above. Alternately (but with more difficulty), if t_0 represents the time at which pulse A trailing edge and Pulse B leading edge are exactly coincident in time, then the minimum resolving time is equal to t_2-t_0.

If input pulses A and B are identical in shape, and if the inputs to the coincidence unit are identical, the trailing edge side of the coincidence curve should be symmetrical to the leading edge. If they differ, the larger one (either 0% to 100% or 100% to 0%) is specified

as the resolving time jitter.

It is important to note that the major contribution toward resolving time jitter in typical logic units is the instability of the "threshold" level of the differential amplifier following the input "AND" stage, particularly for inputs with slow inherent risetimes (i.e., $\geq$ 2 nsec). In the 622, a true high sensitivity discriminator is used which has a very stable and jitter-free threshold (the LD601C hybrid used in all LRS multichannel NIM discriminators). For this reason, the resolving time jitter of the 622 is quite small.

1.11 Timing Characteristics

Maximum continuous pulse train (CW from RF terminology) rate capability of the 622 is guaranteed at 100 MHz. Typically, the maximum rate is 110 MHz, with some units being capable of operation up to 120 MHz for small bursts of input pulses. The measurement for maximum rate is made by applying pulses to one of the two inputs, with the mode switch set in the "OR" position.

The double pulse resolution (DPR), as opposed to CW rate capability, defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur, whereas a CW input pulse train would be unlikely. For a logic unit in the "AND" mode, the coincidence width of the input pulses would limit the double pulse resolution of the unit. Each input itself is capable of operation at a 110 MHz CW rate and a DPR of 9 nsec. This measurement is made by setting the 622 in the "OR" mode, putting in two 4 nsec FWHM pulses spaced approximately 10 nsec apart at the half maximum points (i.e., -375 mV for a -750 mV input signal) and finding how far this 10 nsec time difference can be lowered before the 622 output pulse achieves only a 50% firing rate (i.e., Rate Out/Rate In = 0.5). Alternately, with the 622 set in the "OR" position, two pulses can be fed from different cables into the two inputs. By varying the time from leading edge of one (half max. point) to the leading edge of the other, the DPR can be measured. Care should be taken to use pulses of as narrow a width as possible when measuring minimum double pulse resolution.

1.12 Packaging

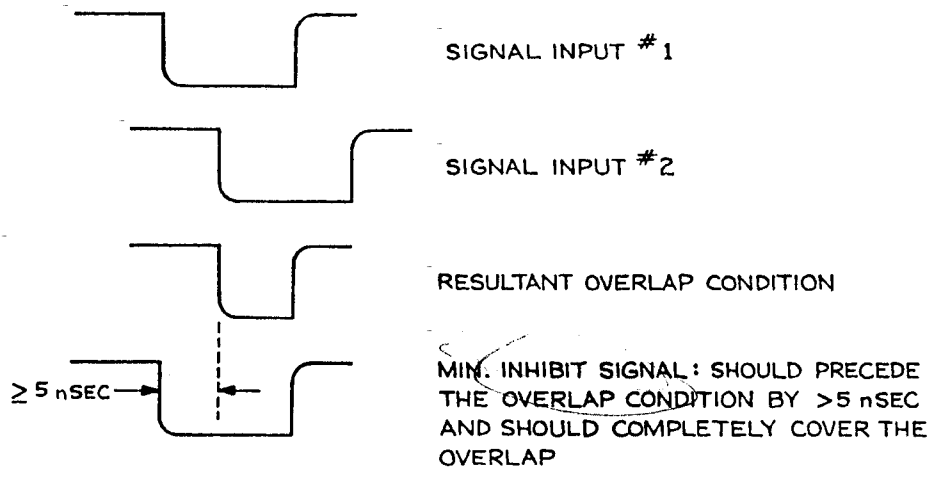
The 622 Quad Coincidence Unit is packaged in a #1 NIM module with Lemo-type connectors. Due to front panel space limitations, the 622 is not offered with BNC's.

1.13 Power Requirements

The current usage of the 622 is low enough to permit the use of the 12 modules per standard 96-watt NIM bin offering 5 A of +6 V, 2 A of $\pm$12 V, and 1 A of $\pm$24 V. The maximum power used is 7.8 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot.

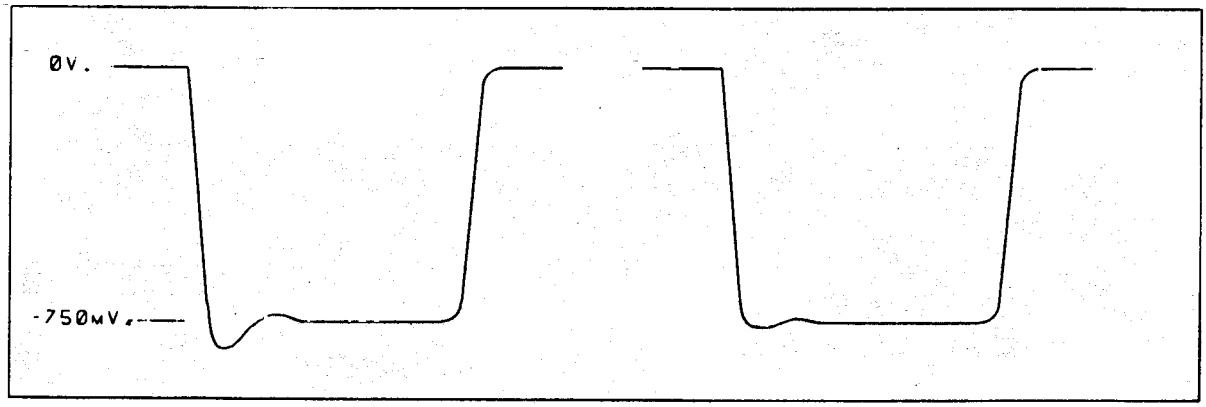
1.14 Recommended Use of the NIM Power Bins

It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.



INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

Figure 1.1

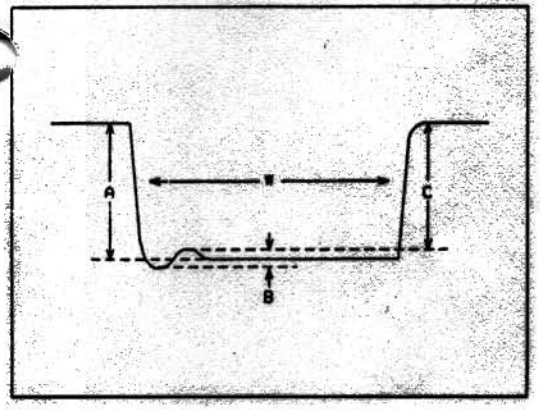


SWITCHED CURRENT OUTPUT, ADJACENT OUTPUT PAIR UNTERMINATED:
TR-2.5 NSEC: OVERSHOOT <15%

SWITCHED CURRENT OUTPUT, ADJACENT OUTPUT PAIR TERMINATED:
TR-2.0 NSEC: OVERSHOOT <10%

MODEL 622 OUTPUT WAVEFORMS

Figure 1.2



AMPLITUDE -700mV<A<-850mV

OVERSHOOT B<10% OF A; C DOES NOT REACH -600mV

RISETIME: <2.5 NSEC.

FALLTIME <2.5 NSEC. AT MINIMUM WIDTH.

MINIMUM WIDTH WMIN (FWHM) <5.0 NSEC.

MAXIMUM WIDTH WMAX (FWHM) - 1 USEC.

Figure 1.3

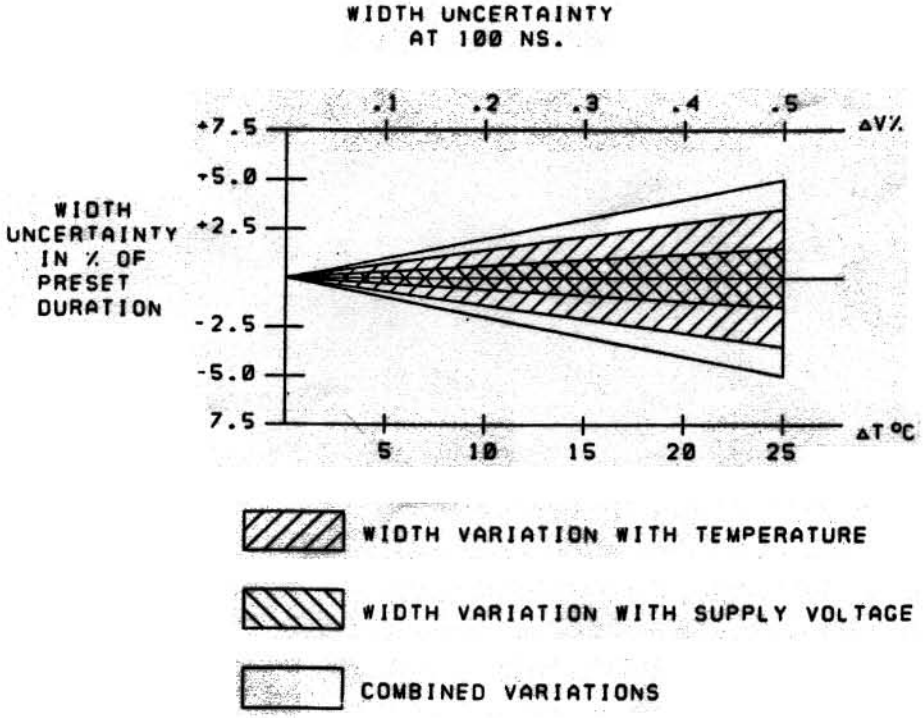


Figure 1.4

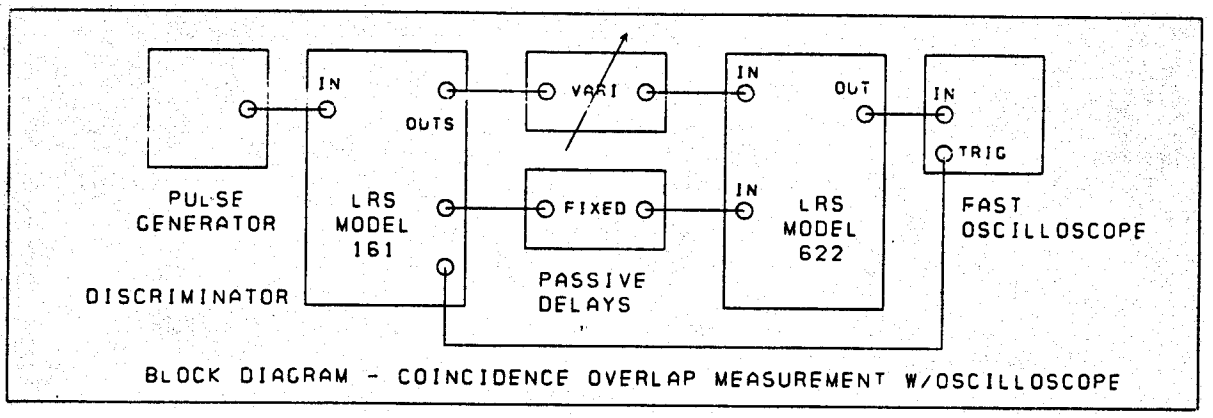


Figure 1.5

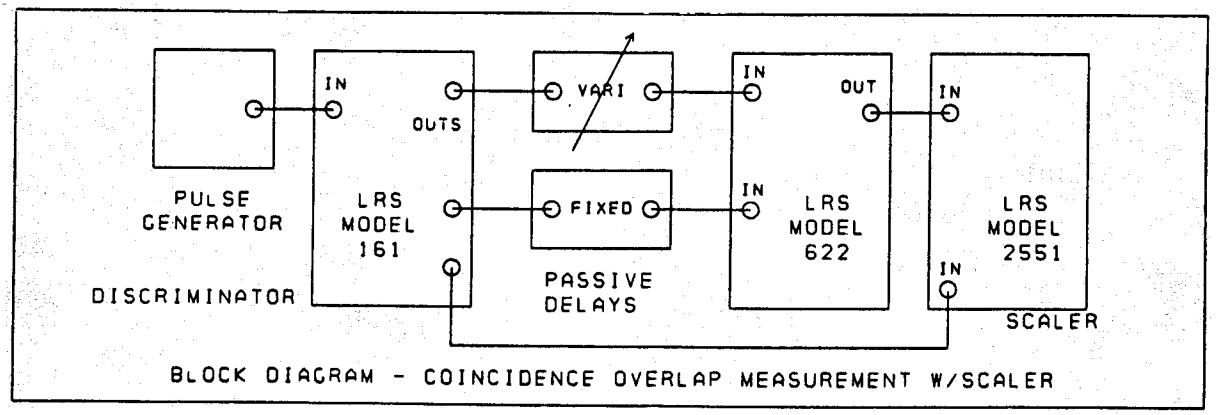


Figure 1.6

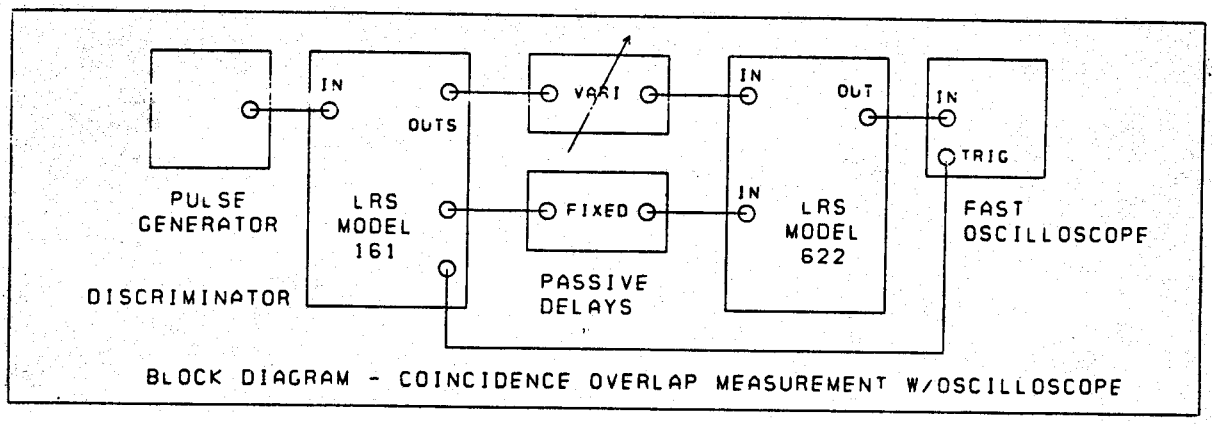


Figure 1.5

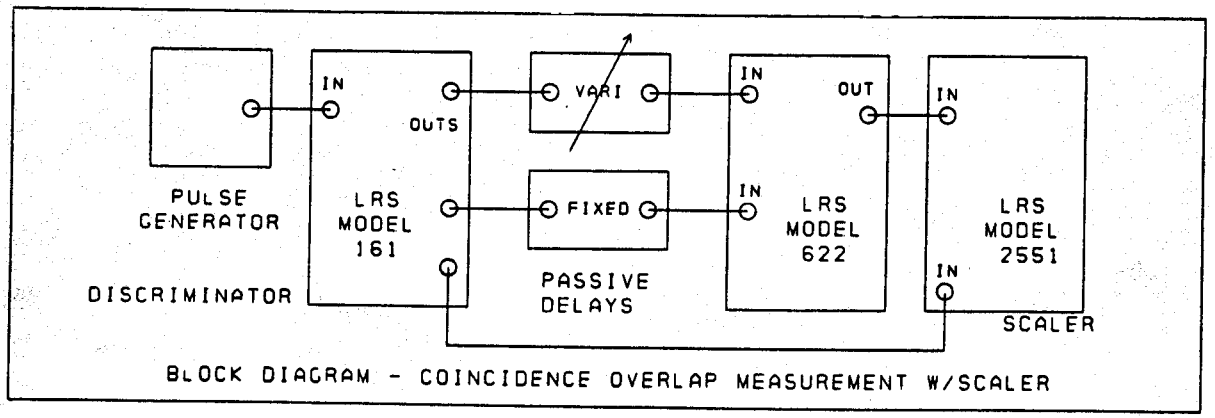


Figure 1.6

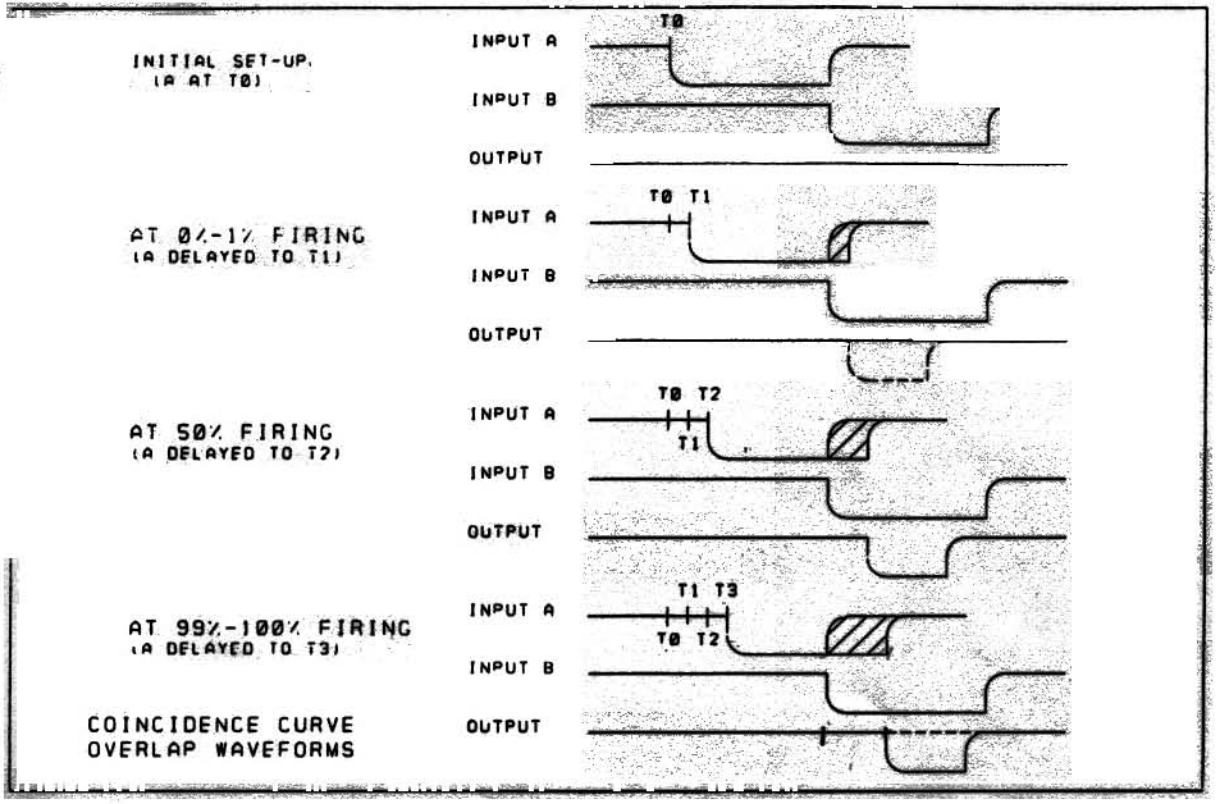


Figure 1.7

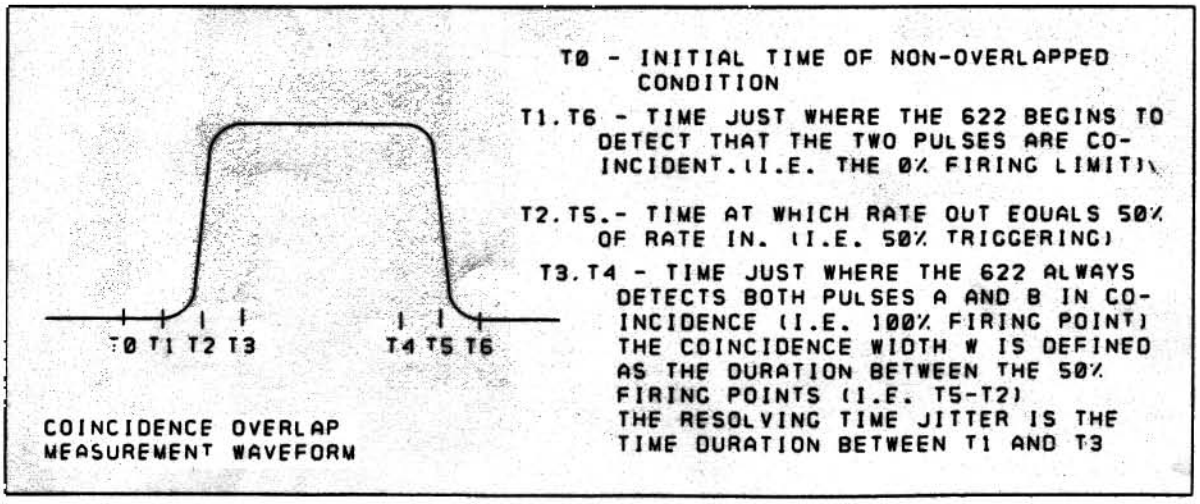


Figure 1.8

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 General

Each of the four channels of the Model 622 is composed of four basic sections. The Input Logic-Level-to-Analog Converter, the Discriminator Stage, the Timing or Pulse-Former Stage, and the Output Stage. A block diagram of the Model 622 can be in Figure 2.1 and a complete schematic can be found at the end of this manual.

2.2 Input Logic-Level-to-Analog Converter

The input stage accepts two inputs, and (via a two diode current switch) removes one unit of current per input from the resistor diodes connected to the -IN of the LD601C. The result is that with no inputs, the voltage at -IN is near zero V, with one NIM-level input the -IN voltage will go to about -250 mV, with two inputs it goes to about -450 mV to detect the existence of two time coincident inputs (AND mode).

2.3 Discriminator and Pulse Standardizer Stage

The discriminator and pulse former stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator as is functionally presented below. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small amount of internal positive feedback to provide regeneration at threshold. In actual operation the V_T is grounded, and the threshold level is determined by the 2.5:1 (AND) or 4:1 (OR) voltage divider (composed of the switch selected external 150 Ω or 300 Ω resistor and the internal 100 Ω resistor) operating from -0.8 V (Figure 2.2).

When an input signal applied to -IN is equal to the threshold voltage at +IN the amplifier output will begin to go positive. This will force +IN closer to 0 V, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (Pin 6). The quiescent level should be nominally -2.4 V going to -1.6 V during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate and veto) must be off. The required level at Pins 7 and 16 of the LD601 must be 0 to -1.6 V to enable, and -2.5 to -6.0 to disable. The purpose of the first inhibit is to avoid generating a low level transient at the output associated with the leading edge of an amplified input pulse inhibited at the dV/dt stage only. (The common inhibit driver provides a level shift so that 0 V at the bin gate or -600 mV at the veto input will inhibit, greater than +3 V at the bin gate input or 0 V at the veto input will enable). Once the latch is set, a latch OUTPUT is available to start

the 622 timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL. OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external section of RC time constant and voltage levels at Pin 3. It is set at approximately 3 nsec in the Model 622.

Older 622's used LD601B hybrids, while more recent units use LD601C's. These two hybrids are identical and interchangeable.

2.4 Timing Stage

The timing or pulse-forming stage of the 622 utilizes three stages of MC1692 MECL receiver for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601C (via one MC1692 stage) and the differential stage (composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604 Ω emitter resistor. The actual current is varied from near zero (for the 1 μsec maximum width) to about 10 mA (for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, T, sets the minimum width to 5 nsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The 1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601C to the timing stage, as well as driving the output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601C output, independent of the delay encountered in initializing the timing stage. Before the 601C output is over, the timing capacitor is charged, causing the third 1692 amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing until the timing capacitor is subsequently discharged to a sufficiently low level (approximately -2.0 V)). At this point (because of regeneration) the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

2.5 Output Stage

The output stages of the 622 utilize two different types of circuits. The single normal and complementary outputs use a conventional differential stage. This stage requires a continuous 16 mA of current which is quiescently available at %the complementary output connector. During an output pulse, the MC 1692 receiver will switch from the quiescent level of -2.4 V to a higher level of -1.6 V,

causing the differential stage to switch the 16 mA current from the complementary to the normal output connector for the duration of the pulse. The other two pairs of outputs each supply 32 mA of current during the pulse, because at this time the bases of the two A430 transistors are at -1.6 V. The emitters are therefore at about -2.4 V. This places about 600 mV across each 16 Ω emitter resistor, and the resulting 32 mA will be available at each output connector pair for the duration of the pulse. Quiescently, the bases of these transistors are at -2.4 V; therefore, there is only a -600 mV drop available for V_{BE} so the transistors are off, resulting in a substantial power saving.

All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, even on a single output stage, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages.

The amplitudes of the Model 622's can be trimmed, if necessary, with resistors (labeled T) in parallel with the 10 Ω emitter resistors.

2.6 Internal Power Supplies

Four internal power supplies are used to generate the -0.8, -2.35, -3.0, and -11.5 V which are special bias voltages used by the four channels. These stages provide voltage regulation and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but during use in a normal bin environment, these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is sequenced on before the +6 voltage, the LD601C may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC, is energized. This insures that the +6 is up before the -6 in any power-on sequence.

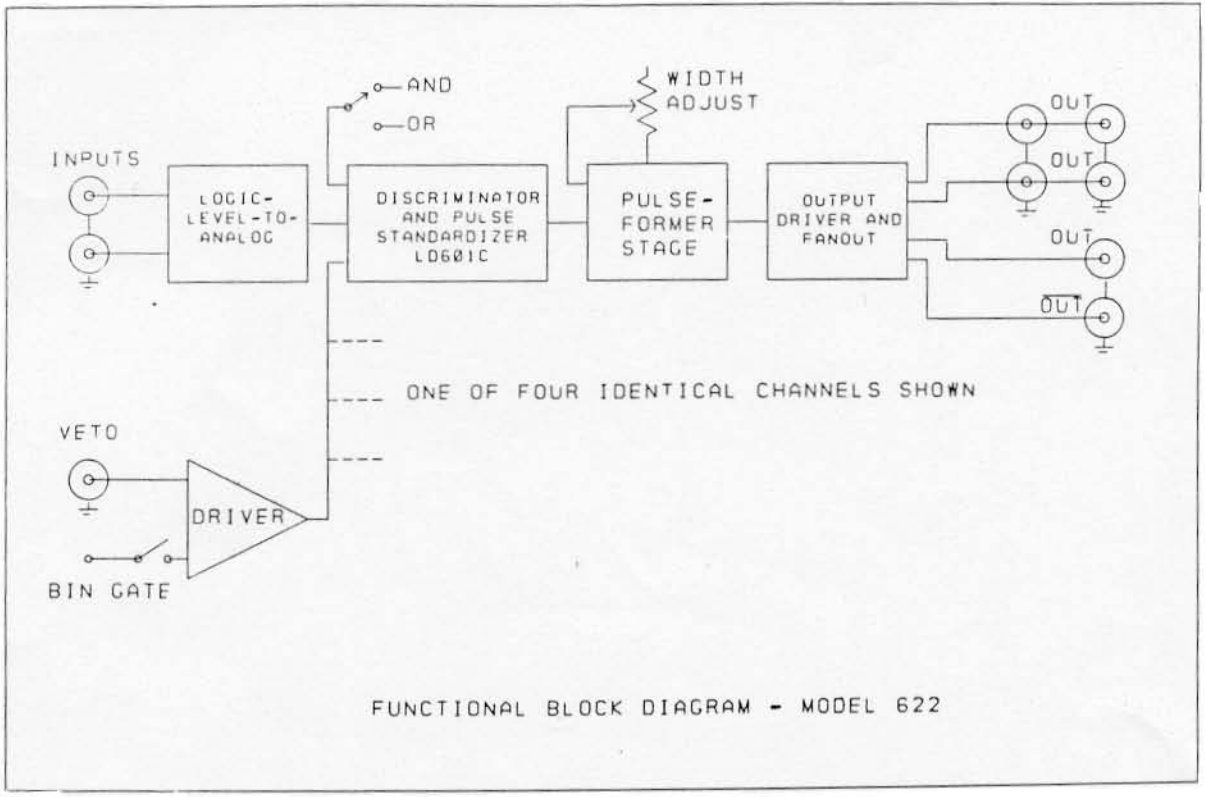


Figure 2.1

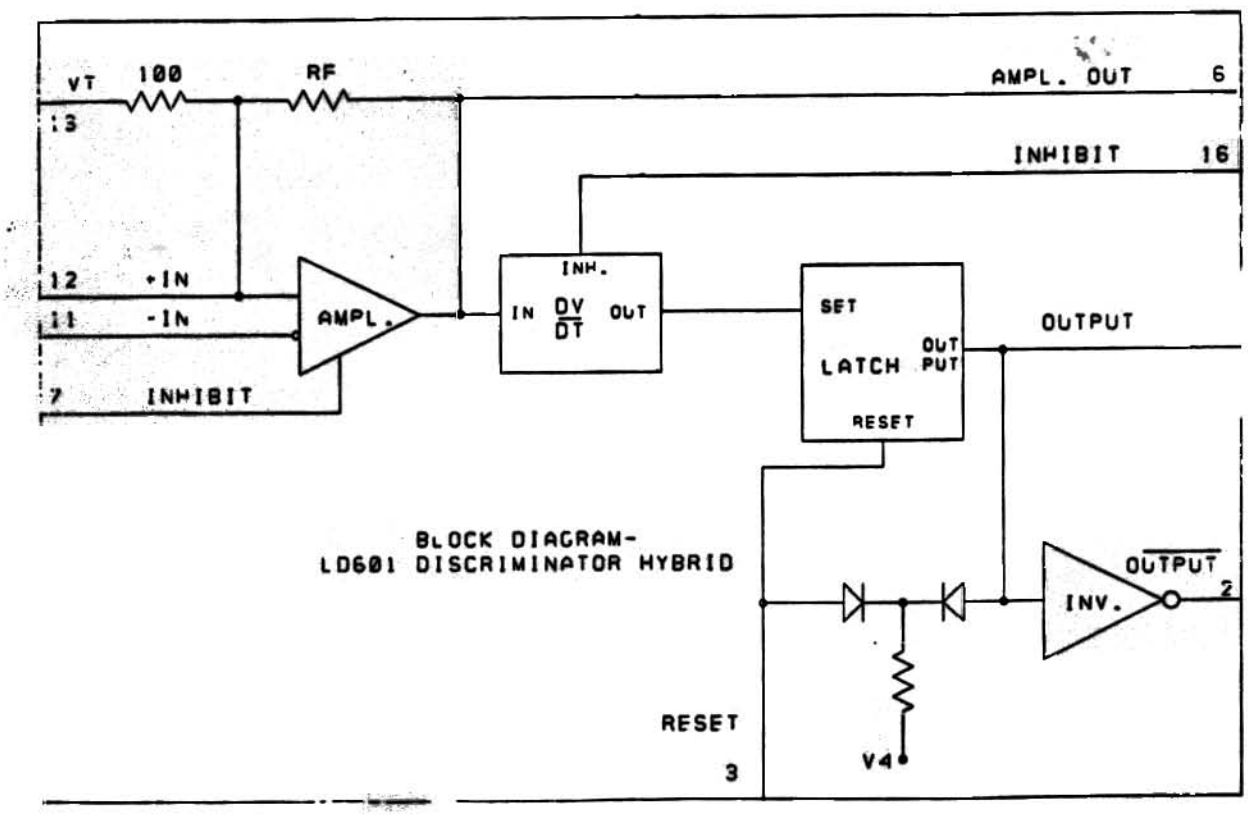


Figure 2.2