## HDI Stackup Planner — Detailed Report for HSP-189472 Option A

## Sierra Circuits, Inc.

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## **Customer Input**

Part Number/ Rev : amINO/ 1.0

PCB Size in X : 0.51 inches X 0.59 inches

Number of layers : 6 PCB Thickness :0.031 inches Material : NP175 Outer Layer :Signal

MicroVia	s depicted by		Finished Copper Weight	Finished Thickness (inches)
	SOLDER MASK			0.0005
L-1	TOP SIGNAL	rand brane.	1 Oz	0.0014
	DIELECTRIC			0.0035
L-2	PLANE		0.5 Oz	0.0007
	DIELECTRIC			0.0040
L-3	SIGNAL	rant hans	0.5 Oz	0.0007
	DIELECTRIC			0.0085
L-4	SIGNAL	1000	0.5 Oz	0.0007
	DIELECTRIC			0.0040
L-5	PLANE		0.5 Oz	0.0007
	DIELECTRIC			0.0035
L-6	BOTTOM SIGNAL		1 Oz	0.0014
	SOLDER MASK			0.0005
		Total Thickness	0.0301 (inches)	

Customer Saved I	mpedance Results			
Layer	Impedance Model	Impedance (ohms)	Trace Width (mils)	Space (mils)
Layer 1	Soldermask Coated Microstrip Single-ended	51.7	5	
Layer 1	Soldermask Coated Microstrip Differential Pair	90.03	5	6
Layer 3	Stripline Single-ended	51.11	4.5	

## **Stackup Details**

Number of Layers	Number of Signal Layers	Number of Sequential Laminations	Number of Plane Layers	Maximum Number of Laser Drills	Mechanical Drills
	4	0	2	0	1

Technology Parameters and Cost Index			Via Set Information		
PCB TECHNOLOGY LEVELS	Level 1	Level 2	Level 3	Level 4	This stack up supports the following via set
Mechanical Micro via Drill diameter (in mils)	8.00	8.00	7.00	6.00	L1-L6
Mechanical Micro via Pad diameter (in mils)	16.00	14.00	13.00	12.00	
Micro Via Drill Diameter (in mils)	6.00	6.00	6.00	4.00	
Micro Via Pad Diameter (in mils)	14.00	12.00	12.00	10.00	
Trace Width Top Layer (in mils)	5.00	4.50	4.00	4.00	
Trace width Inner Buildup Layers (in mils)	4.50	4.00	3.50	3.00	
Trace Width Inner Core Layers (in mils)	4.50	4.00	3.50	3.00	
Trace Width Bottom Layer (in mils)	5.00	4.50	4.00	4.00	
Cost Index	1.9	2.2	2.7	3.2	

6L\_STD\_4S-2P\_OS\_T031\_A

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