ENEL 453 Lab 4: Pulse-Width Modulation

1. Revision History

Version	Comments
v1	Initial document

Path: C:\Users\donen\Dropbox\U of C\Teaching\ENEL 453\ENEL 453 F2020\Labs\Lab 4\ENEL 453 Lab 4 v1.docx

2. Introduction

This is the fourth lab project of the course and its focus for the team is to use Pulse-Width Modulation (PWM) to control a buzzer and the LEDs and 7-segment displays of the DE10-Lite board. You will extend the design of Lab 3 to interface the buzzer and add the PWM functionality, to provide proximity alarm features. The functionality of Lab 3 must be preserved, except for displaying the SW positions on LEDR.

The prerequisite knowledge for Lab 4 is a solid understanding of your Lab 3 design and a solid understanding of using the Quartus and ModelSim tools and debugging.

3. Technical Requirements

3.1. Modify the functionality of your Lab 3 by controlling the brightness of the LEDR as a function of distance, using PWM.

1. The prior functionality of presenting the SW slide switch positions on the LEDR is now eliminated to allow the brightness control.
2. When the distance measured is off scale (i.e. there is no target in front of the distance sensor (e.g. greater than 40 cm for my system)), then the LEDR must be off.
3. When a target is gradually brought closer to the distance sensor, the brightness of the LEDR must gradually increase, reaching maximum brightness at the closest measurable distance (e.g. around 3.5 cm for my system).

Hints:

- This is the easiest of the requirements, so you should start here.
- The PWM_DAC module will useful, either in its current form or your own modified form. If it's not already obvious, you should use the *distance* signal as a control signal to PWM_DAC (not the *voltage* or the *adc_out* signal).
- You may wish to consider using the *distance* signal to control the *duty_cycle* input of PWM_DAC. This is because the PWM_DAC output signal's duty cycle will control the brightness of the LEDR.
- You should write a testbench for PWM_DAC and study its behavior to understand how it works and to decide whether you need to modify it.

3.2. The 7-segment displays must start flashing when a target is 20 cm or closer. At 20 cm, the flash rate will be the slowest. Then when the target is gradually brought closer, the flash rate must gradually increase and flash rapidly at the closest measurable distance (e.g. 3.5 cm for my system). At target distances greater than 20 cm, the 7-segment displays must not be flashing at all.

Hints:

- This is a challenging requirement and it will take you time and effort to meet it. You will probably need to use a modified version of PWM_DAC and the downcounter modules, plus any other required modules you develop. You should write a testbench for PWM_DAC and downcounter to study their behavior to understand how they work and to decide whether you need to modify any of them.
- The downcounter module will be very useful to "slow down" the PWM_DAC operation so that its effects are visible to the human eye. You would connect the *zero* output of the downcounter module to some sort of "enable" signal in the PWM_DAC, so that the PWM_DAC would only count when enabled by downcounter.
- Be prepared to iterate your design to achieve a good range of flash rates.

3.3. The buzzer must always be on (i.e. buzzing) and must increase in frequency as the target is brought closer to it, reaching a maximum frequency (e.g around perhaps 5 kHz) at the closest measurable distance (e.g. 3.5 cm for my system). When there is no target, the lowest frequency could be around 300 Hz.

Hints:

- This is a challenging requirement, but the hardware required is almost the same as the previous requirement for flashing the 7-segment displays.
- You will have to edit the .QSF file to add your PWM output signal for the buzzer. It is suggested to use the ARDUINO_IO[2] pin in the .QSF, for your PWM output. Recall that you have to edit the .QSF in two places!! Refer to the figures in this document to show you how to connect the buzzer to your DE10-Lite board.
- Be prepared to iterate your design to achieve a good range of buzzer frequencies.

3.4. The system reset must be an asynchronous active-low reset_n as it was for Lab 1. This applies to any new modules you add to the design. All flip flops except those of the synchronizer, must have reset.

3.5. Synchronous Design: The design must be synchronous, meaning that whenever you use a clocked process, it must always be rising_edge(clk). Not falling_edge(clk) nor rising_edge(some_other_signal), etc. Further to synchronous design, all asynchronous inputs to the design must be synchronized (already covered by the synchronizer and debounce circuits). No Latches are permitted to be used in the design.

4. Resources Provided

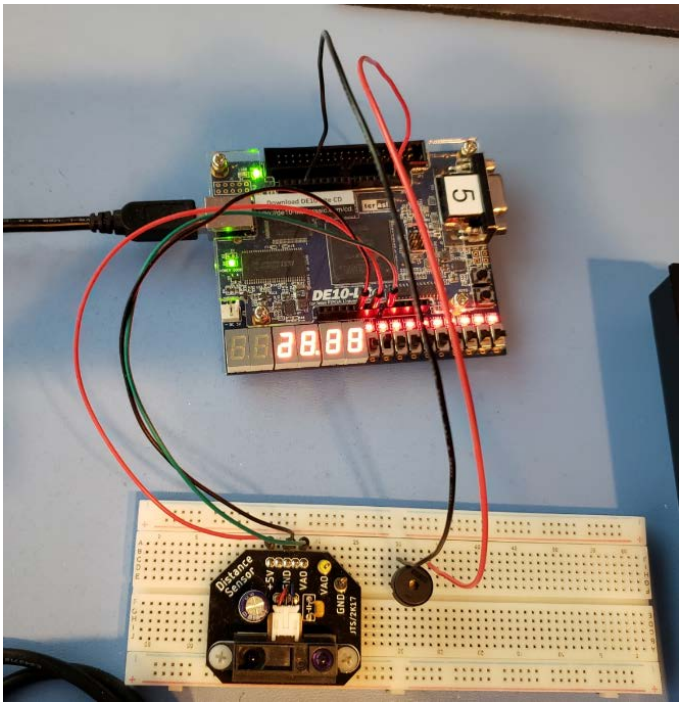
- DE10-Lite kit, Distance Sensor, prototyping kit with jumper wires and breadboard, multimeter, and buzzer.
- Reference code PWM_DAC.vhd and downcounter.vhd.
- Lab and lecture videos.

5. Supporting Information

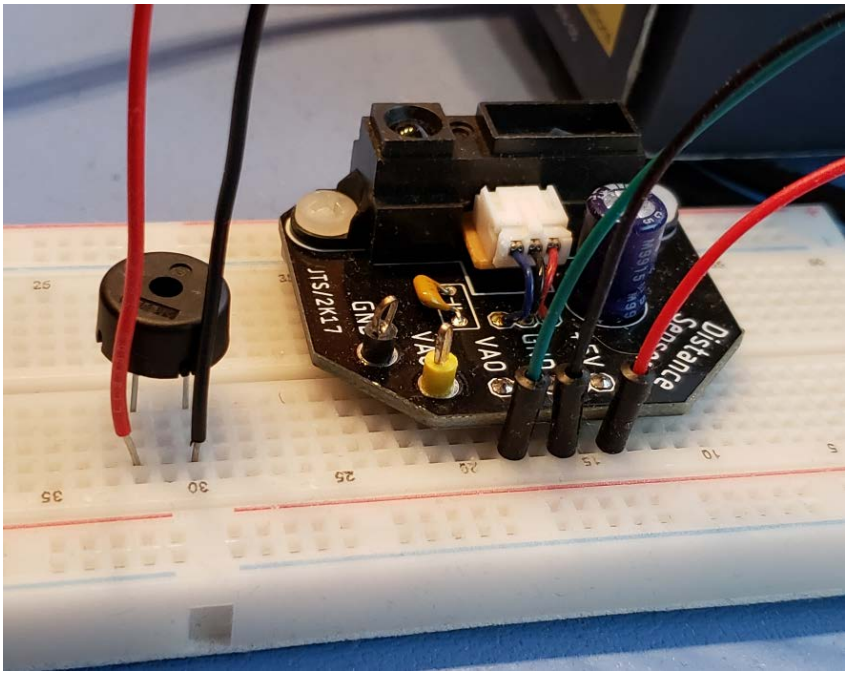
5.1. Connecting the Buzzer to the DE10-Lite

If you are using the ARDUINO_IO[2] pin following the instructor's reference design, you would connect the buzzer as shown in the pictures below.

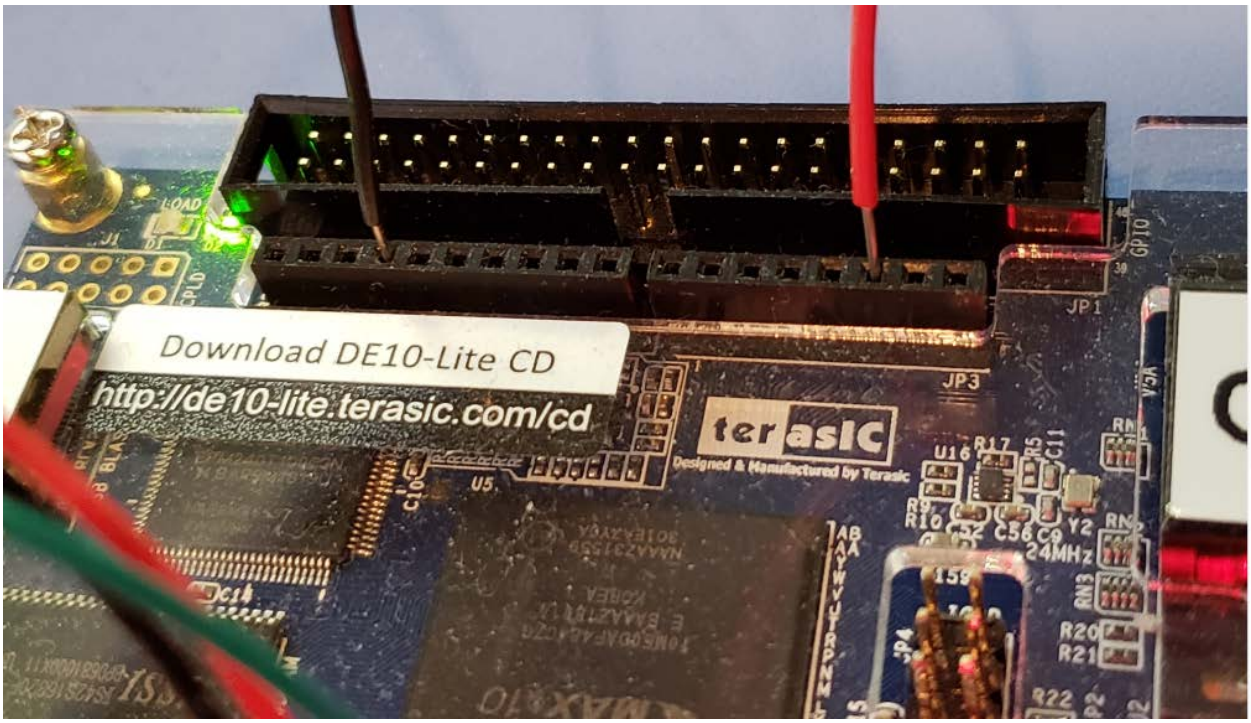
Overall connections.



Close up of buzzer connections. The buzzer has no polarity, so the wires can be switched around.



Close up of DE10-Lite connections.



A view of the buzzer connections circled in red on the DE10-Lite board Arduino header from Terasic documentation (basically a repetition of the above figure but in a different format).

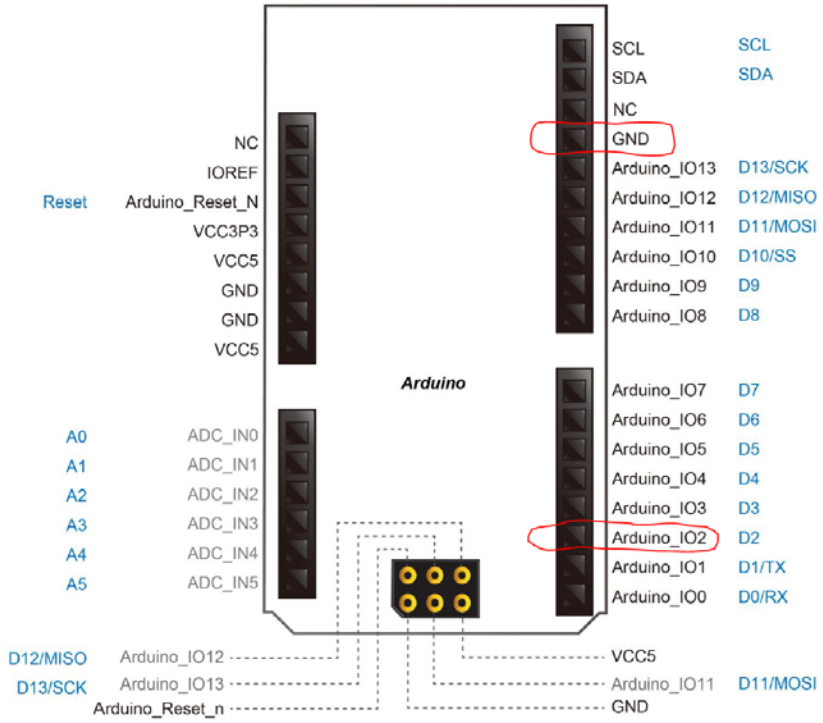
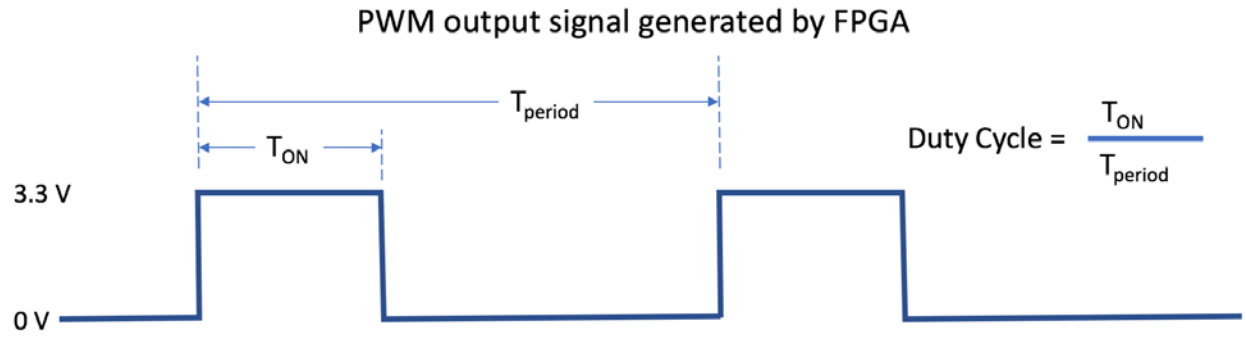


Figure 3-19 lists the all the pin-out signal name of the Arduino Uno connector. The blue font represents the Arduino pin-out definition.

5.2. PWM Basics

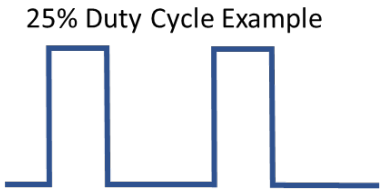
A brief description of the PWM DAC operation is given below.



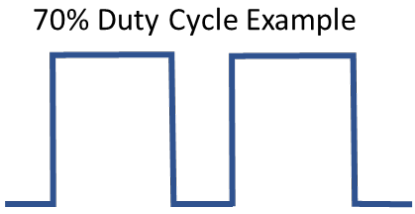
The FPGA output is a square wave with a variable ON time, or T_{ON}. The period of the square wave is T_{period}. The ratio of T_{ON}/ T_{period} is the Duty Cycle, and this is the percentage of the period that the square wave is high (e.g. 3.3.V).

LEDR

For dimming or brightening the LEDR, the persistence of vision of the human eye is what allows the perception of different light intensities of LEDR. When the duty cycle is relatively low, like in the 25% example below, the light intensity would be perceived as dim.



If the duty cycle were higher, like in the 70% example below, the LEDR would be perceived as brighter.



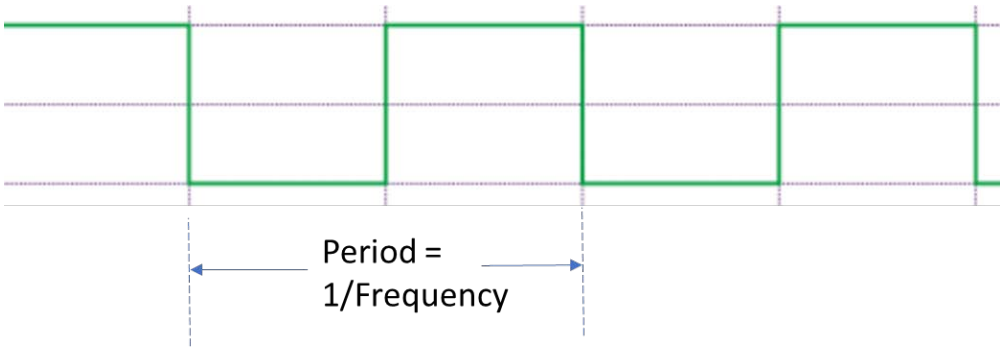
Note that the period of the PWM waveform would need to be low enough so that flickering would not be detected by the eye. In this case, around 20 Hz would be about the lowest frequency before flickering starts to become visible. But with an FPGA, the frequency would typically be much higher in your design.

CAUTION: Depending on the LED wiring of the circuit board, the duty cycle relationship with brightness may be inverted, so you may need to do an inversion in your code. Watch for this behavior.

7-Segment Displays Flashing

In the case of the flashing 7-segment displays, the important features of using PWM will be:

- Modifying the PWM period with distance measured. I.e. the longer the distance, the longer the period (and therefore, a slower flashing rate), and vice versa.
- Preserving the 50% duty cycle of the PWM waveform, so that the flashing of the 7-segment displays is evenly on and off.



Buzzer

In the case of the buzzer, the important features of using PWM will be very similar to the 7-segment displays:

- Modifying the PWM period with distance measured. I.e. the longer the distance, the longer the period (and therefore, a lower frequency sound), and vice versa.
- Preserving the 50% duty cycle of the PWM waveform, but this feature is not quite so critical for the buzzer but a good target.

For both the 7-segment displays and the buzzer, the period must be carefully controlled to suit human perceptions, so careful use of the downcounter module will be very helpful to control the period.

6. Deliverables

The team will upload the following to the D2L Dropbox by **11:59 pm Monday December 6**. You must follow the submission requirements specified in D2L: Content > Labs > Lab Submission Procedure to D2L Dropbox. **No zipped files. Yuja link and also your MP4 uploaded for video presentations.**

1. VHDL code for their project:
    a. RTL code, i.e. the design code, for the complete project.
    b. A testbench for the top_level, demonstrating the system operating in all 3 new modes: dimming LEDR, flashing 7-segment displays, buzzing and showing the hold (i.e. freeze) and Reset behavior. This is going to be tricky because of the greatly differing time scales for the various PWM signals, so be prepared to spend some effort on this task.
2. The .sdc and .qsf files for their project.
3. A Design Record which is a PDF document that contains the following screenshots. Please refer to the Lab 1 Design Record Example document to see the required format and instructions on how to obtain the screenshots.
    a. Your RTL schematic.
    b. Your Slow 1200mV 85C Model Fmax Summary – we want to see the maximum frequency of your design.
    c. Your Messages Window.
    d. ModelSim simulation waveforms for top_level, showing the operations in 1 b.
    e. Note, you do not have to show the useful instructions on how to obtain the screenshots, as shown in the example document. You just have to show the screenshots, the document title, and the student names.
4. Three videos of **no more than 3 minutes each**, delivered by the respective leads. All students in a team must present at least one video. You must feature your face in the video, as you are speaking. The videos must be recorded in "one-take." No video editing, splicing, cutting, speeding up or slowing down, etc. The videos must be uploaded to the D2L Dropbox in MP4 format. You must follow the Lab Submission Procedure to D2L Dropbox, in the Labs folder in D2L. This will allow the video to be played within the D2L Dropbox player and will make it more convenient for the marker and for you. Do not speak too quickly to rush through your presentation and jam more information. Rather, carefully decide how to show the most relevant information and consider this a communication exercise.
    a. <u>Design Lead Video:</u>
        i. Use Quartus and your face must be present throughout the presentation. You can start a Zoom session and share the screen with yourself and this should make your face visible in a small picture.
        ii. Introduce yourself and your role.
        iii. Using Quartus: Explain the design and how it works, starting with an overview of the RTL schematic and dive into the design modules as needed, especially how you achieved the additional functionality required by this lab project. Then explain the RTL code, starting with top_level and explain the lower level modules as needed.

b. Simulation Lead Video:
    i. Use ModelSim and your face must be present throughout the presentation. You can start a Zoom session and share the screen with yourself and this should make your face visible in a small picture.
    ii. Introduce yourself and your role.
    iii. Using ModelSim: Explain the testbench code, starting with tb_top_level and show and explain its simulation waveforms in ModelSim. Be sure to explain how the testbench exercises the design and how the simulation displays the correct functionality of the design (this is the purpose of the testbench). You may use screenshots of the other testbenches, besides tb_top_level. But your video must show you interacting with your tb_top_level simulation to explain it
c. Implementation Lead Video:
    i. Introduce yourself and your role, while looking into the camera, so that your face is visible.
    ii. Focus the camera on your DE10-Lite board and demonstrate the required functionality of the system, while explaining what you are doing and the results you are seeing and how it confirms the required behavior: the system operating in all the required modes:
        1. Distance;
        2. Voltage;
        3. ADC;
        4. LEDR dimming and brightening with distance;
        5. 7-segment displays flashing with distance;
        6. Buzzer buzzing with distance; and
        - Hold behavior; and
        - Reset behavior.

7. Grading Rubric

Lab 4 will be weighted at 42% of the final course grade and it represents a significant design challenge. The grades of the 3 video presentations will be averaged with equal weighting for all the students in the team and rounded to two decimal places.

The Design Record will be used primarily as a reference but a poor-quality Design Record will detract from the presentation grades.

7.1. Presentation Rubric

The video presentations will be assessed on a grade-point scale for a single grade out of 4.00. The grade will be interpreted from the description below.

Grade	Description
3.7 to 4.00 (A- to A)	Excellent: superior performance, showing comprehensive understanding of subject matter. *To earn a grade in this category the submitted work must fully complete and fully meets the project requirements. The work is of very high quality from both the technical and communication perspectives.* ***All requirements must be completed to be eligible for a grade in this category.***
2.70 to 3.30 (B- to B+)	Good: clearly above average performance with knowledge of subject matter generally complete. *The submitted work is complete and meets the project requirements. The work is very high quality but has minor weakness or weaknesses either technically and/or in communications.* ***At least two of the 3.1, 3.2, and 3.3 requirements must be completed to be eligible for a grade in this category. All other requirements must be completed.***
1.70 to 2.30 (C- to C+)	Satisfactory: basic understanding of the subject matter. *Submitted work is complete but has significant weakness or weaknesses either technically and/or in communications. Generally indicates insufficient effort or accomplishment is moderate.* ***At least one of the 3.2 and 3.3 requirements must be completed to be eligible for a grade in this category.***
1.00 to 1.30 (D to D+)	Minimal pass: marginal performance; generally insufficient preparation for subsequent labs or courses in the same subject. *Weak effort demonstrated by missing elements or superficially completed elements either technically and/or in communications.*
0.00 (F)	Fail: unsatisfactory performance or failure to meet course requirements. *Clear lack of effort or ability to accomplish the project requirements.*

Notes: Grade can be reduced down to 0.0 for not complying with requirements or for unprofessional behavior. Excessive video lengths will be penalized one letter grade (e.g. B+ to B) for every 15 second interval overlength of the stated limit.

Late penalty: one letter grade per day late (e.g. A- to B+, not A- to B-), according to the D2L Dropbox timestamp, based on the latest submission for the project. Students are responsible for retaining the D2L Dropbox submission confirmation email and for double-checking their Dropbox submission. Submissions must be fully complete to be eligible for grading of the lab project. This includes code and design files, videos, and Design Record, otherwise the late penalty will apply to the entire lab project.