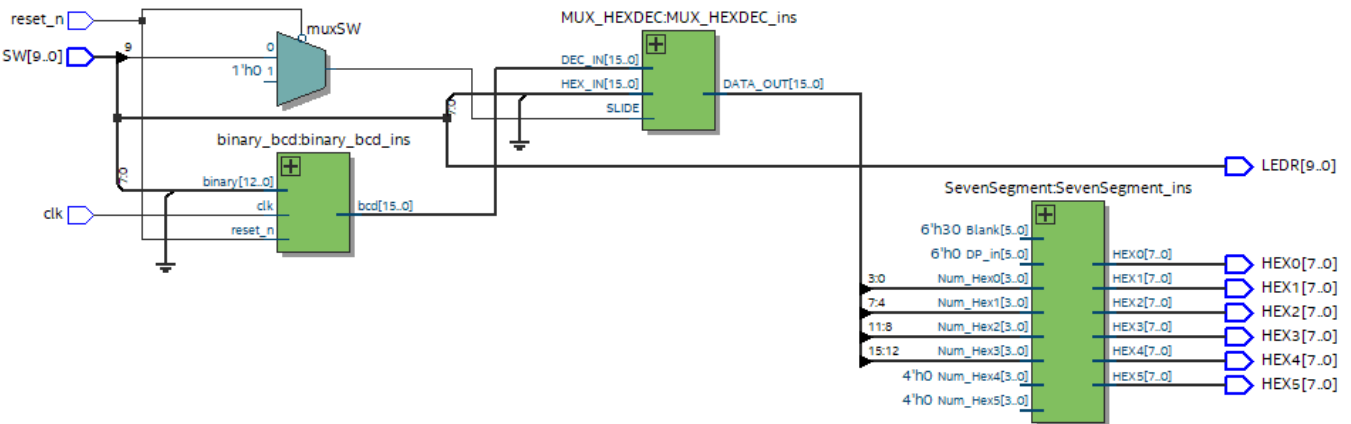


Lab 1 Design Record

Students: Nabeel Amjad, Tahseen Intesar, Michael Tagg



Quartus Prime Lite Edition - S:/QuartusProjects/ENEL453_Group8/lab1/QuartusFiles/Lab1/Group8_Lab1_ENC453 - top_level

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Files top_level.vhd tb_top_level.vhd tb_MUX_HEXDEC.vhd top_level.SDC

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Analysis & Elaboration

Flow Summary

Flow Status: Successful - Sat Oct 03 12:51:38 2020

Quartus Prime Version: 18.1.0 Build 625 09/12/2018 SJ Lite Edition

Revision Name: top_level

Top-level Entity Name: top_level

Family: MAX 10

Device: 10M50DAF484C6GES

Timing Models: Preliminary

Find... Find Next

Type ID Message

- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
- 10492 VHDL Process Statement warning at top_level.vhd(66): signal "sw" is read inside the Process Statement but isn't in the Process Statement's sensitivity list
- 13024 Output pins are stuck at VCC or GND
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
- 292013 Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
- 15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment warnings report for details
- 332174 Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
- 332049 Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
- 332174 Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
- 332049 Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
- 15705 Ignored locations or region assignments to the following nodes
- 334000 Timing characteristics of device 10M50DAF484C6GES are preliminary
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- 171167 Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter compilation Report for more information.
- 169177 12 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V LVTT/LVCMOS I/O systems.
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
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Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	144.28 MHz	144.28 MHz	clk	

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