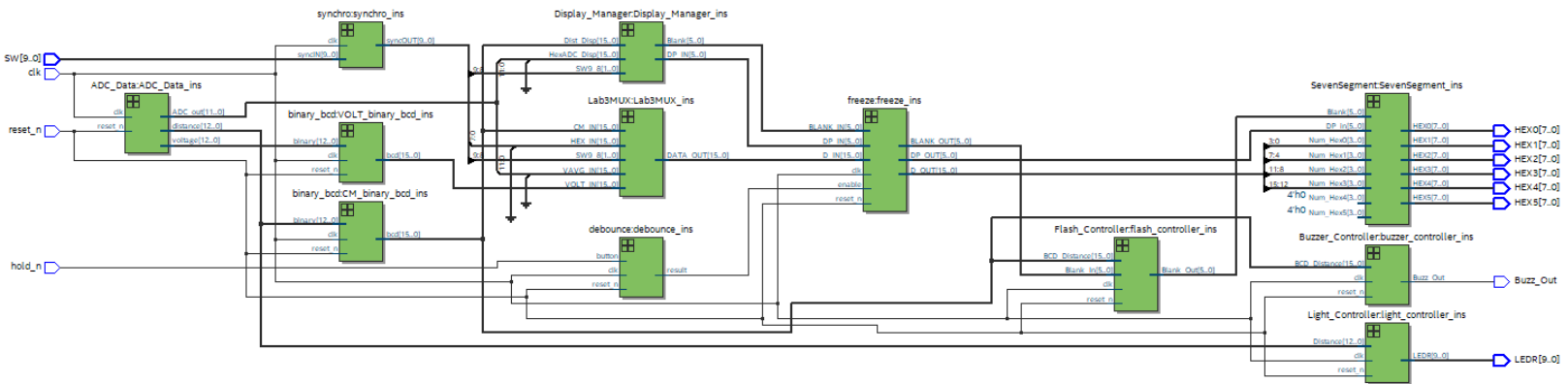


Lab 4 Design Record – Group 8

Students: Nabeel Amjad, Tahseen Intesar, Michael Tagg

RTL Viewer



ERRORMESSAGES

UI window showing error messages. The window has a toolbar with icons for All, Find, and Find Next, and a search bar labeled <<Filter>>. The message list includes:

- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSOR...
- 10036 Verilog HDL or VHDL warning at top_level.vhd(33): object "ADC_raw" assigned a value but never read
- 10036 Verilog HDL or VHDL warning at ADC_Conversion.v(98): object "cur_adc_ch" assigned a value but never read
- 10036 Verilog HDL or VHDL warning at ADC_Conversion.v(99): object "adc_sample_data" assigned a value but never read
- 10036 Verilog HDL or VHDL warning at altera_modular_adc_control_fsm.v(70): object "sync_ctrl_state_nxt" assigned a value but never read
- 10540 VHDL Signal Declaration warning at Flash_Controller.vhd(21): used explicit default value for signal "duty_cycle" because signal was never assigned
- 10540 VHDL Signal Declaration warning at Buzzer_Controller.vhd(18): used explicit default value for signal "duty_cycle" because signal was never assigned
- 10540 VHDL Signal Declaration warning at Buzzer_Controller.vhd(21): used explicit default value for signal "en" because signal was never assigned
- 14284 Synthesized away the following node(s):
- 12241 1 hierarchies have connectivity warnings - see the Connectivity checks report folder
- 13024 Output pins are stuck at VCC or GND
- 18061 Ignored Power-Up Level option on the following registers
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSOR...
- 292013 Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
- 15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment warnings report for details
- 332174 Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
- 332049 Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
- 332174 Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
- 332049 Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
- 15705 Ignored locations or region assignments to the following nodes
- 334000 Timing characteristics of device 10M50DAF484C6GES are preliminary
- 334000 Timing characteristics of device 10M50DAF484C6GES are preliminary
- 171167 Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.
- 169177 13 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V interfaces. For more information, refer to AN 447: Interfacing MAX 10 Devices to 3.3V, 3.0V, and 2.5V I/O Standards
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSOR...
- 12914 The file, S:/QuartusProjects/ENEL453_Group8/lab4/adc_qsys.sopcinfo, is not embedded into sof file as expected. Some tools, such as System C, require the file to be embedded.
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSOR...
- 332174 Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
- 332049 Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
- 332174 Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
- 332049 Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
- 334000 Timing characteristics of device 10M50DAF484C6GES are preliminary
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSOR...
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TIMING@85C

UI window showing timing summary. The window has tabs for Flash_Controller.vhd, Buzzer_Controller.vhd, and Compilation Report - top_level. The title bar is Slow 1200mV 85C Model Fmax Summary. The table below shows the timing summary:

	Fmax	Restricted Fmax	Clock Name
1	75.51 MHz	75.51 MHz	clk
2	172.53 MHz	172.53 MHz	ADC_Data_ins ADC_ins ADC_Conversion_ins u0 altpll_sys sd1 pll7 clk[0]

SIMULATIONS

tb_top_level.vhd

