

# Matthew Tan

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in matthew-tan-canada

## Languages and Other Software

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- C
- C++
- Python
- Verilog
- Docker
- Git
- Linux
- Jira

## Hardware Skills

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### Lab Test Equipment

Oscilloscopes, Multimeters, Power Supplies

### Soldering and Board Rework

### Hardware Design and Debugging

## Skills

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- Quick Learner
- Adaptability
- Problem Solving
- Communication
- Project Management and Teamwork

## Education

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### University of Waterloo,

*Computer Engineering*

09/2019 – present | Waterloo, Canada

3.9 GPA

Embedded Microprocessor Systems

Algorithms and Data Structures

Systems Programming and Concurrency

Computer Architecture

Operating Systems

## Professional Experience

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### Sibros, *Firmware Engineering Intern*

05/2023 – present | San Jose, USA

- Developed several C modules for vehicle electronic control units to support over-the-air updates.
- Developed a C++ module to use Google's protobuf text format for our executables' config files, to allow automatic generation of classes and APIs based on a defined proto file.
- Collaborated with team members to reduce the complexity of different code modules and remove repetitive code
- Designed Python integration tests for updater executables that reduced testing time by 60%.

### Splunk, *Software Engineering in Test Intern*

01/2023 – 04/2023 | San Jose, USA

- Containerized data generation services to be easily deployed and developed Python scripts for end-to-end testing of the service deployment.
- Developed Gitlab CI/CD pipelines to build, test, and upload our docker images to Artifactory and deploy the images to production servers within 15 minutes.

### onsemi, *Hardware and Systems Developer*

05/2022 – 08/2022 | Waterloo, Canada

- Developed toolchains to build embedded projects in different IDEs with multiple options and optimizations.
- Programmed C firmware tests, such as I2C and SPI tests, and used behavior-driven development modules in Python to reduce the amount of manual testing by 40%.
- Tested C firmware issues on a hardware development board, and debugged them by stepping in C/Assembly and using an oscilloscope.

## Projects

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### RISC-V Core Implementation, *Verilog*

- Implemented and simulated a single-issue RISC-V core with a 5-stage pipeline and support for instruction bypassing using Verilog.