10-GHz Clock Recovery Using an Optoelectronic Phase-Locked Loop Based on Three-Wave Mixing in Periodically Poled Lithium Niobate

Fausto Gómez Agis, Cédric Ware, Didier Erasme, Raimund Ricken, Viktor Quiring, and Wolfgang Sohler

***Abstract*—Clock recovery is a critical function of any digital communications system. To replace the classical electronic phase-locked loops (PLLs) at higher bit rates, several all-optical or optoelectronic clock recovery methods are being studied. This letter presents an optoelectronic PLL where three-wave mixing in a periodically poled lithium niobate (PPLN) device provides the phase comparator. Since PPLN is passive, it generates no amplified spontaneous emission noise; also, the error signal is in the visible (763 nm), therefore easily separated from infrared input signals. Clock recovery is performed on a 10-GHz sinusoidal optical signal. Being based on ultrafast nonlinear effects, this scheme should be able to reach still higher bit rates, on the order of several hundred gigahertz. Also, subclock extraction (e.g., 40-to-10 GHz) should be possible without modifications.**

***Index Terms*—Clock recovery, optical signal processing, periodically poled lithium niobate (PPLN), phase-locked loops (PLLs), three-wave mixing (TWM).**

I. Introduction

CLOCK recovery is a critical function of any digital communications system, required for receiving and possibly regenerating the signal. It is traditionally performed by an electronic phase-locked loop (PLL); however, to process optical signals at higher bit rates, electronic devices become a bottleneck.

Therefore, numerous all-optical or optoelectronic clock recovery methods are being researched, notably optoelectronic PLLs, which use the same basic scheme, replacing the up-front mixer or phase comparator by a nonlinear optical device. Systems using four-wave mixing or cross-phase modulation in semiconductor optical amplifiers [1]–[3] or electroabsorption modulators [4] have been previously demonstrated.

In this letter, we present an optoelectronic PLL where three-wave mixing (TWM) in a periodically poled lithium niobate (PPLN) device provides the phase comparator operation. Since PPLN is passive, it generates no amplified spontaneous emission noise; in addition, the error signal is in the visible range (763 nm), therefore easily separated from the infrared input signals by a silicon photodetector. To our knowledge, it is the first demonstration of the use of PPLN for clock recovery.

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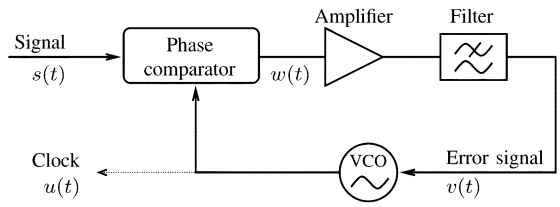

Fig. 1. PLL basic scheme.

After a brief reminder of current clock recovery methods and PLL principles, our setup is described. An analysis is then proposed, which agrees with our preliminary results [5] as well as new experimental results: phase comparison using TWM in PPLN, and successful clock recovery from a 10-GHz sinusoidal optical signal.

II. General PLL Principles

The PLL basic scheme is illustrated in Fig. 1. The clock $u(t)$ is generated by a voltage-controlled oscillator (VCO), driven by $v(t)$, which results from filtering and amplifying the output $w(t)$ of a phase comparator, which in turn measures the phase difference between said clock $u(t)$ and the input signal $s(t)$.

Supposing that the input and clock signal are sinusoidal, and that the phase comparator has a sinusoidal response, these signals can be modelled as [6]

$$s(t) = S_0 \sin(\omega_s t + \varphi_s(t)) \tag{1a}$$

$$u(t) = U_0 \cos(\omega_o t + \varphi_o(t)) \tag{1b}$$

$$w(t) = K_1 \sin[(\omega_s - \omega_o)\, t + \varphi_s(t) - \varphi_o(t)] \tag{1c}$$

$$v(t) = K_2\, [w * f](t) \tag{1d}$$

$$\frac{d\varphi_o}{dt} = K_3\, v(t) \tag{1e}$$

where K_1 is the phase comparator's sensitivity, K_2 the amplifier's gain, f the filter's impulse response (possibly including a time delay to account for the loop length), and ω_o and K_3 the VCO's natural frequency and sensitivity. The *loop gain* is defined as $K = K_1 K_2 K_3$.

The PLL's behavior depends on the loop gain and the filter's response. A full analysis is outside the scope of this letter, but two basic results can be used:

- if the loop filter does not include an integrator, the maximum lock bandwidth is twice the loop gain;
- the longer the loop and the higher its gain, the less stable the loop is.

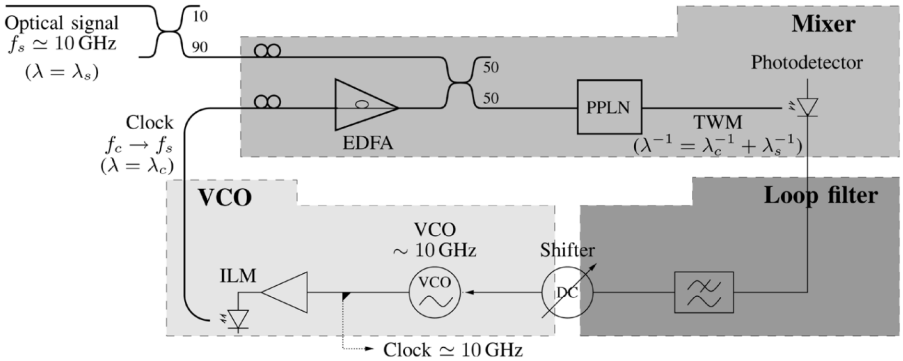

Fig. 2. Optoelectronic PLL basic scheme. Illustrates the three basic PLL blocks (VCO, mixer, and filter): The "VCO" includes an integrated laser and modulator, making its output an optical pulse train; the "mixer" is based on TWM in the PPLN, detected by a silicon photodetector; the "filter" includes a voltage shifter so as to tune the VCO's operating point.

III. Optoelectronic PLL Setup

The clock recovery system is described in Fig. 2. The three basic blocks of a PLL can be recognized: VCO, mixer, and loop filter.

The VCO is a standard electronic oscillator. Its operating point is tuned by a dc voltage shifter. Its output drives the electroabsorption modulator of an integrated laser and modulator (ILM) at $\lambda_c \simeq 1550$ nm. Thus one has an optical signal, modulated at a frequency $f_c \simeq 10$ GHz, amplified by an erbium-doped fiber amplifier (EDFA). This forms the *clock signal*.

The clock signal is coupled into a 3-dB coupler along with the input signal. The latter is produced by a tunable laser set at $\lambda_s \simeq 1502$ nm so as to match the wavelength where the PPLN performs a sum-frequency generation: $[\lambda_c^{-1} + \lambda_s^{-1}]^{-1} = 763\text{ nm} = 1526\text{ nm}/2$. That beam is sinusoidally modulated at $f_s \simeq 10$ GHz by an external modulator.

Upon injection into the PPLN, these signals generate a TWM beam at 763 nm, detected by a silicon avalanche photodetector, insensitive to the infrared input signals which would otherwise blind it. This *error signal's* envelope depends on the input and clock signals' intercorrelation—in the same way as in an optical autocorrelator.

If the modulation frequencies f_s and f_c are not equal, the photodetector output signal bears a low-frequency component at $|f_s - f_c|$. (Other components, at the sum frequency, are filtered out by the photodetector, whose bandwidth is only a few tens of megahertz.)

On the other hand, if the PLL is locked in $f_s = f_c$ (or even $f_s = N \times f_c$ for subclock recovery), the error signal is constant, and its level depends on the delay between the input and clock pulse trains. This behavior, therefore, mimics that of an electrical mixer, which can act as a phase comparator.

This comparator's output is low-pass filtered and shifted, then drives the VCO, which closes the loop.

IV. Experimental Results

A. Phase Comparator Using TWM

The operation of the PPLN as a phase comparator is demonstrated by injecting two 10-GHz sinusoidally modulated optical signals into it. Both signals are driven by the same synthesizer so as to be synchronous, and a delay line is used to create a phase difference between them. The equation which describes the operation of the PPLN as phase comparator for sinusoidal inputs is

$$P_{\text{TWM}} = P_0 + K_0 \sin\varphi. \tag{2}$$

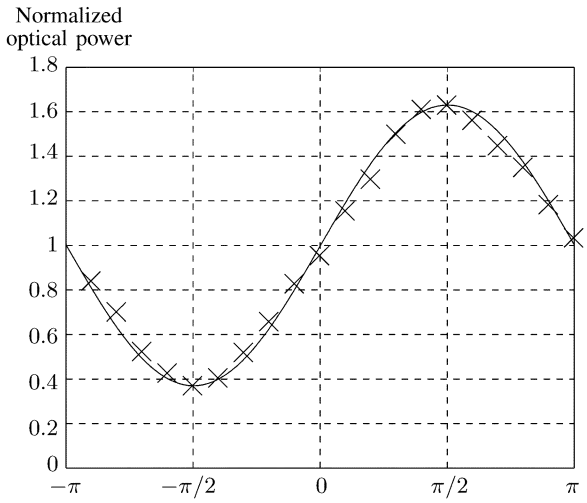

Fig. 3. TWM error signal for two 10-GHz sinusoidal signals as a function of the time delay between them.

Fig. 3 shows the optical power of the resulting TWM beam as a function of this phase offset.

In the clock recovery experiment, we estimate $P_0 = 12.00$ nW and $K_0 = 7.56$ nW from the TWM beam power. Associated with a photodetector sensitivity $\mathcal{R} = 7.66 \cdot 10^4$ V/W, this yields a phase comparator sensitivity $K_1 = \mathcal{R} \times K_0 \simeq 5.790 \cdot 10^{-4}$ V; with $K_2 = 1$ and $K_3 = 10^7$ Hz/V, we have a total loop gain $K \simeq 5,790$ Hz.

B. Clock Recovery

Clock was successfully recovered on a 10-GHz sinusoidal optical signal. Fig. 4(a) and (b) shows a sampling oscilloscope

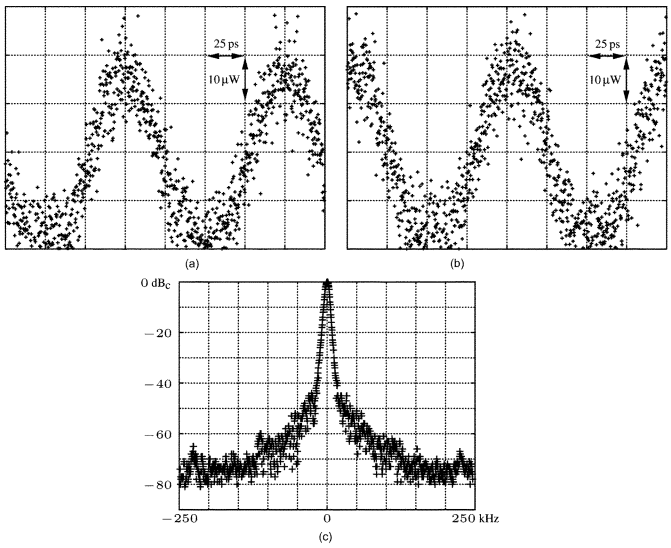

Fig. 4. Recovered clock and signal. (a) Input signal, triggered by generator. (b) Input signal, triggered by recovered clock. (c) Recovered clock spectrum around 10 GHz.

trace of the input signal triggered, respectively, by the synthesizer clock and the recovered clock. The latter clock's spectrum is shown Fig. 4(c).

The PLL is locked in; the electrical clock jitter can be estimated at 6.6 ps by integragting the pedestal on Fig. 4(c) as specified in [7]; and the tracking bandwidth varies between 6 and 11 kHz, which is of the order of the loop gain determined in Section IV-A.

Another experiment with $K_0 = 13.67$ nW gives a total loop gain $K \simeq 10,470$ Hz and a tracking bandwidth between 12 and 16 kHz, which also shows an agreement between theory and experiment.

It is to be noted that in order to bring the loop's gain to a useful value, we used an EDFA to amplify the beam at 1550 nm, which for reasons of source availability had to be the clock signal; using different wavelengths, or a PPLN sample with a higher frequency doubling wavelength, would allow the EDFA to be placed outside the loop, decreasing its length, thus improving its stability. The loop length could be minimized further by integrating the phase comparator onto an optical circuit.

Clock recovery of a data-modulated signal has not yet been attempted, but earlier SOA-based experiments [3] indicate that this setup should withstand pseudorandom binary sequence ON–OFF keying modulation of the input signal. The loop filter bandwidth being small compared to the clock frequency, the same loop gain would be achieved for the same *average* input power (requiring twice as much power in the 1's if half the bits are 0's). Likewise, resistance to a long string of zeros would be determined by the loop filter's response time.

V. Conclusion

We have demonstrated an optoelectronic PLL based on TWM in PPLN. This device successfully recovers clock from a 10-GHz sinusoidal signal.

This scheme being based on ultrafast nonlinear effects, it should be able to reach still higher bit rates, on the order of several hundred gigabits per second. Also, as noted in Section III, the TWM-based phase comparator operates as well if the signal frequency is a multiple of the clock frequency; therefore, we anticipate this scheme to be capable of subclock extraction (e.g., 40-to-10 GHz), without modifications. The corresponding experiments remain to be done.

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References

[1] O. Kamatani and S. Kawanishi, "Ultrahigh-speed clock recovery with phase lock loop based on four-wave mixing in a traveling-wave laser diode amplifier," *J. Lightw. Technol.*, vol. 14, no. 8, pp. 1757–1767, Aug. 1996.

[2] L. K. Oxenløwe, P. Jeppesen, D. Zibar, M. Galili, A. T. Clausen, and L. J. Christiansen, "Clock recovery for 320 Gb/s OTDM data using filtering-assisted XPM in an SOA," in *CLEO/Eur.*, Munich, Germany, Jun. 2005, Paper CI3-4-MON.

[3] C. Ware and D. Erasme, "30 GHz sub-clock recovery using an opto-electronic phase-locked loop based on four-wave mixing in a semiconductor optical amplifier," in *CLEO/Eur.*, Munich, Germany, Jun. 2005, Paper CI3-5-MON.

[4] C. Boerner, V. Marembert, S. Ferber, C. Schubert, C. Schmidt-Langhorst, R. Ludwig, and H. Weber, "320 Gbit/s clock recovery with electro-optical PLL using a bidirectionally operated electroabsorption modulator as phase comparator," in *OFC*, Anaheim, CA, Mar. 2005, vol. 2, Paper CI3-4-MON.

[5] F. G. Agis, C. Ware, D. Erasme, R. Ricken, V. Quiring, and W. Sohler, "10 GHz clock recovery using an opto-electronic phase-locked loop based on three-wave mixing in periodically-poled lithium niobate," in *CLEO*, Long Beach, CA, May 2006, Paper JWB34.

[6] A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York: Wiley, 1976.

[7] J. Rutman, "Characterization of phase and frequency instabilities in precision frequency sources: Fifteen years of progress," *Proc. IEEE*, vol. 66, no. 9, pp. 1048–1075, Sep. 1978.