Enclustra User Schematics

Mercury XU1 Revision 4.1

Disclaimer

User schematics do not include proprietary Enclustra design elements, such as power supply circuits.
These circuits use optimized designs which are extremely compact and remain proprietary to Enclustra.
The user manual provides all necessary information to use the module and its interfaces.

User schematics are provided after purchase of Enclustra hardware, and may also be provided in certain cases before purchase, to assist in product evaluation.
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Full schematics, including a full bill-of-materials, may be available through the purchase of a hardware licence for the product in question.
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Note: DNE = Do Not Equip (parts not equipped by default)

Mercury+ XU1 SoC Module

Revision 4.1

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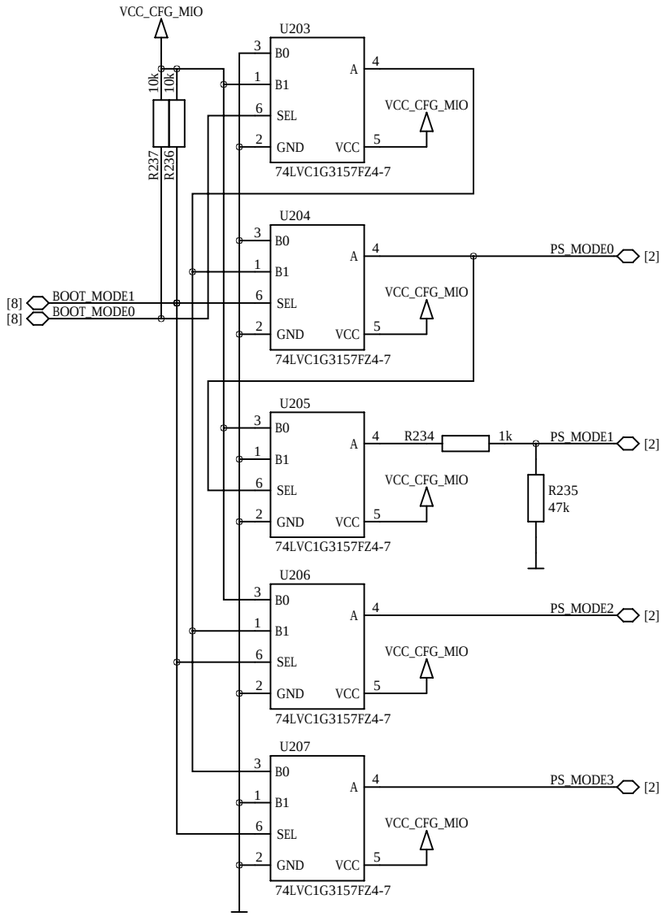
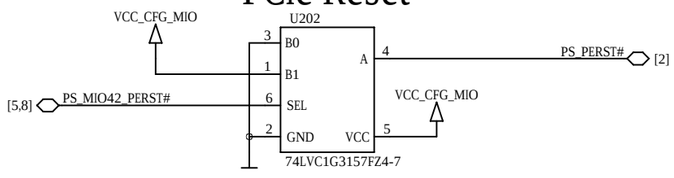
Company	Enclustra FPGA Solution Center	Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 1 / 22

Boot Mode Selection



PCIe Reset



IO / MGT Selection

[3]	MGT_B128_REFCLK0_F25_P	R207-A	0R	MGT_SEL	IO_B66_Y10_B128_REFCLK0_F25_P	[9]
[3]	MGT_B128_REFCLK0_F26_N	R207-B	0R	MGT_SEL	IO_B66_N11_B128_REFCLK0_F26_N	[9]
[3]	IO_B66_Y10	R208-B	0R	#MGT_SEL#		
[4]	IO_B66_N11	R208-A	0R	#MGT_SEL#		
[3]	MGT_B128_REFCLK1_D25_P	R209-A	0R	MGT_SEL	IO_B65_AE7_B128_REFCLK1_D25_P	[9]
[3]	MGT_B128_REFCLK1_D26_N	R209-B	0R	MGT_SEL	IO_B65_AE1_B128_REFCLK1_D26_N	[9]
[3]	IO_B65_AE7	R210-B	0R	#MGT_SEL#		
[4]	IO_B65_AE1	R210-A	0R	#MGT_SEL#		
[3]	MGT_B128_RX0_H29_P	R211-A	0R	MGT_SEL	IO_B65_L5_AD14_AA12_B128_RX0_H29_P	[9]
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[4]	IO_B65_L5_AD14_AA12_P	R212-B	0R	#MGT_SEL#		
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[3]	MGT_B128_RX1_F30_N	R213-B	0R	MGT_SEL	IO_B65_L4_AD7_AD11_B128_RX1_F30_N	[9]
[4]	IO_B65_L4_AD7_AC11_P	R214-B	0R	#MGT_SEL#		
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[4]	IO_B65_L11_GC_AC7_P	R216-B	0R	#MGT_SEL#		
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[4]	IO_B65_L3_AD15_AD12_P	R218-B	0R	#MGT_SEL#		
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[4]	IO_B66_L5_AD14_U2_P	R220-B	0R	#MGT_SEL#		
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[3]	MGT_B128_TX1_E27_P	R221-A	0R	MGT_SEL	IO_B66_L4_AD7_V2_B128_TX1_E27_P	[9]
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[3]	MGT_B128_TX3_A27_P	R225-A	0R	MGT_SEL	IO_B66_L11_GC_V7_B128_TX3_A27_P	[9]
[3]	MGT_B128_TX3_A28_N	R225-B	0R	MGT_SEL	IO_B66_L11_GC_V6_B128_TX3_A28_N	[9]
[4]	IO_B66_L11_GC_V7_P	R226-B	0R	#MGT_SEL#		
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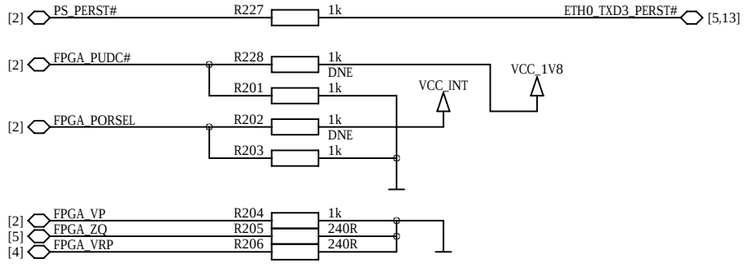
Miscellaneous

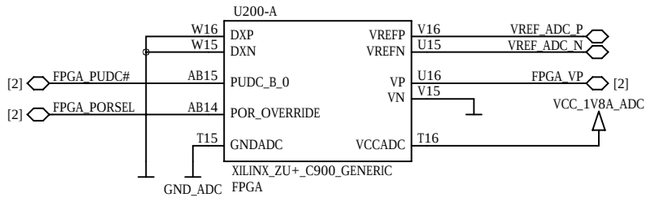


Boot Modes

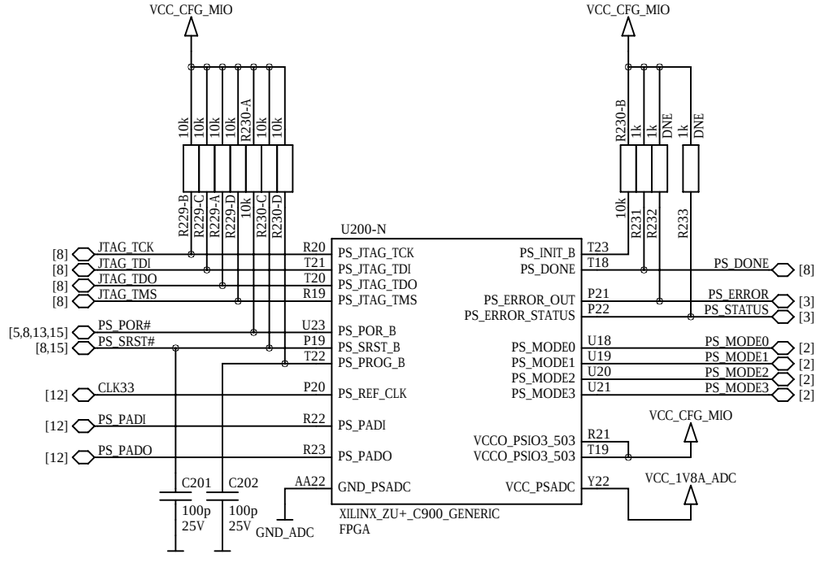
	Boot Mode		Mode Straps	Configuration	
	1	0	PS_MODE	PL Boot	PS Boot
eMMC Mode	0	0	0110	PS	eMMC
SD Mode LS (not supported)	0	1	1110	PS	SDIO (with level shifter)
QSPI Mode	1	0	0010	PS	QSPI
SD Mode (default)	1	1	0101	PS	SDIO
JTAG Mode (*)	1	0	0000	PS	JTAG

SD Mode LS mode may be supported in the future.
SD Mode LS requires VCC_CFG_MIO of 1.8V.
(*) Short-circuit R235 to enable JTAG mode

FPGA Configuration



FPGA PS Configuration



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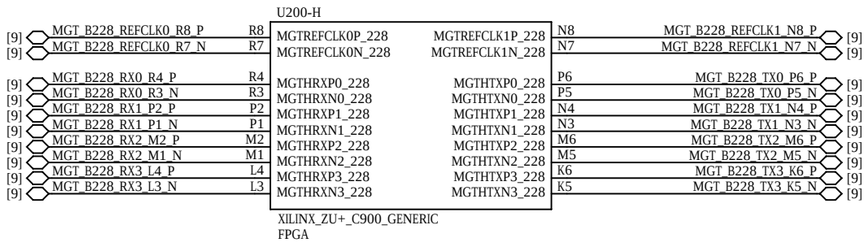
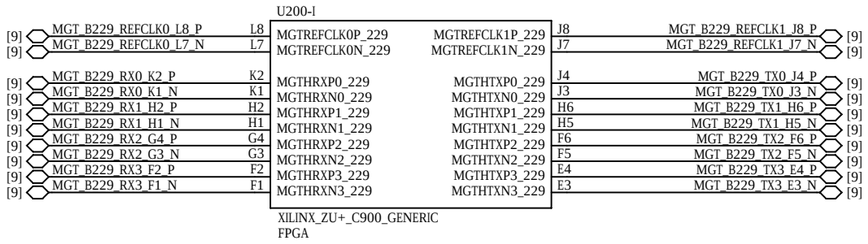
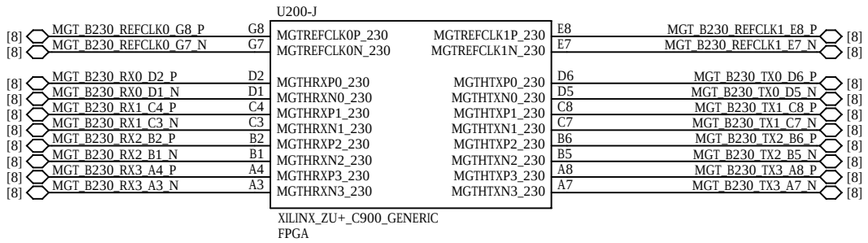
FPGA MGT Bank 228



FPGA MGT Bank 229

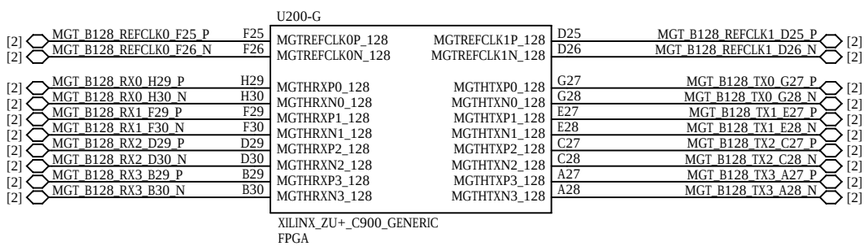


FPGA MGT Bank 230

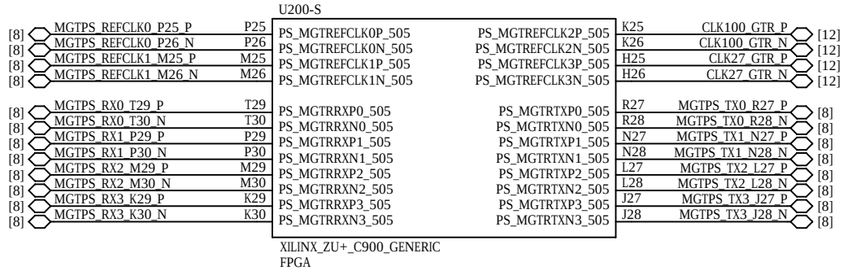


FPGA MGT Bank 128

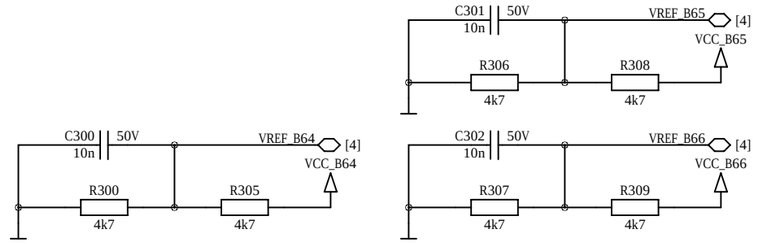
optional via MGT_SEL



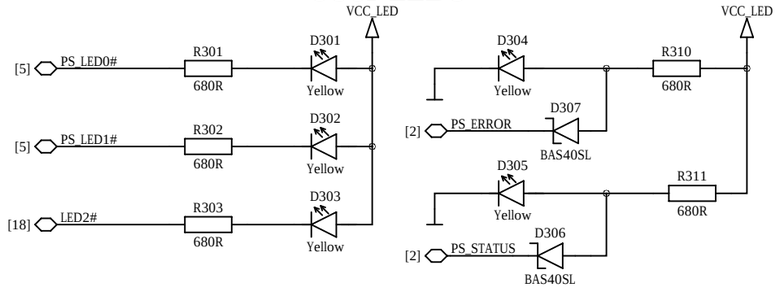
FPGA PS GTR Bank 505



FPGA Reference Voltages



User LEDs



LED Power

not included in user schematics

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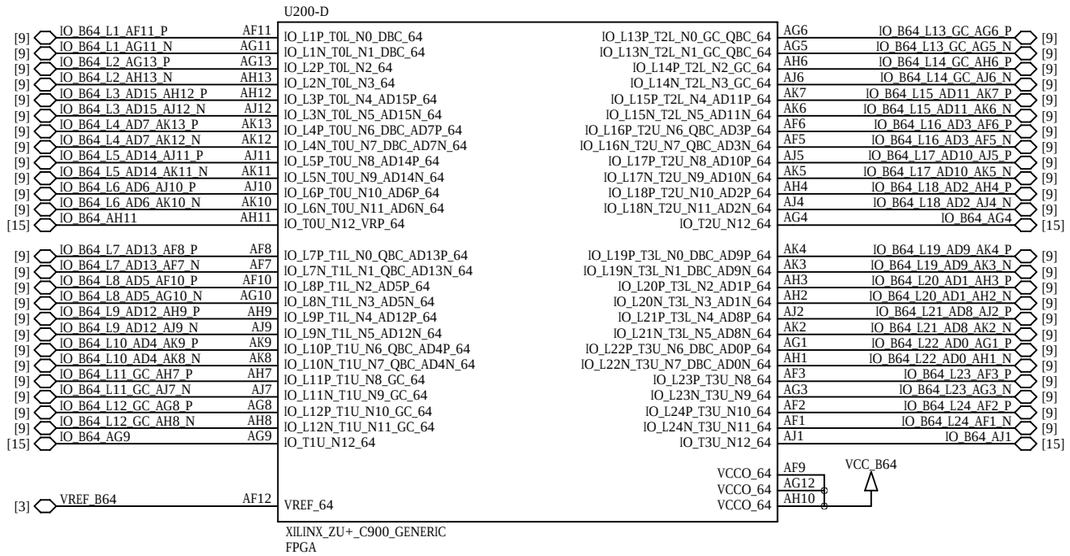
Sheet Name	03_FPGA_MGT_BANKS_LEDS	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 3 / 22

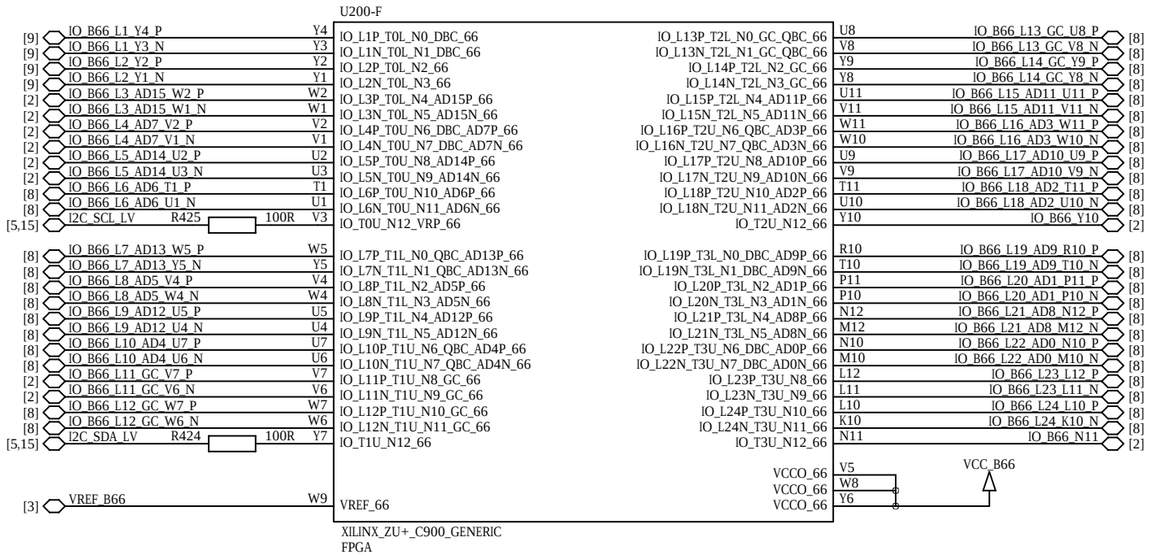
FPGA HP Bank 64

VCCO = VCC_IO_B64 (max 1.8V)



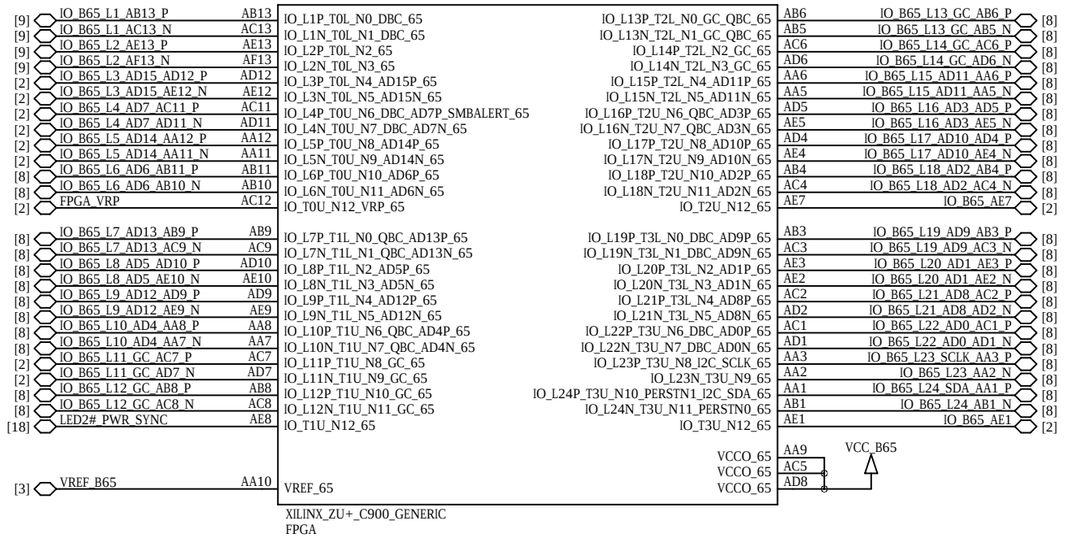
FPGA HP Bank 66

VCCO = VCC_IO_B66 (max 1.8V)



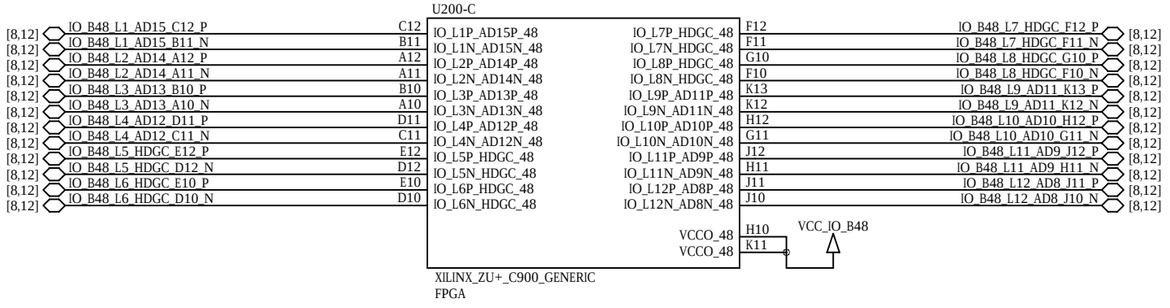
FPGA HP Bank 65

VCCO = VCC_IO_B65 (max 1.8V)



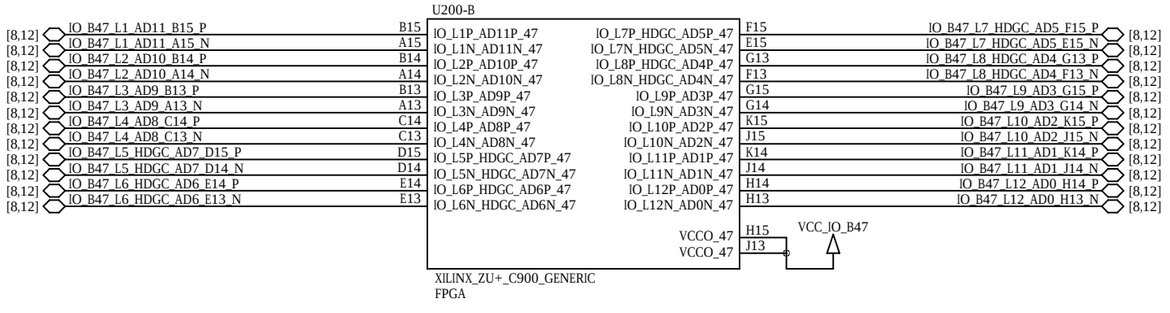
FPGA HD Bank 48

VCCO = VCC_IO_B48 (max 3.3V)



FPGA HD Bank 47

VCCO = VCC_IO_B47 (max 3.3V)



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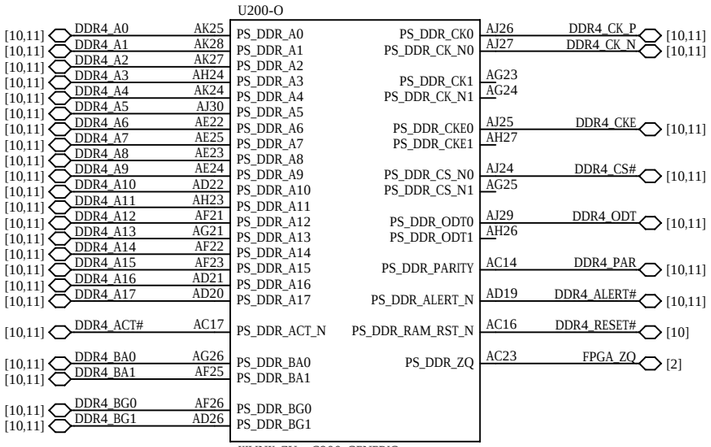
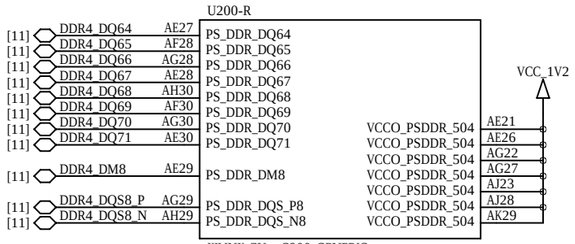
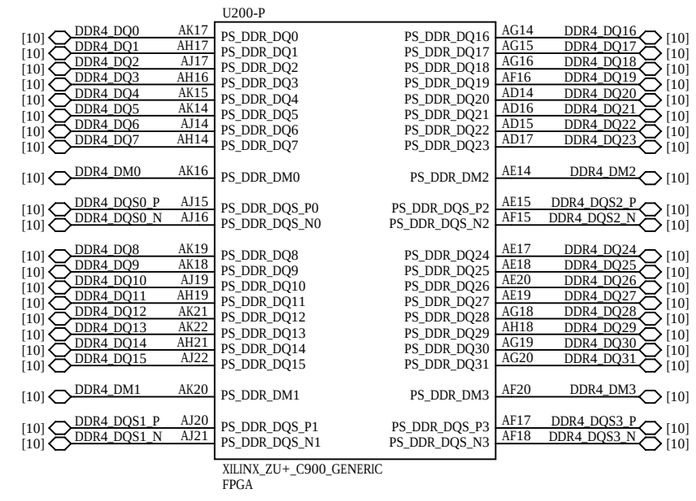
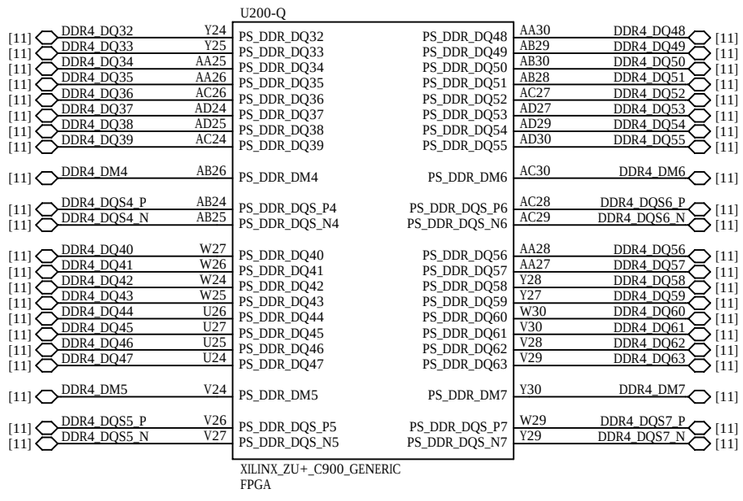
FPGA PS DDR Bank 504

VCCO = VCC_1V2



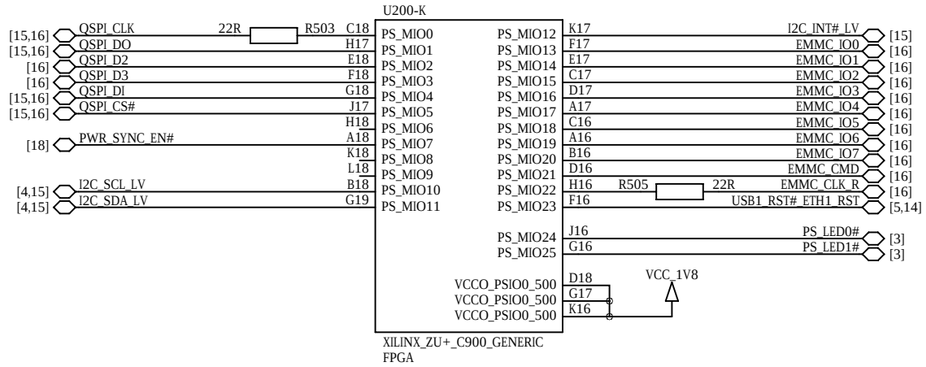






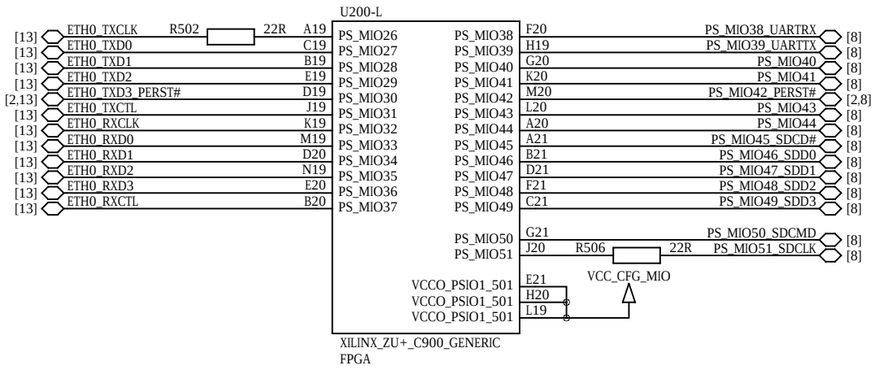
FPGA PS Bank 500

VCCO = VCC_1V8



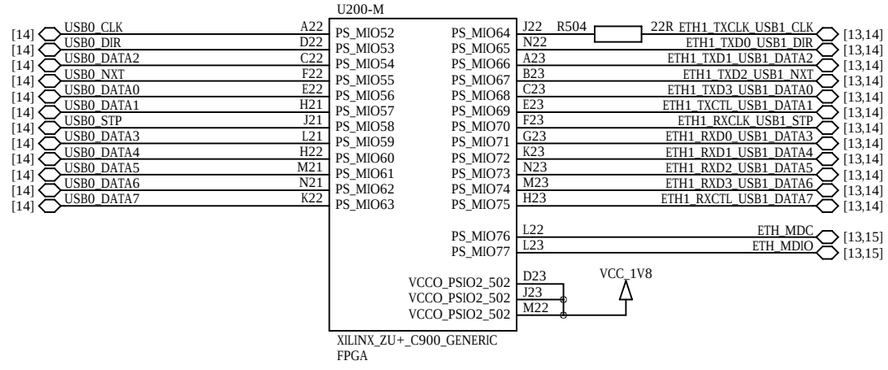
FPGA PS Bank 501

VCCO = VCC_CFG_MIO



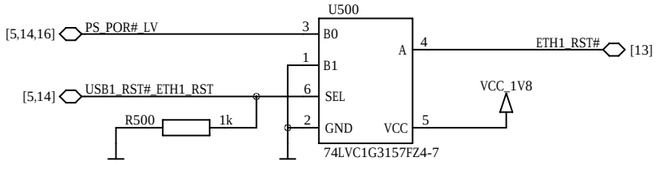
FPGA PS Bank 502

VCCO = VCC_1V8

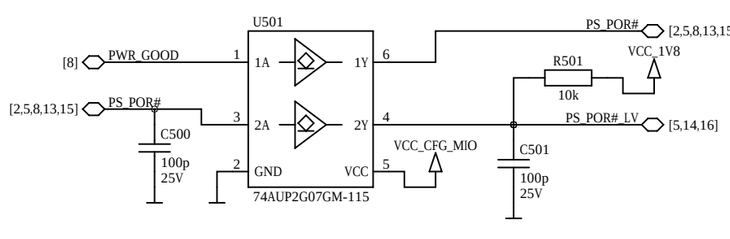


USB1/ETH1 Selection

default is ETH1 enabled, USB1 in reset



Reset Circuit



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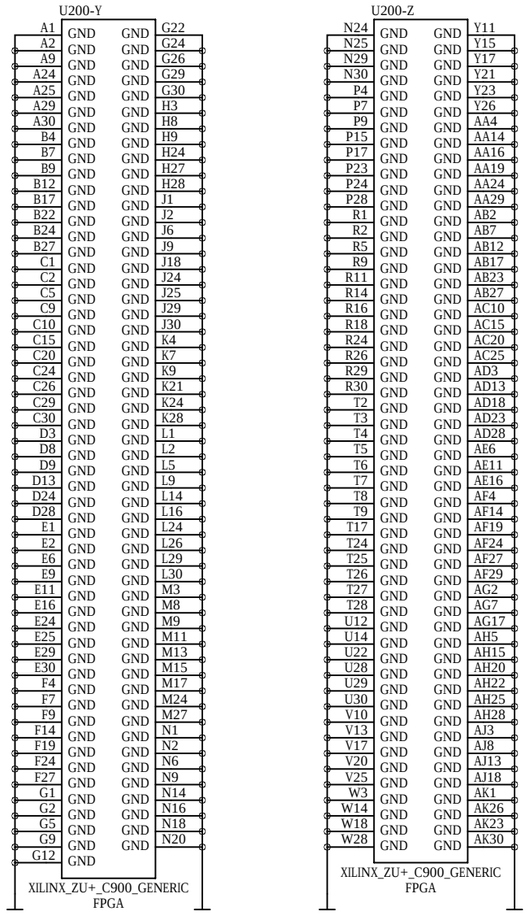
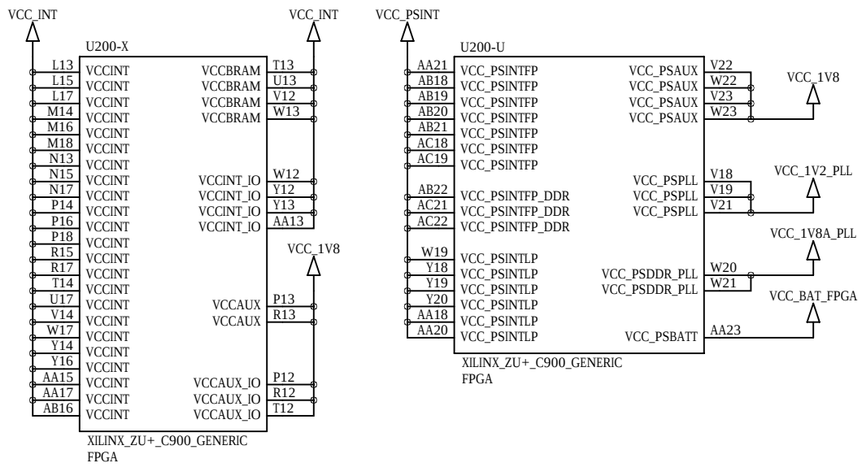
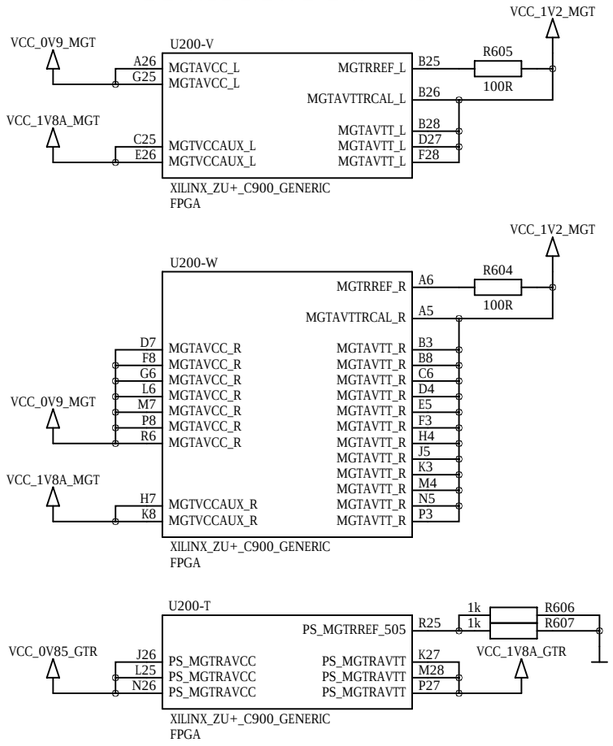
FPGA Ground



FPGA Power



FPGA MGT Power



MGT Power Filters

not included in user schematics

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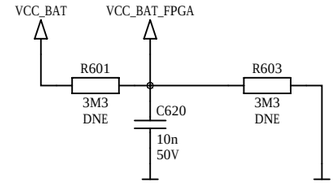
FPGA Battery Voltage



ADC Power

not included in user schematics

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ADC Reference

not included in user schematics

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PLL and GTR Power Filters

not included in user schematics

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FPGA Decoupling

not included in user schematics

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Power Decoupling

not included in user schematics

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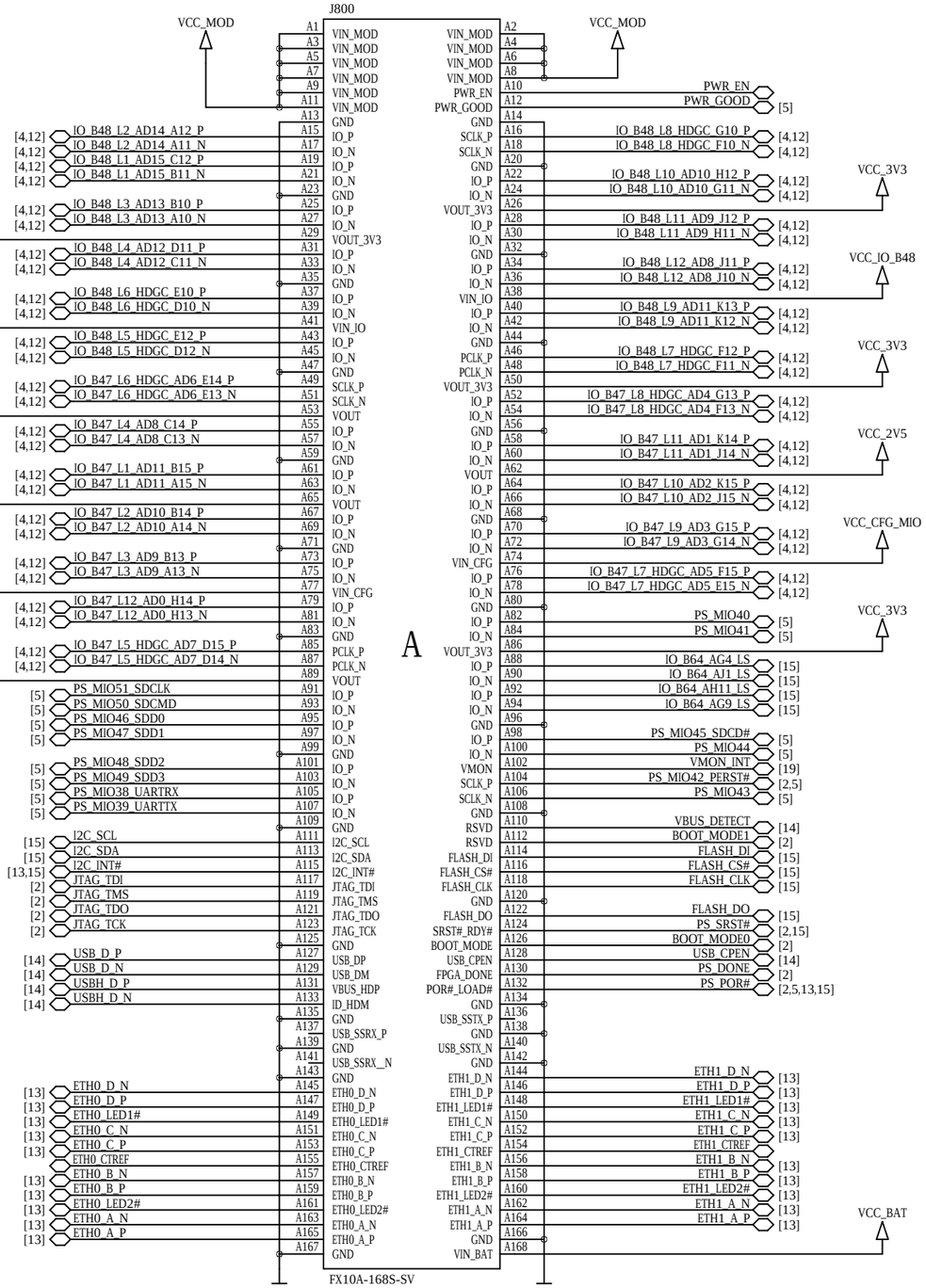
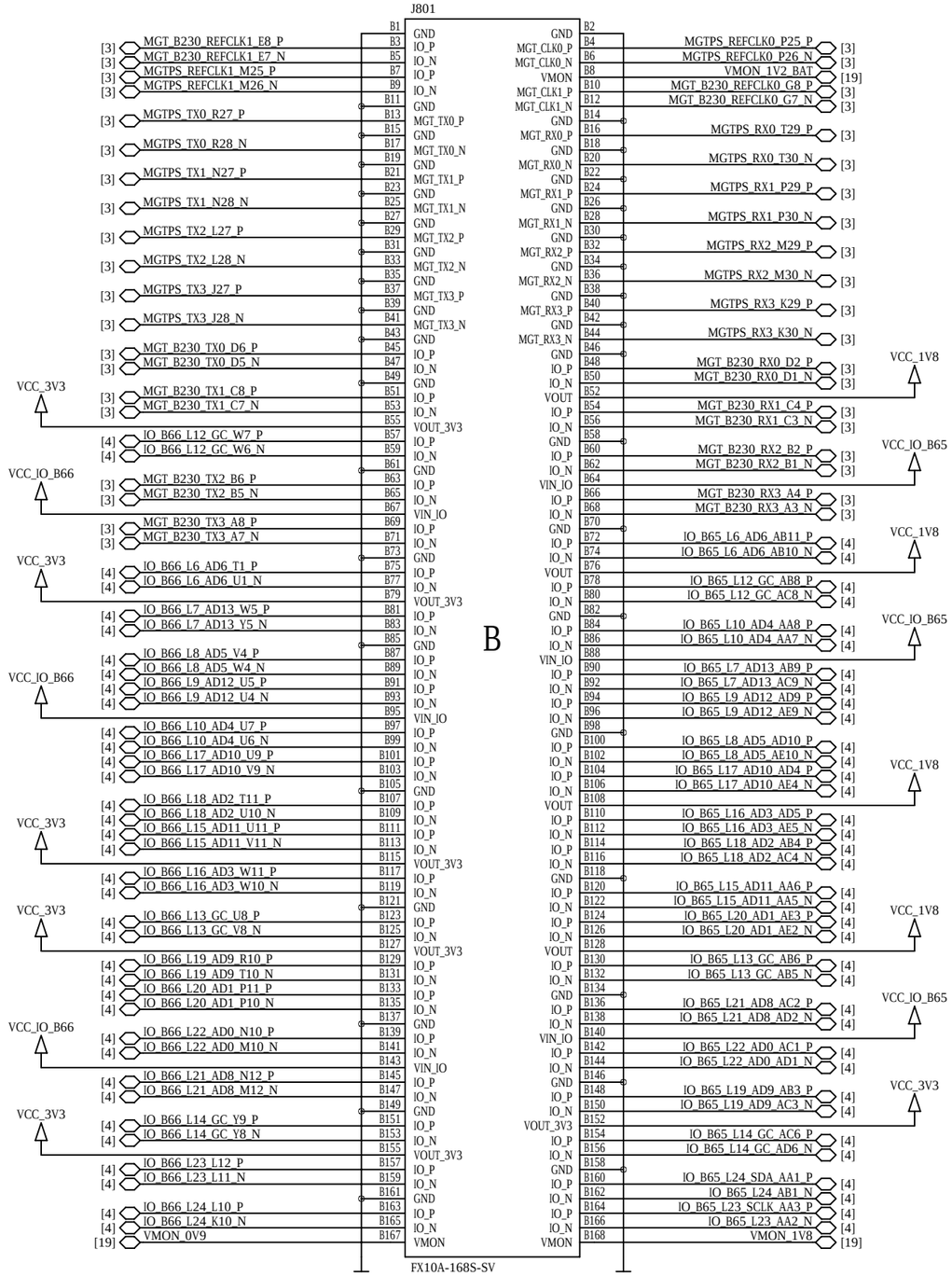
Module Connector A



Module Connector B



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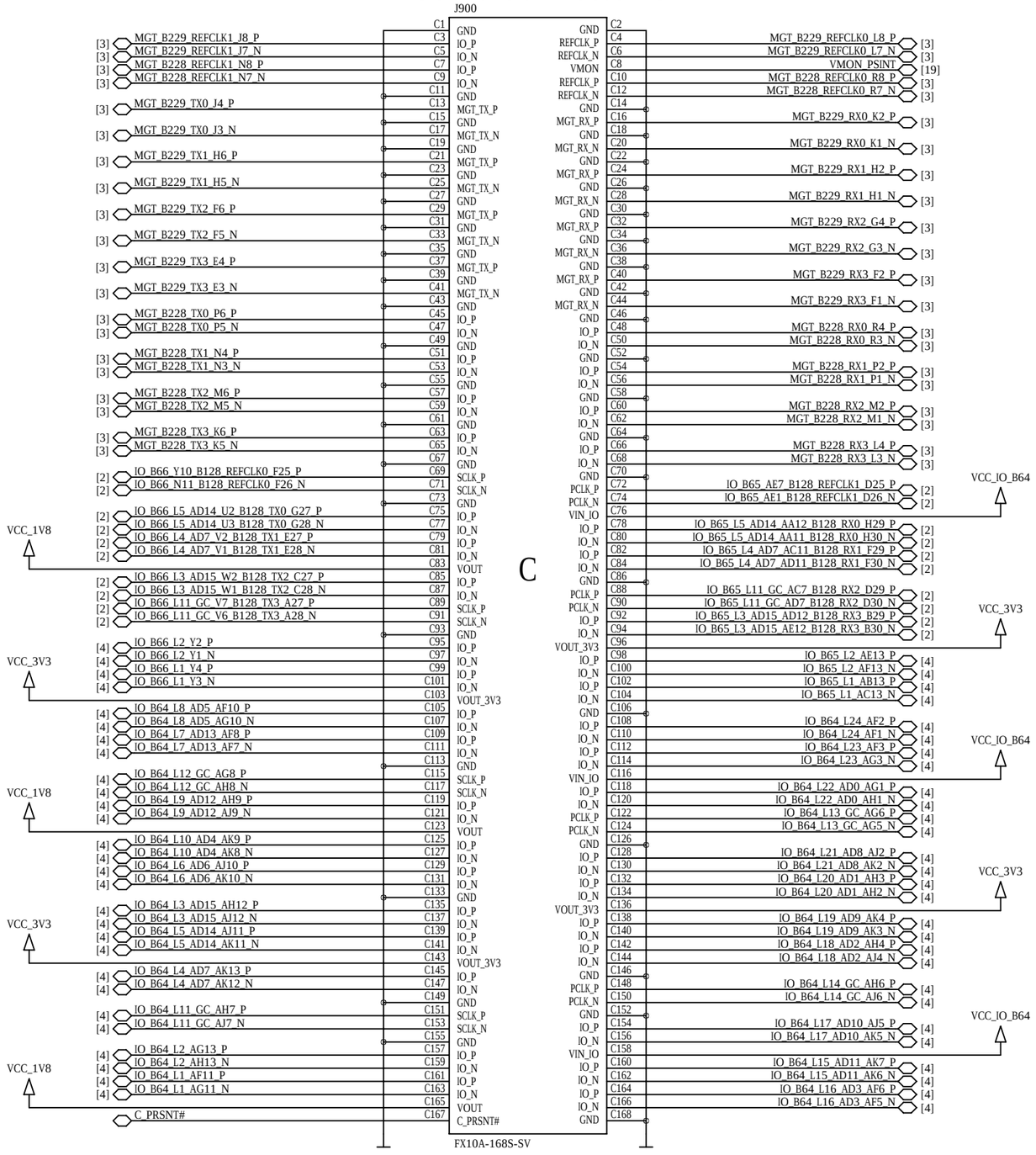
Module Connector C



IO Voltage Generation

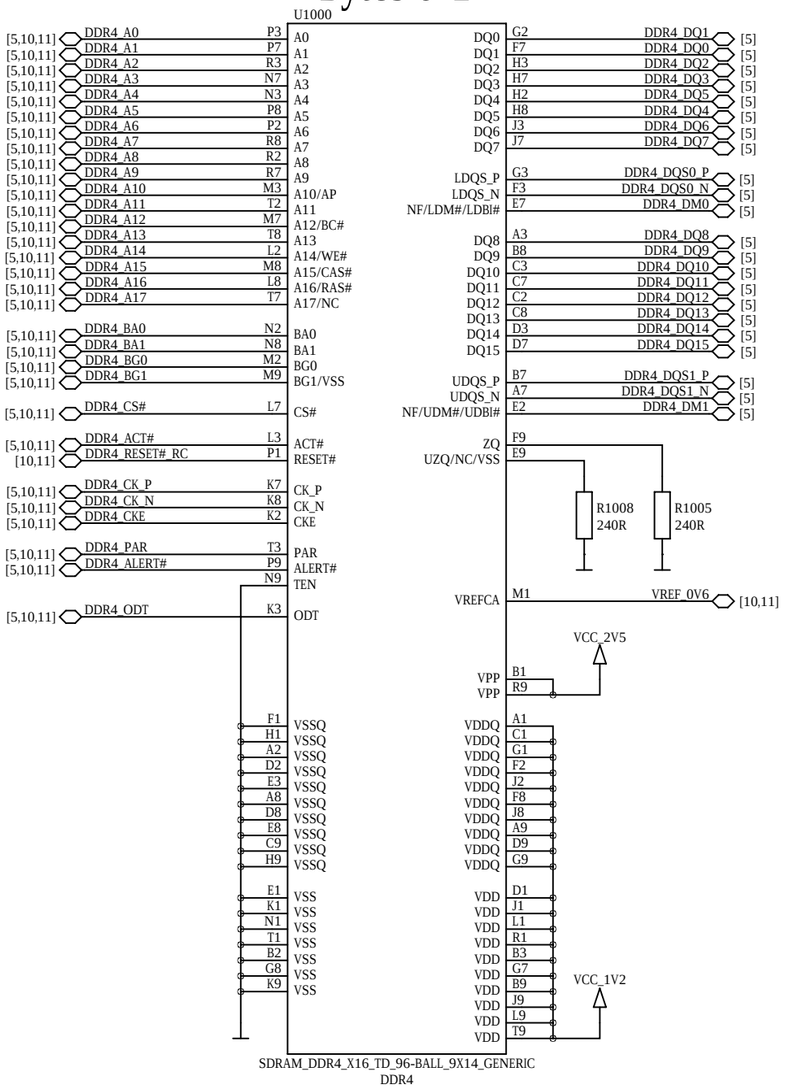
when C connector is not present on base board
not included in user schematics

This part is intentionally left blank.

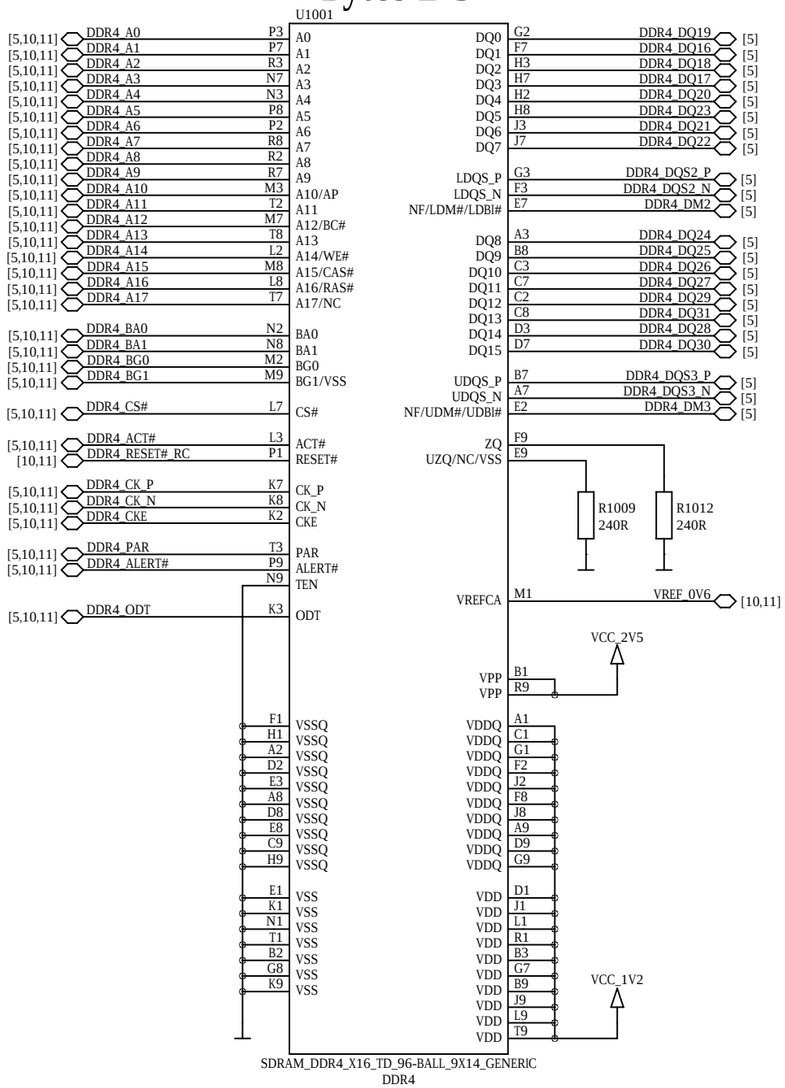
ENCLUSTRA	Copyright	© 2020 by Enclustra GmbH	Sheet Name	09_MODULE_CONNECTOR_C	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 9 / 22

DDR4 SDRAM

Bytes 0-1



Bytes 2-3

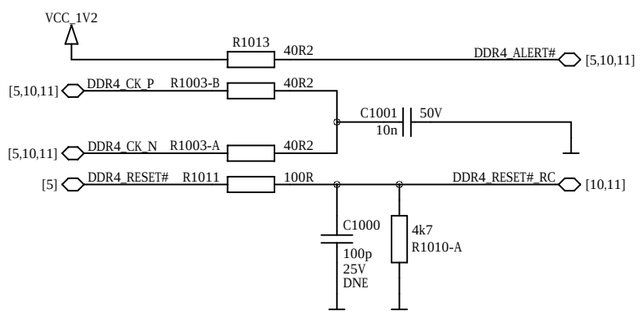


DDR4 Termination

not included in user schematics

This part is intentionally left blank.

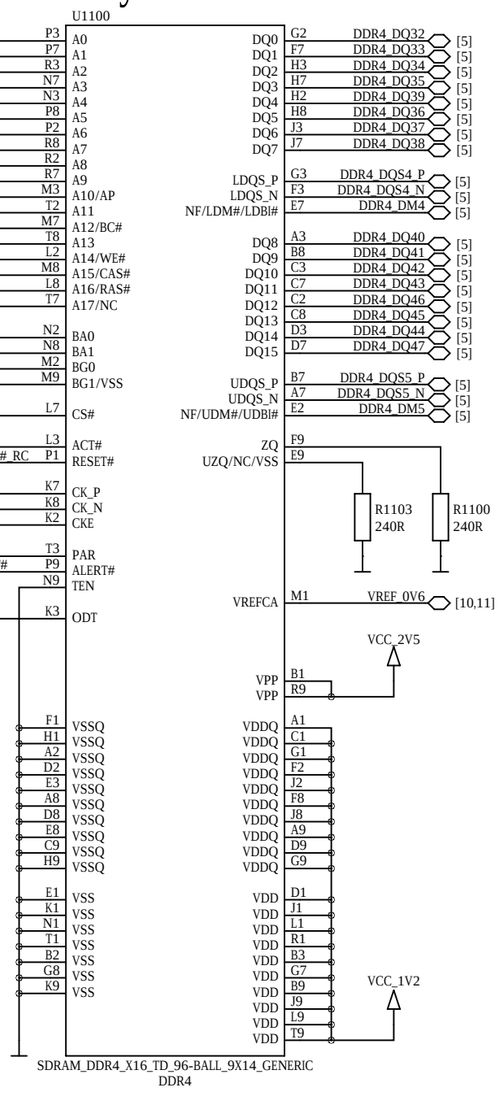
DDR4 Miscellaneous



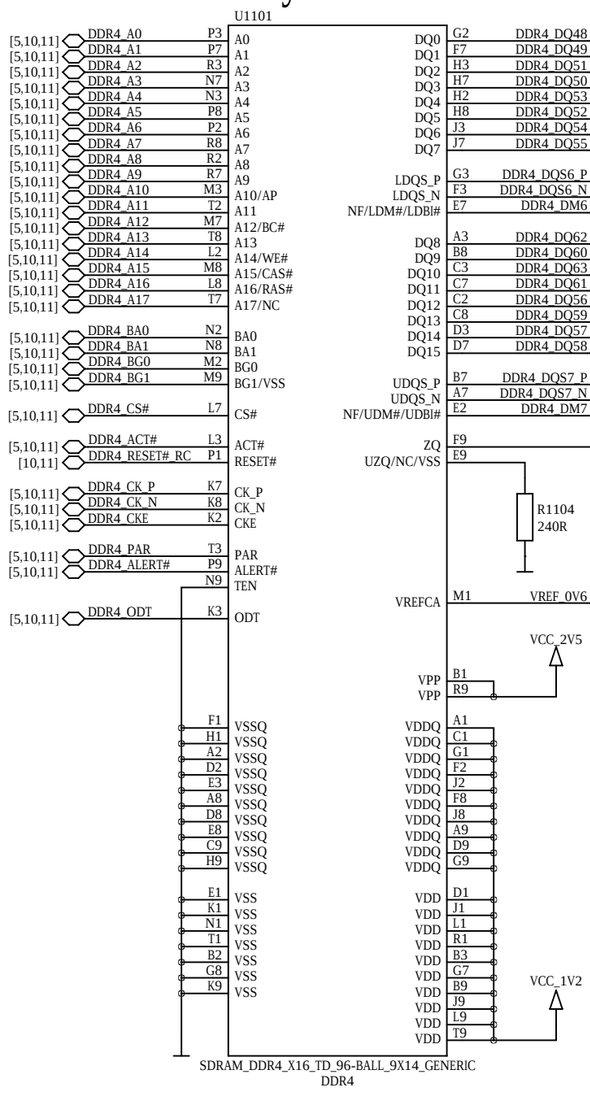
ENCLUSTRA	Copyright	© 2020 by Enclustra GmbH	Sheet Name	10_DDR4_SDRAM_0-3	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 10 / 22

DDR4 SDRAM

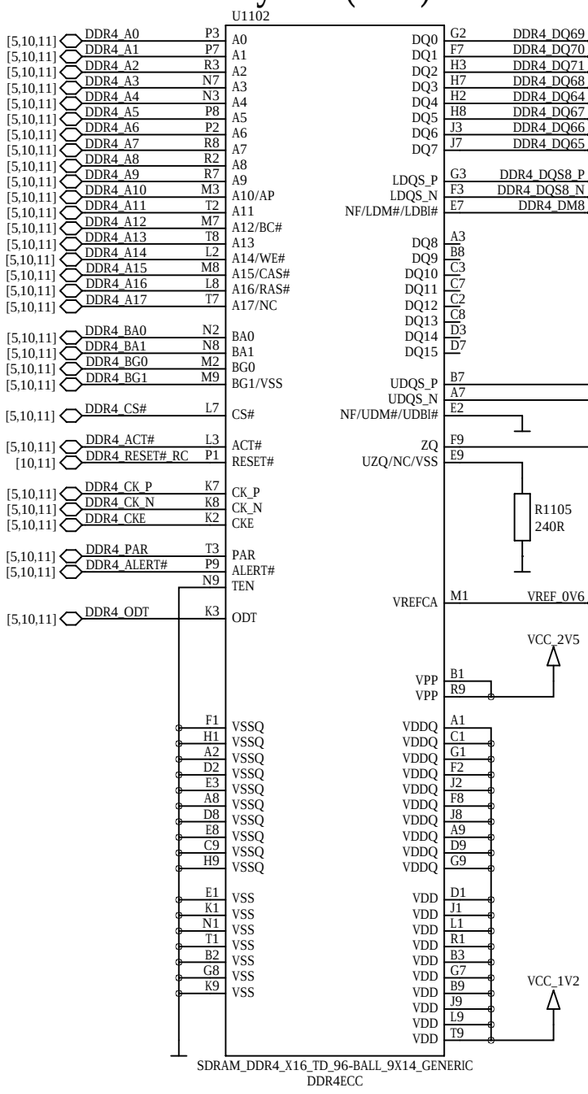
Bytes 4-5



Bytes 6-7



Byte 8 (ECC)

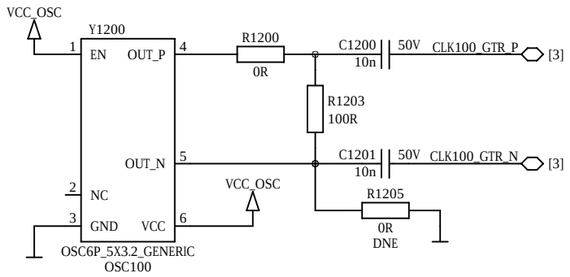


DDR4 Decoupling

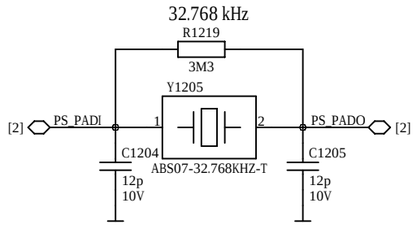
not included in user schematics

This part is intentionally left blank.

GTR 100 MHz Oscillator



RTC Crystal

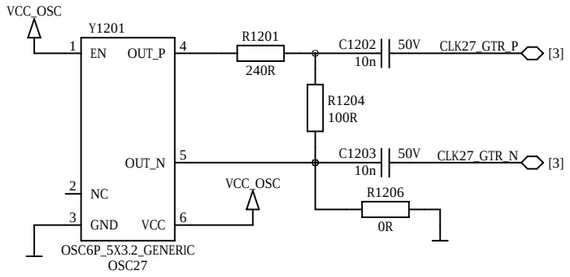


Oscillator Power Filters

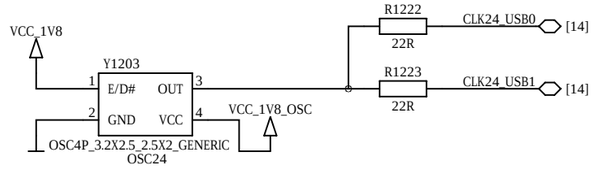
not included in user schematics

This part is intentionally left blank.

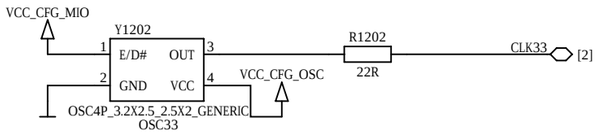
GTR 27 MHz Oscillator



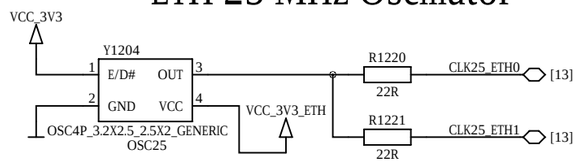
USB 24 MHz Oscillator



PS 33.3 MHz Oscillator



ETH 25 MHz Oscillator



HD Bank Termination

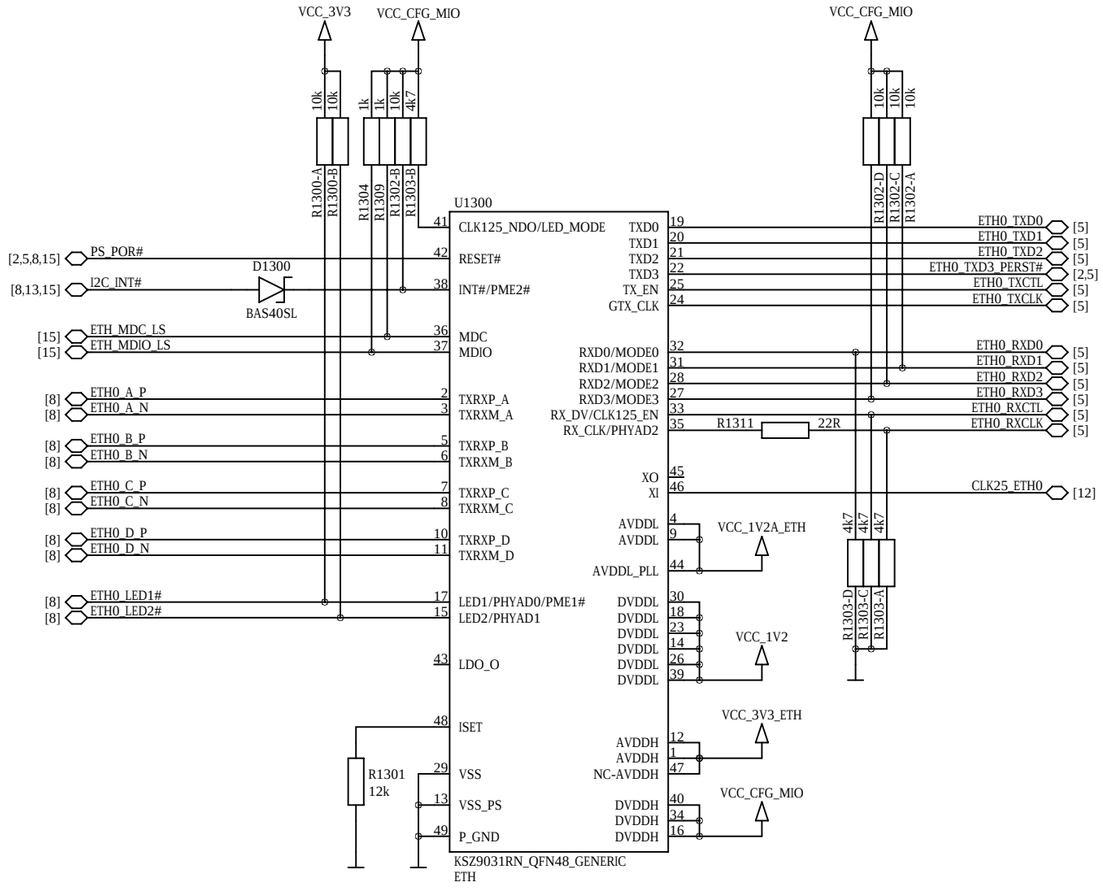
optional

[4,8]	IO_B48_L1_AD15_C12_P	R1207	100R DNE	IO_B48_L1_AD15_B11_N	[4,8]	[4,8]	IO_B48_L7_HDGC_F12_P	R1224	100R DNE	IO_B48_L7_HDGC_F11_N	[4,8]
[4,8]	IO_B48_L2_AD14_A12_P	R1208	100R DNE	IO_B48_L2_AD14_A11_N	[4,8]	[4,8]	IO_B48_L8_HDGC_G10_P	R1225	100R DNE	IO_B48_L8_HDGC_F10_N	[4,8]
[4,8]	IO_B48_L3_AD13_B10_P	R1209	100R DNE	IO_B48_L3_AD13_A10_N	[4,8]	[4,8]	IO_B48_L9_AD11_K13_P	R1226	100R DNE	IO_B48_L9_AD11_K12_N	[4,8]
[4,8]	IO_B48_L4_AD12_D11_P	R1210	100R DNE	IO_B48_L4_AD12_C11_N	[4,8]	[4,8]	IO_B48_L10_AD10_H12_P	R1227	100R DNE	IO_B48_L10_AD10_G11_N	[4,8]
[4,8]	IO_B48_L6_HDGC_E10_P	R1211	100R DNE	IO_B48_L6_HDGC_D10_N	[4,8]	[4,8]	IO_B48_L11_AD9_J12_P	R1228	100R DNE	IO_B48_L11_AD9_H11_N	[4,8]
[4,8]	IO_B48_L5_HDGC_E12_P	R1212	100R DNE	IO_B48_L5_HDGC_D12_N	[4,8]	[4,8]	IO_B48_L12_AD8_J11_P	R1229	100R DNE	IO_B48_L12_AD8_J10_N	[4,8]
[4,8]	IO_B47_L1_AD11_B15_P	R1213	100R DNE	IO_B47_L1_AD11_A15_N	[4,8]	[4,8]	IO_B47_L7_HDGC_AD5_F15_P	R1230	100R DNE	IO_B47_L7_HDGC_AD5_E15_N	[4,8]
[4,8]	IO_B47_L2_AD10_B14_P	R1214	100R DNE	IO_B47_L2_AD10_A14_N	[4,8]	[4,8]	IO_B47_L8_HDGC_AD4_G13_P	R1231	100R DNE	IO_B47_L8_HDGC_AD4_F13_N	[4,8]
[4,8]	IO_B47_L3_AD9_B13_P	R1215	100R DNE	IO_B47_L3_AD9_A13_N	[4,8]	[4,8]	IO_B47_L9_AD3_G15_P	R1232	100R DNE	IO_B47_L9_AD3_G14_N	[4,8]
[4,8]	IO_B47_L4_AD8_C14_P	R1216	100R DNE	IO_B47_L4_AD8_C13_N	[4,8]	[4,8]	IO_B47_L10_AD2_K15_P	R1233	100R DNE	IO_B47_L10_AD2_J15_N	[4,8]
[4,8]	IO_B47_L5_HDGC_AD7_D15_P	R1217	100R DNE	IO_B47_L5_HDGC_AD7_D14_N	[4,8]	[4,8]	IO_B47_L11_AD1_K14_P	R1234	100R DNE	IO_B47_L11_AD1_J14_N	[4,8]
[4,8]	IO_B47_L6_HDGC_AD6_E14_P	R1218	100R DNE	IO_B47_L6_HDGC_AD6_E13_N	[4,8]	[4,8]	IO_B47_L12_AD0_H14_P	R1235	100R DNE	IO_B47_L12_AD0_H13_N	[4,8]

Sheet Name	12_OSCILLATORS	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 12 / 22

Gigabit Ethernet PHY 0

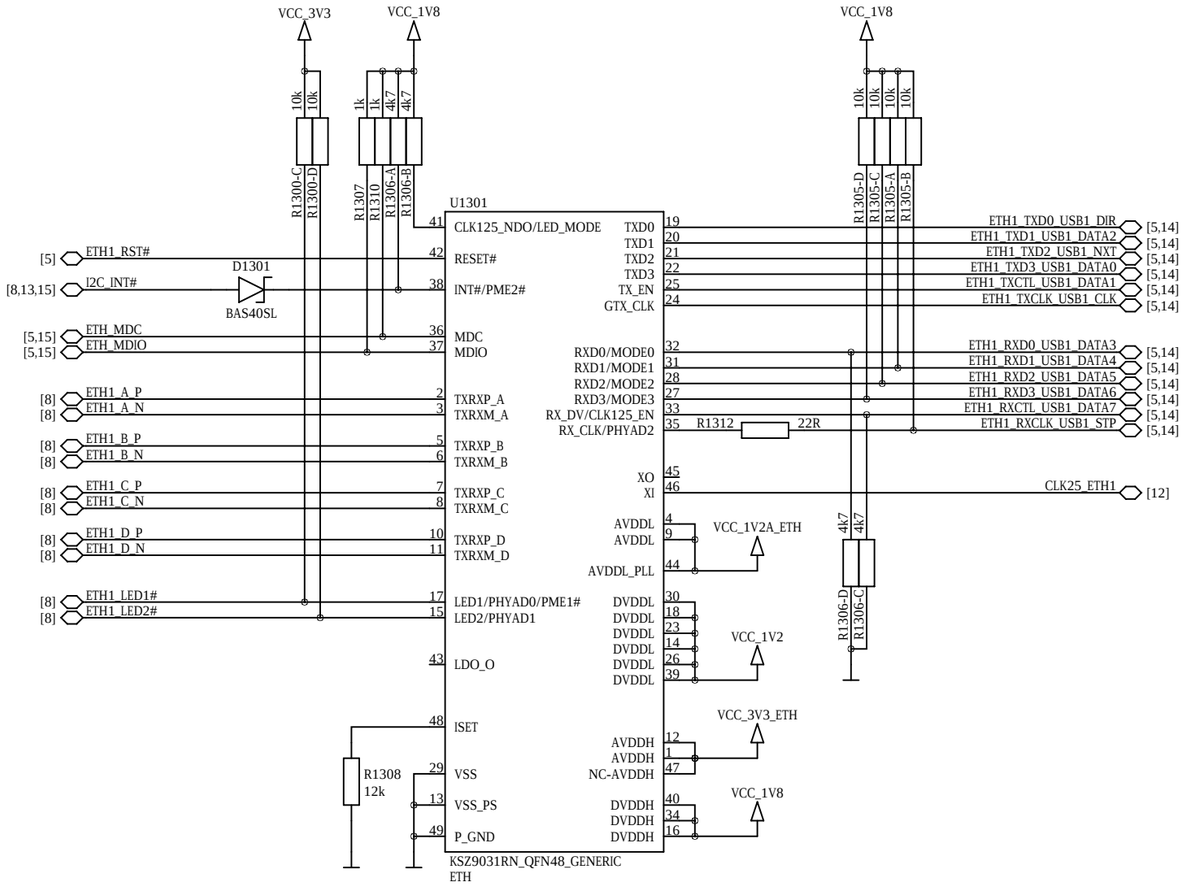
not available when using PS PCIe



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 011 -> 3
LED1 and LED2 are active low

Gigabit Ethernet PHY 1

not available when using USB1



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 111 -> 7
LED1 and LED2 are active low

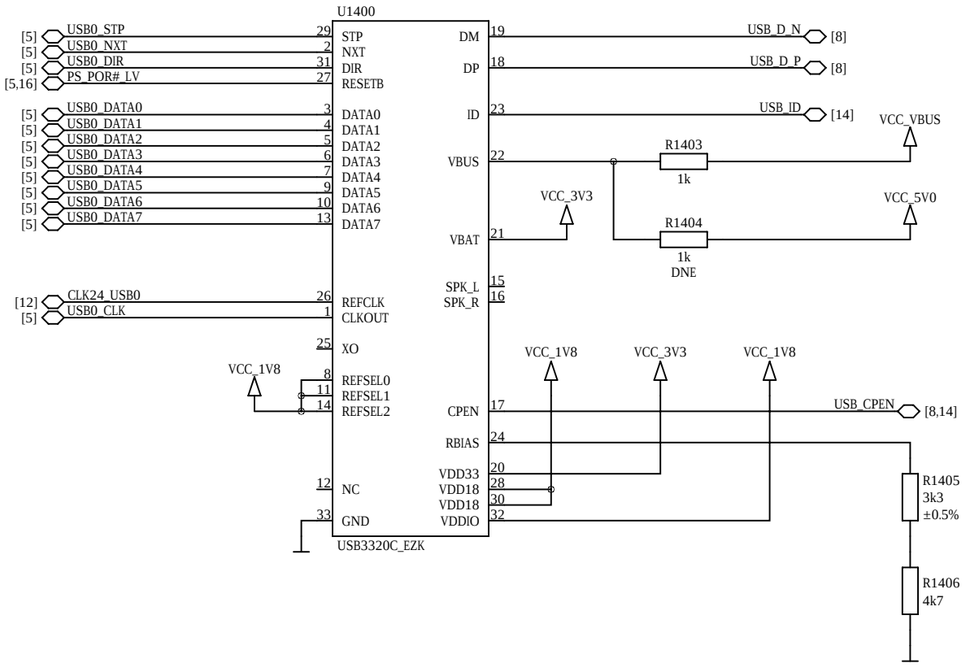
Ethernet Power Filters

not included in user schematics

This part is intentionally left blank.

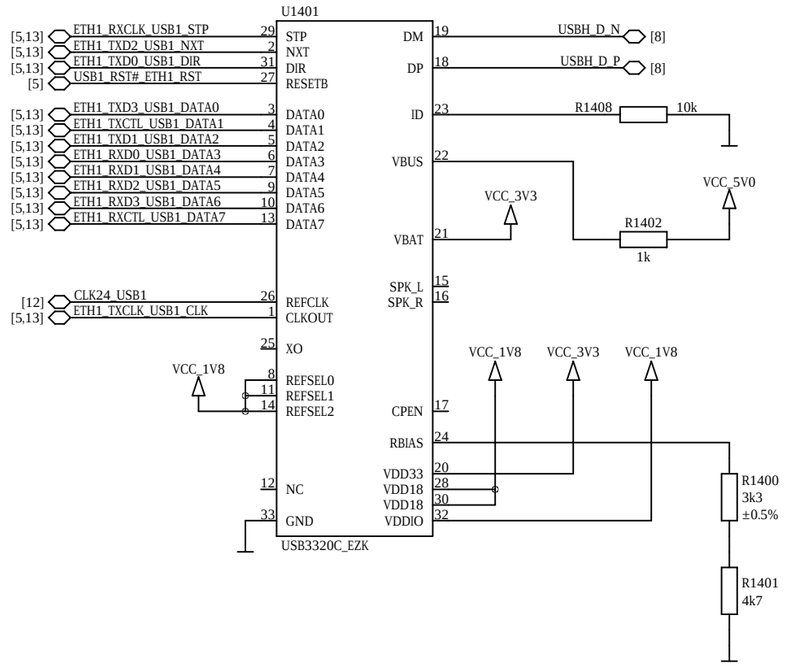
USB 2.0 Device/Host PHY 0

A-Device ID=GND, B-Device ID=Float, Not Used ID=VDD33

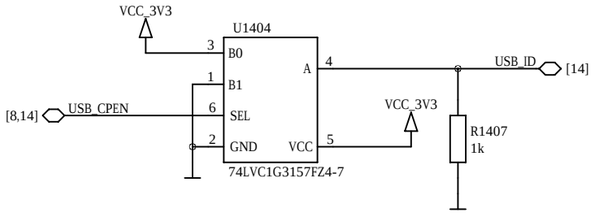


USB 2.0 Host PHY 1

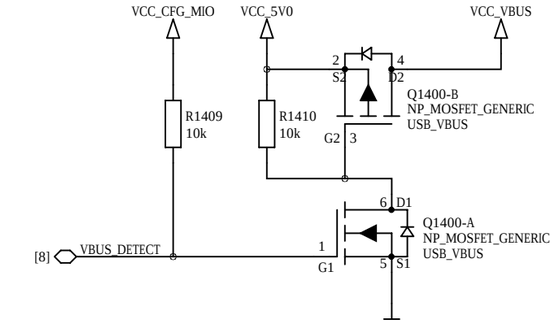
not available when using Ethernet 1



USB 2.0 Host/Device Mode



USB 2.0 VBUS Detect

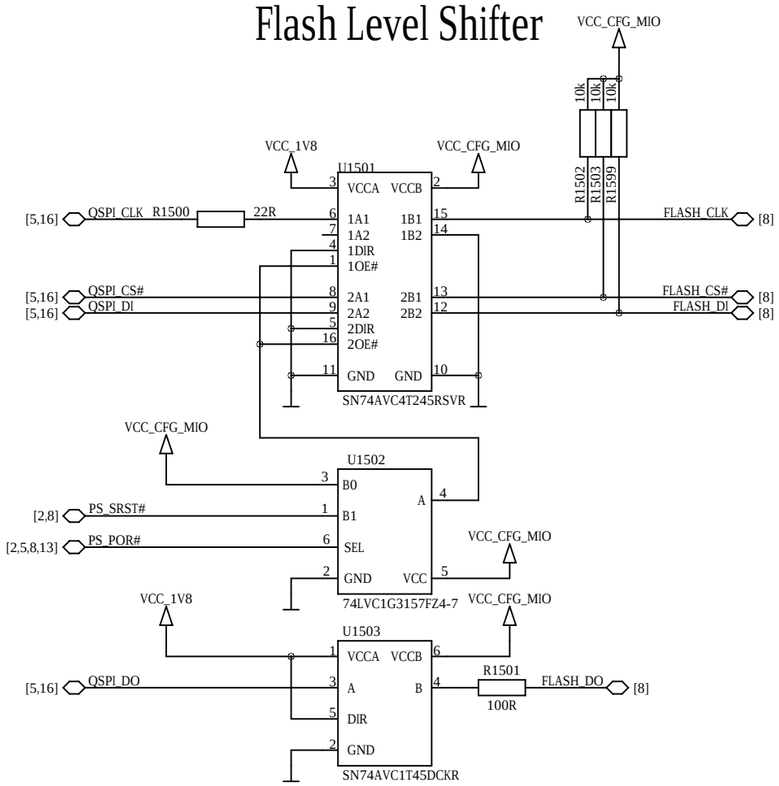


USB 2.0 Power Decoupling

not included in user schematics

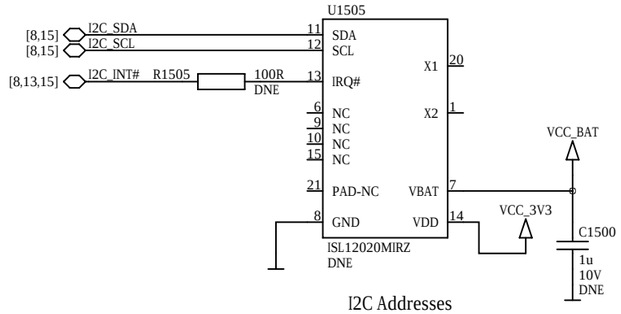
This part is intentionally left blank.

Flash Level Shifter



Real-time Clock

optional

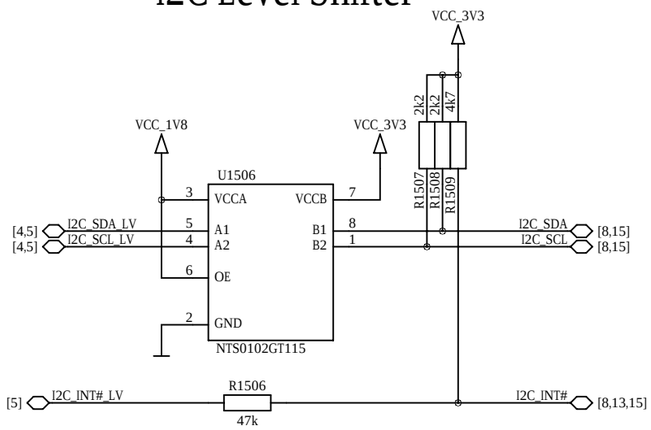


I2C Addresses

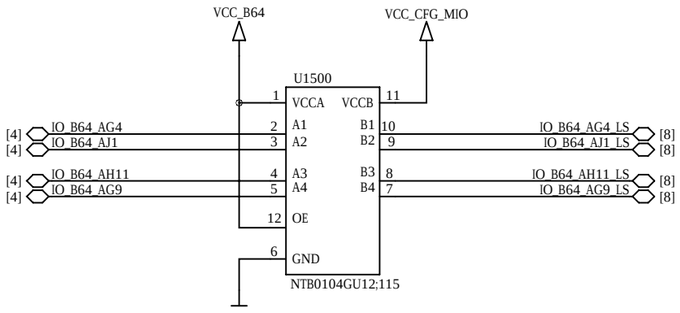
RTC registers: 1 1 0 1 1 1 1 Rw

User SRAM: 1 0 1 0 1 1 1 Rw

I2C Level Shifter

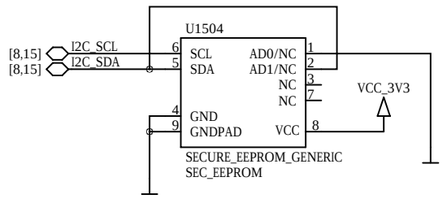


IO Level Shifter



Secure EEPROM

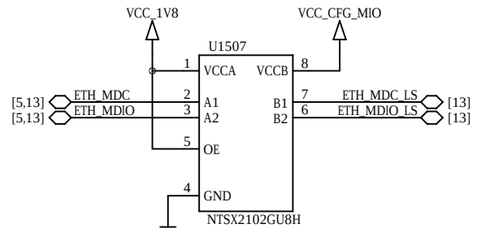
for Enclustra use only



ATSHA204A-MAHDA-T I2C Address: 1 1 0 0 1 0 0 Rw

DS28CN01U-A00+ I2C Address: 1 0 1 1 1 0 0 Rw

MDIO Level Shifter



ENCLUSTRA	Copyright	© 2020 by Enclustra GmbH	Sheet Name	15_LEVEL_SHIFTERS_EEPROM	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
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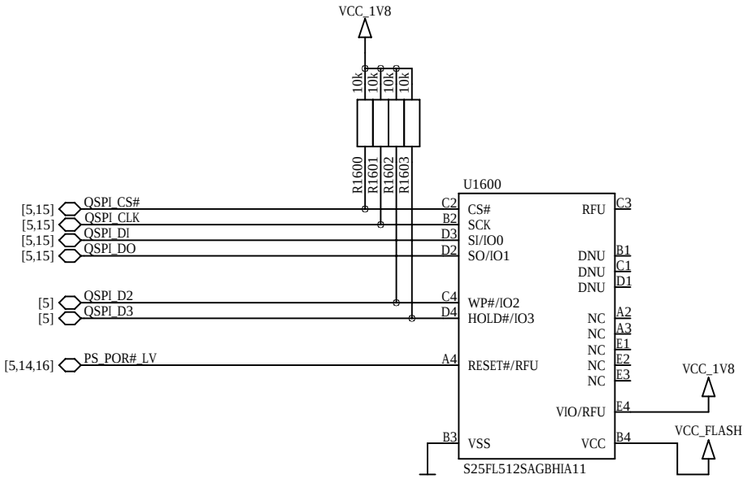
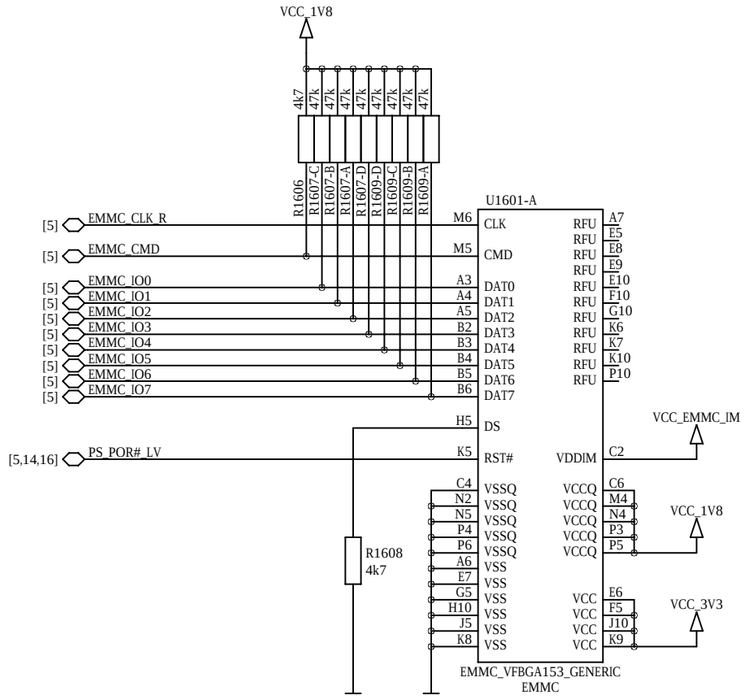
Quad SPI Flash

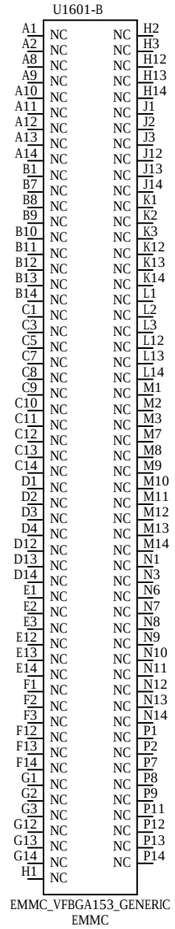
pin compatible with Micron N25Q512A11G1240F

Micron requires VCC_FLASH = 1.8V



eMMC Flash





Quad SPI Power

not included in user schematics

This part is intentionally left blank.

eMMC Power

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2020 by Enclustra GmbH	Sheet Name	16_EMMC_QSPI_FLASH	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 16 / 22

Dual Buck Converter

channel 1: 3.3V 6A 5% channel 2: 1.2V 6A 5%

not included in user schematics

This part is intentionally left blank.

Supported Voltage Ranges

Power Rail	Direction	Range	Tolerance
VCC_MOD	input	5 - 15V	±5%
VCC_CFG_MIO	input	1.8 - 3.3V	±5%
VCC_IO_B47	input	1.2 - 3.3V	±5%
VCC_IO_B48	input	1.2 - 3.3V	±5%
VCC_IO_B64	input	1.0 - 1.8V	±5%
VCC_IO_B65	input	1.0 - 1.8V	±5%
VCC_IO_B66	input	1.0 - 1.8V	±5%
VCC_BAT	input	2.7 - 3.6V *	-
VCC_1V8	output	1.8V	±5%
VCC_2V5	output	2.5V	±5%
VCC_3V3	output	3.3V	±5%

When using VCC_IO_B47, VCC_IO_B48 at 3.3V, the tolerance is -5% +3%.

When using VCC_IO_B64 below 1.2V, the level shifted signals of bank 64 are not operational.

When using VCC_IO_B66 below 1.8V, the I2C bus on bank 66 is not operational.

* Voltage range valid for LDO assembly option for VCC_BAT_FPGA (default assembly variant)

DC / DC Converter 0.85/0.9V/0.72 35A 3%

not included in user schematics

This part is intentionally left blank.

Input Power Filter

not included in user schematics

This part is intentionally left blank.

LDO 5.0V 0.15A

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2020 by Enclustra GmbH	Sheet Name	17_POWER_INT_3.3V_1.2V_5.0V	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 17 / 22

Dual Buck Converter

channel 1: 0.85/0.9V 6A 3% channel 2: 0.9V 6A 3%

not included in user schematics

This part is intentionally left blank.

LDO 2.5V 0.5A

not included in user schematics

This part is intentionally left blank.

Power Converter Synchronization

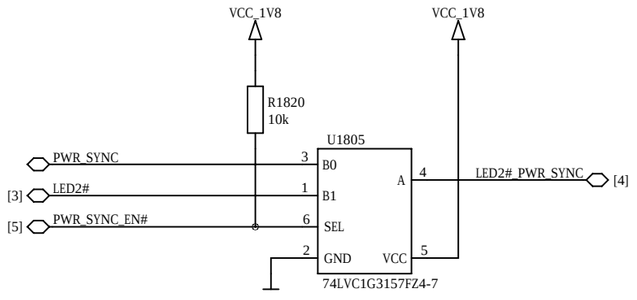
not included in user schematics

This part is intentionally left blank.

DDR4 Termination Voltage Regulator

not included in user schematics

This part is intentionally left blank.



DDR4 VREF Decoupling

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2020 by Enclustra GmbH	Sheet Name	18_POWER_PSINT_0.9V_2.5V_VTT	Customer No	0000	Revision	R4.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU1	Project No	437	Designed	MHEI	Date 4 Feb 2020	Sheet/sheets 18 / 22

Buck Converter 1.8V

1.8V 3A 3%
not included in user schematics

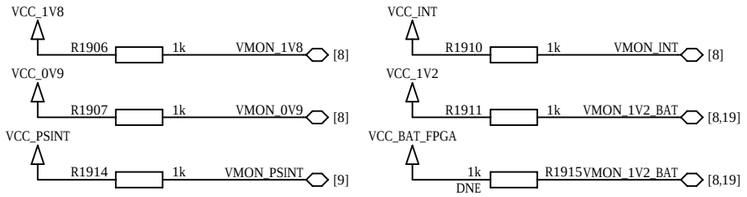
This part is intentionally left blank.

LDO 1.2V 10 mA

not included in user schematics

This part is intentionally left blank.

Voltage Monitoring



Voltage Reference

This part is intentionally left blank.

FPGA I/O Over-Voltage Protection

not included in user schematics

This part is intentionally left blank.

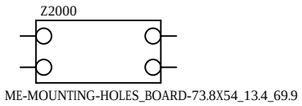
LDO 0.85V 0.5A

only used for -1LI, -2LE and -3E speed grade SoC FPGAs
not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright © 2020 by Enclustra GmbH	Sheet Name 19_POWER_1.8V_0.85V_BAT	Customer No 0000	Revision R4.1	DNE = do not equip	Confidential	
	Company Enclustra FPGA Solution Center	Project Mercury+ XU1	Project No 437	Designed MHEI	Date 4 Feb 2020	Sheet/sheets 19 / 22	

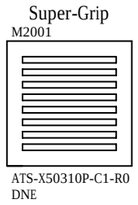
Module Mounting Holes M3



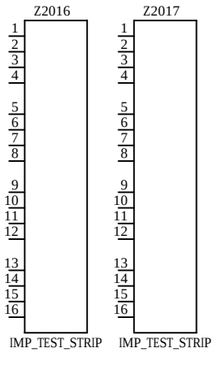
Panel Tooling Holes

FPGA Heat Sink

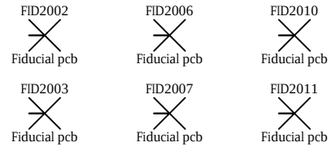
optional



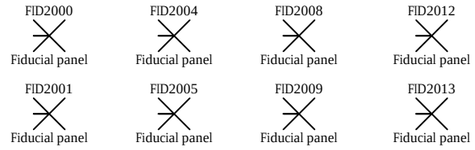
Impedance Test Strip



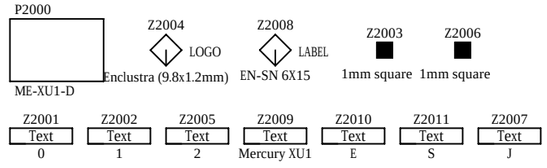
PCB Fiducials



Panel Fiducials



PCB / Logo / Pin-1 Marking / Text



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Component Variants

FPGA	DDR4	DDR4ECC	eMMC	Ethernet PHY	OSC27	OSC24	MGT_SEL	SEC_EEPROM
Part U200A XCZU6CG-1FFVC900E EN102377 Part U200B XCZU6EG-1FFVC900I EN101561 Part U200C XCZU9EG-1FFVC900E EN102616 Part U200D XCZU9EG-2FFVC900I EN101562 Part U200E XCZU9EG-3FFVC900E EN102113 Part U200F XCZU15EG-1FFVC900E EN102609 Part U200G XCZU15EG-2FFVC900I EN101957	Part U1000A:1 H5AN4G6NAFR-UHC EN101655 Part U1000A:2 MT40A256M16GE-083E EN101632 Part U1000B K4A4G165WE-BIRC EN101868 Part U1000C K4A8G165WB-BIRC EN101979 Part U1001A:1 H5AN4G6NAFR-UHC EN101655 Part U1001A:2 MT40A256M16GE-083E EN101632 Part U1001B K4A4G165WE-BIRC EN101868 Part U1001C K4A8G165WB-BIRC EN101979 Part U1100A:1 H5AN4G6NAFR-UHC EN101655 Part U1100A:2 MT40A256M16GE-083E EN101632 Part U1100B K4A4G165WE-BIRC EN101868 Part U1100C K4A8G165WB-BIRC EN101979 Part U1101A:1 H5AN4G6NAFR-UHC EN101655 Part U1101A:2 MT40A256M16GE-083E EN101632 Part U1101B K4A4G165WE-BIRC EN101868 Part U1101C K4A8G165WB-BIRC EN101979	Part U1102A:1 H5AN4G6NAFR-UHC EN101655 Part U1102A:2 MT40A256M16GE-083E EN101632 Part U1102B K4A4G165WE-BIRC EN101868 Part U1102C K4A8G165WB-BIRC EN101979	Part U1601A H26M52208FPRI EN101865 Part U1601B EMMC16G-IB29-PZ90 EN102591	Part U1300A KSZ9031RNXIA EN101934 Part U1300B KSZ9031RNXCA EN100202 Part U1301A KSZ9031RNXIA EN101934 Part U1301B KSZ9031RNXCA EN100202	Part Y1201A ASEMPC_27.000MHZ-LR-T EN101608 Part Y1201B ASEMPC-27.000MHZ-XR-T EN101609	Part Y1203A ASDMB-24.000MHZ-LC-T EN101221 Part Y1203B ASEMB_24.000MHZ-LC-T EN101187	R207, R209, R211, R213, R215, R217, R219. R221, R223, R225 or R208, R210, R212, R214, R216, R218, R220. R222, R224, R226	Part U1504A ATSHA204A-MAHDA-T EN100827 Part U1504B DS28CN01U-A00+ EN100280

Assembly Variants

Assembly Variant	FPGA	DDR4	DDR4ECC	eMMC	Ethernet PHY	OSC27	OSC24	MGT_SEL	SEC_EEPROM
Variant EN102601:0 ME-XU1-6CG-1E-D11E-R4.1	Option EN102601:1 FPGA EN102377	Option EN102601:2 DDR4 EN101868	Option EN102601:3 DDR4ECC EN101868	Option EN102601:4 EMMC EN102591	Option EN102601:5 ETH EN101934	Option EN102601:6 OSC27 EN101608	Option EN102601:7 OSC24 EN101221	Option EN102601:8 MGT_SEL DNE	Option EN102601:9 SEC_EEPROM EN100827
Variant EN102600:0 ME-XU1-6CG-1E-D11E-G1-R4.1	Option EN102600:1 FPGA EN102377	Option EN102600:2 DDR4 EN101868	Option EN102600:3 DDR4ECC EN101868	Option EN102600:4 EMMC EN102591	Option EN102600:5 ETH EN101934	Option EN102600:6 OSC27 EN101608	Option EN102600:7 OSC24 EN101221	Option EN102600:8 MGT_SEL	Option EN102600:9 SEC_EEPROM EN100827
Variant EN102372:0 ME-XU1-6EG-1I-D11E-R4.1	Option EN102372:1 FPGA EN101561	Option EN102372:2 DDR4 EN101868	Option EN102372:3 DDR4ECC EN101868	Option EN102372:4 EMMC EN102591	Option EN102372:5 ETH EN101934	Option EN102372:6 OSC27 EN101608	Option EN102372:7 OSC24 EN101221	Option EN102372:8 MGT_SEL DNE	Option EN102372:9 SEC_EEPROM EN100827
Variant EN102614:0 ME-XU1-6EG-1I-D11E-G1-R4.1	Option EN102614:1 FPGA EN101561	Option EN102614:2 DDR4 EN101868	Option EN102614:3 DDR4ECC EN101868	Option EN102614:4 EMMC EN102591	Option EN102614:5 ETH EN101934	Option EN102614:6 OSC27 EN101608	Option EN102614:7 OSC24 EN101221	Option EN102614:8 MGT_SEL	Option EN102614:9 SEC_EEPROM EN100827
Variant EN102602:0 ME-XU1-9EG-1E-D11E-G1-R4.1	Option EN102602:1 FPGA EN102616	Option EN102602:2 DDR4 EN101868	Option EN102602:3 DDR4ECC EN101868	Option EN102602:4 EMMC EN102591	Option EN102602:5 ETH EN101934	Option EN102602:6 OSC27 EN101608	Option EN102602:7 OSC24 EN101221	Option EN102602:8 MGT_SEL	Option EN102602:9 SEC_EEPROM EN100827
Variant EN102373:0 ME-XU1-9EG-2I-D12E-R4.1	Option EN102373:1 FPGA EN101562	Option EN102373:2 DDR4 EN101979	Option EN102373:3 DDR4ECC EN101979	Option EN102373:4 EMMC EN102591	Option EN102373:5 ETH EN101934	Option EN102373:6 OSC27 EN101608	Option EN102373:7 OSC24 EN101221	Option EN102373:8 MGT_SEL DNE	Option EN102373:9 SEC_EEPROM EN100827
Variant EN102603:0 ME-XU1-9EG-2I-D12E-G1-R4.1	Option EN102603:1 FPGA EN101562	Option EN102603:2 DDR4 EN101979	Option EN102603:3 DDR4ECC EN101979	Option EN102603:4 EMMC EN102591	Option EN102603:5 ETH EN101934	Option EN102603:6 OSC27 EN101608	Option EN102603:7 OSC24 EN101221	Option EN102603:8 MGT_SEL	Option EN102603:9 SEC_EEPROM EN100827
Variant EN102374:0 ME-XU1-9EG-3E-D12E-R4.1	Option EN102374:1 FPGA EN102113	Option EN102374:2 DDR4 EN101979	Option EN102374:3 DDR4ECC EN101979	Option EN102374:4 EMMC EN102591	Option EN102374:5 ETH EN101934	Option EN102374:6 OSC27 EN101608	Option EN102374:7 OSC24 EN101221	Option EN102374:8 MGT_SEL DNE	Option EN102374:9 SEC_EEPROM EN100827
Variant EN102604:0 ME-XU1-15EG-1E-D12E-G1-R4.1	Option EN102604:1 FPGA EN102609	Option EN102604:2 DDR4 EN101979	Option EN102604:3 DDR4ECC EN101979	Option EN102604:4 EMMC EN102591	Option EN102604:5 ETH EN101934	Option EN102604:6 OSC27 EN101608	Option EN102604:7 OSC24 EN101221	Option EN102604:8 MGT_SEL	Option EN102604:9 SEC_EEPROM EN100827
Variant EN102375:0 ME-XU1-15EG-2I-D12E-R4.1	Option EN102375:1 FPGA EN101957	Option EN102375:2 DDR4 EN101979	Option EN102375:3 DDR4ECC EN101979	Option EN102375:4 EMMC EN102591	Option EN102375:5 ETH EN101934	Option EN102375:6 OSC27 EN101608	Option EN102375:7 OSC24 EN101221	Option EN102375:8 MGT_SEL DNE	Option EN102375:9 SEC_EEPROM EN100827
Variant EN102376:0 ME-XU1-15EG-2I-D12E-G1-R4.1	Option EN102376:1 FPGA EN101957	Option EN102376:2 DDR4 EN101979	Option EN102376:3 DDR4ECC EN101979	Option EN102376:4 EMMC EN102591	Option EN102376:5 ETH EN101934	Option EN102376:6 OSC27 EN101608	Option EN102376:7 OSC24 EN101221	Option EN102376:8 MGT_SEL	Option EN102376:9 SEC_EEPROM EN100827

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	Company Enclustra FPGA Solution Center	Project Mercury+ XU1	Project No 437	Designed MHEI	Date 4 Feb 2020	Sheet/sheets 21 / 22	

Component Variants

OSC25	OSC33	OSC100	L0U68	L2U2	L_VCC_INT	L1U5	LDO_0V85	USB_VBUS	VCC_PSINT_0V9	VCC_INT_A	VCC_INT_B
Part Y1204A ASDMB-25.000MHZ-LC-T EN101588	Part Y1202A ASDMB_33.333MHZ-LC-T EN100285	Part Y1200A ASDMPLV-100.000MHZ-LR-T3 EN101610	Part L1703A 0.68uH EN102112	Part L1900A 2u2 EN102185	Part L1702A 0u1 EN102190	Part L1700A 1u5 EN102613	R1912 - R1913, U1905 or R1909	Part Q1400A DMC2038LVT EN100503	R1824, R1804 for 0.9V or R1800 for 0.85V	Part R1725A 10k EN101365	Part R1727A 4k7 EN101399
Part Y1204B ASEMB_25.000MHZ-LC-T EN101589	Part Y1202B ASEMB_33.333MHZ-LC-T EN100914	Part Y1200B ASFLMPLV-100.000MHZ-LR-T EN101611	Part L1703B 0.68uH EN102445	Part L1900B 2u2 EN102208	Part L1702B 220n EN102189	Part L1700B 1u5 EN102207		Part Q1400B DMC2053UVT-7 EN102320		Part R1725B 47k EN101397	Part R1727B 100R EN101363
			Part L1800A 0.68uH EN102112	Part L1900C 2u2 EN101680				Part Q1400C DMC2057UVT-7 EN102321			
			Part L1800B 0.68uH EN102445								
			Part L1801A 0.68uH EN102112								
			Part L1801B 0.68uH EN102445								

Assembly Variants

OSC25	OSC33	OSC100	L0U68	L2U2	L_VCC_INT	L1U5	LDO_0V85	USB_VBUS	VCC_PSINT_0V9	VCC_INT_A	VCC_INT_B
Option EN102601:10 OSC25 EN101588	Option EN102601:11 OSC33 EN100914	Option EN102601:12 OSC100 EN101610	Option EN102601:13 L0U68 EN102112	Option EN102601:14 L2U2 EN101680	Option EN102601:15 L_VCC_INT EN102189	Option EN102601:16 L1U5 EN102207	Option EN102601:17 LDO_0V85 DNE	Option EN102601:18 USB_VBUS EN100503	Option EN102601:19 VCC_PSINT_0V9 DNE	Option EN102601:20 VCC_INT_A EN101365	Option EN102601:21 VCC_INT_B EN101399
Option EN102600:10 OSC25 EN101588	Option EN102600:11 OSC33 EN100914	Option EN102600:12 OSC100 EN101610	Option EN102600:13 L0U68 EN102112	Option EN102600:14 L2U2 EN101680	Option EN102600:15 L_VCC_INT EN102189	Option EN102600:16 L1U5 EN102207	Option EN102600:17 LDO_0V85 DNE	Option EN102600:18 USB_VBUS EN100503	Option EN102600:19 VCC_PSINT_0V9 DNE	Option EN102600:20 VCC_INT_A EN101365	Option EN102600:21 VCC_INT_B EN101399
Option EN102372:10 OSC25 EN101588	Option EN102372:11 OSC33 EN100914	Option EN102372:12 OSC100 EN101610	Option EN102372:13 L0U68 EN102112	Option EN102372:14 L2U2 EN101680	Option EN102372:15 L_VCC_INT EN102189	Option EN102372:16 L1U5 EN102207	Option EN102372:17 LDO_0V85 DNE	Option EN102372:18 USB_VBUS EN100503	Option EN102372:19 VCC_PSINT_0V9 DNE	Option EN102372:20 VCC_INT_A EN101365	Option EN102372:21 VCC_INT_B EN101399
Option EN102614:10 OSC25 EN101588	Option EN102614:11 OSC33 EN100914	Option EN102614:12 OSC100 EN101610	Option EN102614:13 L0U68 EN102112	Option EN102614:14 L2U2 EN101680	Option EN102614:15 L_VCC_INT EN102189	Option EN102614:16 L1U5 EN102207	Option EN102614:17 LDO_0V85 DNE	Option EN102614:18 USB_VBUS EN100503	Option EN102614:19 VCC_PSINT_0V9 DNE	Option EN102614:20 VCC_INT_A EN101365	Option EN102614:21 VCC_INT_B EN101399
Option EN102602:10 OSC25 EN101588	Option EN102602:11 OSC33 EN100914	Option EN102602:12 OSC100 EN101610	Option EN102602:13 L0U68 EN102112	Option EN102602:14 L2U2 EN101680	Option EN102602:15 L_VCC_INT EN102189	Option EN102602:16 L1U5 EN102207	Option EN102602:17 LDO_0V85 DNE	Option EN102602:18 USB_VBUS EN100503	Option EN102602:19 VCC_PSINT_0V9 DNE	Option EN102602:20 VCC_INT_A EN101365	Option EN102602:21 VCC_INT_B EN101399
Option EN102373:10 OSC25 EN101588	Option EN102373:11 OSC33 EN100914	Option EN102373:12 OSC100 EN101610	Option EN102373:13 L0U68 EN102112	Option EN102373:14 L2U2 EN101680	Option EN102373:15 L_VCC_INT EN102189	Option EN102373:16 L1U5 EN102207	Option EN102373:17 LDO_0V85 DNE	Option EN102373:18 USB_VBUS EN100503	Option EN102373:19 VCC_PSINT_0V9 DNE	Option EN102373:20 VCC_INT_A EN101365	Option EN102373:21 VCC_INT_B EN101399
Option EN102603:10 OSC25 EN101588	Option EN102603:11 OSC33 EN100914	Option EN102603:12 OSC100 EN101610	Option EN102603:13 L0U68 EN102112	Option EN102603:14 L2U2 EN101680	Option EN102603:15 L_VCC_INT EN102189	Option EN102603:16 L1U5 EN102207	Option EN102603:17 LDO_0V85 DNE	Option EN102603:18 USB_VBUS EN100503	Option EN102603:19 VCC_PSINT_0V9 DNE	Option EN102603:20 VCC_INT_A EN101365	Option EN102603:21 VCC_INT_B EN101399
Option EN102374:10 OSC25 EN101588	Option EN102374:11 OSC33 EN100914	Option EN102374:12 OSC100 EN101610	Option EN102374:13 L0U68 EN102112	Option EN102374:14 L2U2 EN101680	Option EN102374:15 L_VCC_INT EN102189	Option EN102374:16 L1U5 EN102207	Option EN102374:17 LDO_0V85	Option EN102374:18 USB_VBUS EN100503	Option EN102374:19 VCC_PSINT_0V9	Option EN102374:20 VCC_INT_A EN101397	Option EN102374:21 VCC_INT_B EN101363
Option EN102604:10 OSC25 EN101588	Option EN102604:11 OSC33 EN100914	Option EN102604:12 OSC100 EN101610	Option EN102604:13 L0U68 EN102112	Option EN102604:14 L2U2 EN101680	Option EN102604:15 L_VCC_INT EN102189	Option EN102604:16 L1U5 EN102207	Option EN102604:17 LDO_0V85 DNE	Option EN102604:18 USB_VBUS EN100503	Option EN102604:19 VCC_PSINT_0V9 DNE	Option EN102604:20 VCC_INT_A EN101365	Option EN102604:21 VCC_INT_B EN101399
Option EN102375:10 OSC25 EN101588	Option EN102375:11 OSC33 EN100914	Option EN102375:12 OSC100 EN101610	Option EN102375:13 L0U68 EN102112	Option EN102375:14 L2U2 EN101680	Option EN102375:15 L_VCC_INT EN102189	Option EN102375:16 L1U5 EN102207	Option EN102375:17 LDO_0V85 DNE	Option EN102375:18 USB_VBUS EN100503	Option EN102375:19 VCC_PSINT_0V9 DNE	Option EN102375:20 VCC_INT_A EN101365	Option EN102375:21 VCC_INT_B EN101399
Option EN102376:10 OSC25 EN101588	Option EN102376:11 OSC33 EN100914	Option EN102376:12 OSC100 EN101610	Option EN102376:13 L0U68 EN102112	Option EN102376:14 L2U2 EN101680	Option EN102376:15 L_VCC_INT EN102189	Option EN102376:16 L1U5 EN102207	Option EN102376:17 LDO_0V85 DNE	Option EN102376:18 USB_VBUS EN100503	Option EN102376:19 VCC_PSINT_0V9 DNE	Option EN102376:20 VCC_INT_A EN101365	Option EN102376:21 VCC_INT_B EN101399

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