COM-5501SOFT
10G Ethernet MAC
VHDL SOURCE CODE OVERVIEW

Overview

The COM-5501SOFT is a single-speed 10 Gigabit Ethernet Media Access Controller (MAC) core (including the **VHDL source code**) designed to support full-duplex 10 Gigabit throughput on low-cost FPGAs.

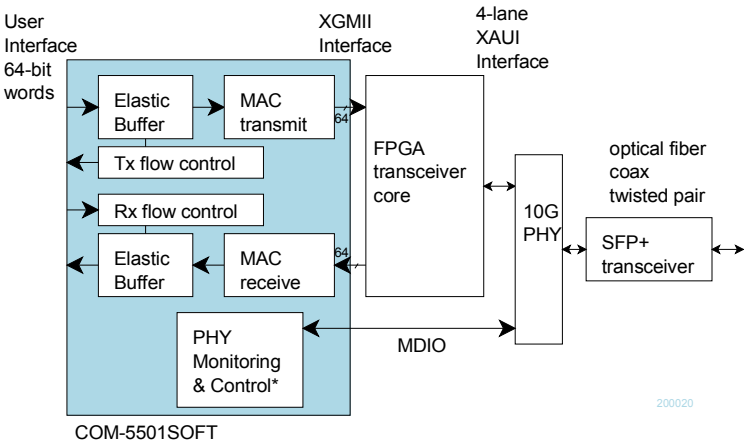
Key features include:

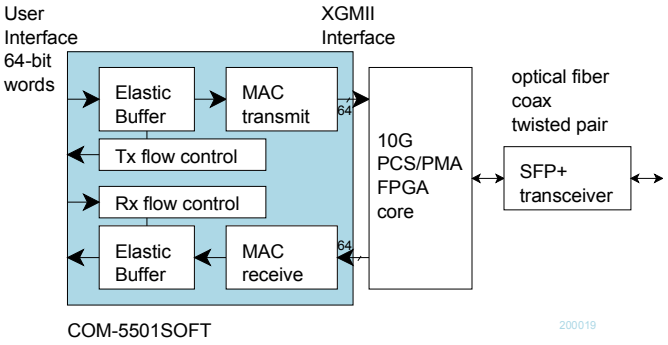
- Low-latency: 4 CLK (25.6ns)
- 10G interface:
  - XGMII interface.
  - Compatible with Xilinx free cores to external PHY (10G PCS/PMA, 7 series FPGA transceivers wizard, XAUI).
  - PHY monitoring and control through MDIO.
- Application interface: simple flow-controlled 64-bit interface synchronous with user-supplied clock. For full 10Gbps throughput, the user clock must be greater than 156.25 MHz.
- Transmit pause through MAC control messages
- VLAN-aware (i.e., IEEE 802.1Q conformant) can include VLAN tags
- Compatible with Jumbo frames. User can set MTU frame lengths for the transmit and receive paths.
- Address filter to reject undesirable received packets.
- Automatic
  - Preamble generation and removal
  - 32-bit CRC generation and checking.
  - Payload padding for very short transmit frames.

Keywords

10gE, Ethernet MAC, MAC core, XGMII, VHDL, FPGA, 10G Ethernet PHY, Ethernet transceiver.

Block Diagram





Target Hardware

The code is written entirely in generic VHDL and is thus portable to a variety of FPGAs. The code was developed and tested on a Xilinx 7-series FPGA.

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Device Utilization Summary

Device: Xilinx Artix7 –1 speed

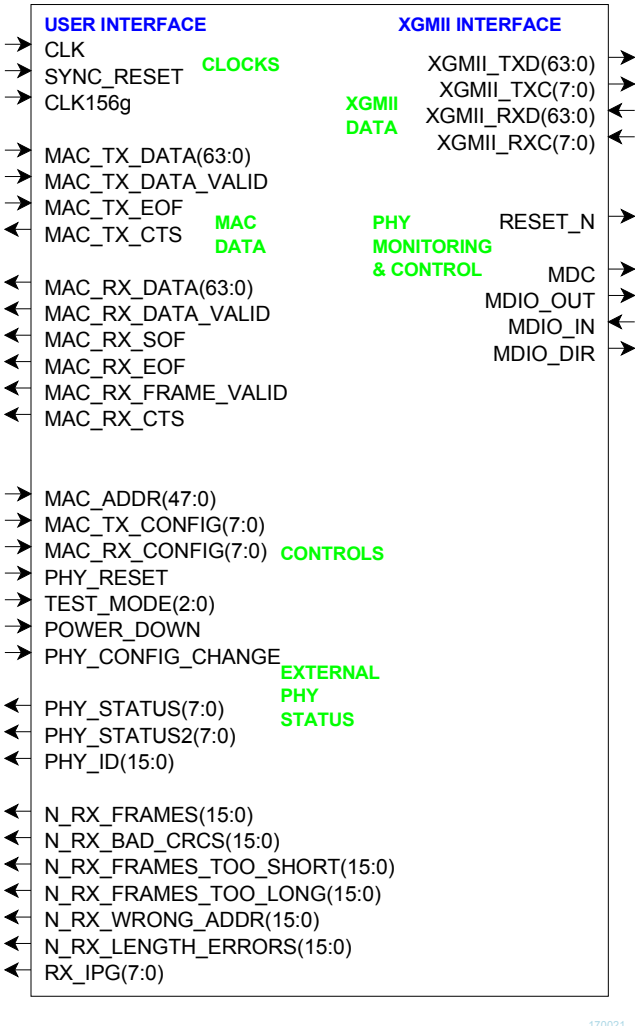
	XGMII only	XGMII + XAUI
Flip-Flops	1573	3305
LUTs	2016	3231
Block RAM/FIFO	0/8	0
DSP48A1s	0	0
GCLKs	2	1
DCMs/PLLs	0	1

PHY clock frequency: 156.25 MHz

FPGA Speed Grade

The code is compatible with Xilinx 7-series, -1 speed (slowest) for 10G operation with 156.25 MHz clock.

Interfaces

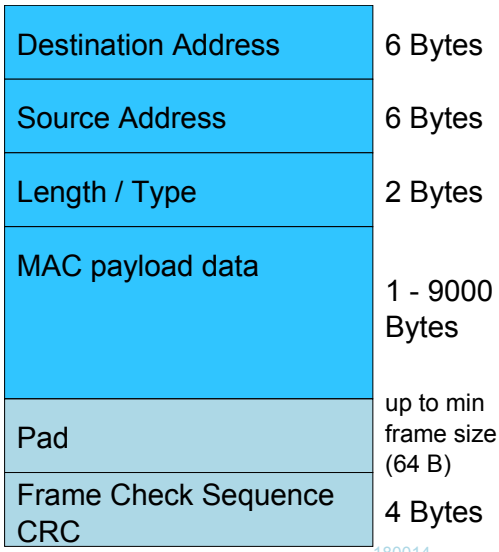


User Interface

The user interface comprises three primary signal groups: transmit data, receive data and monitoring & control. All signals are clock synchronous with a user-selected clock CLK (it does not have to be the same as the 156.25MHz PHY clock, although it generally is).

Elastic buffers can be included in both tx/rx directions at the user interface, at the user's discretion, either to cross clock domains from CLK to CLK156g, or for flow control reasons when one side of the interface is slower than the other.

In the Ethernet frame illustrated below, the user handles at least the dark blue section.

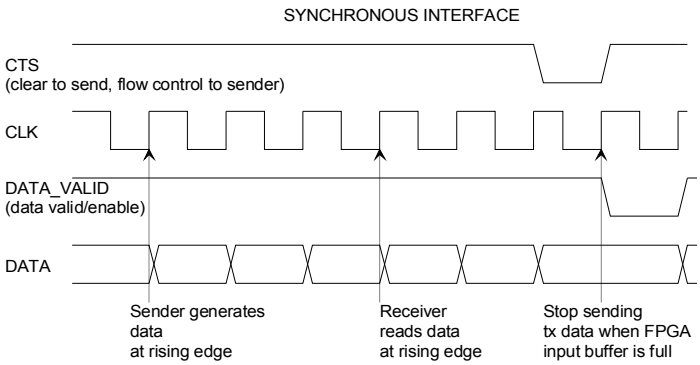


The software inserts the pad and frame check sequence (CRC) fields automatically unless disabled by the user.

The software then encapsulates the tx frame into an Ethernet Packet by adding a preamble, start of frame delimiter and extension as needed.

User Interface

MAC receive interface signals	*Description*
MAC_RX_DATA(63:0)	contains up to 8 data bytes. Byte order: LSB byte was received first. The first byte of a frame (Destination address) is always aligned with the 64-bit word LSB. Note: short-frame zero padding and 4-byte CRC are always passed to the user.
MAC_RX_DATA _VALID(7:0)	'1' for each meaningful byte in MAC_RX_DATA. For example: 0x03 when the two LSB bytes of MAC_RX_DATA have meaning. Only valid values are 0x00,01,03,07,0F,1F,3F,7F ,FF.
MAC_RX_SOF	1 CLK pulse marking the first word in a frame
MAC_RX_EOF	1 CLK pulse marking the last (partial) word in a frame
MAC_RX_FRAME_VALID	'1' when the current frame passed all validity checks including the CRC check. The entire frame validity is confirmed at the end of frame when MAC_RX_FRAME _VALID = '1' and MAC_RX_EOF = '1'.
MAC_RX_CTS	'Clear To Send' input. The user application drives this flow control signal to indicates that it is ready to accept received words at the next clock period. Set to '1' when the user application can handle the maximum throughput.
MAC transmit interface signals	*Description*
MAC_TX_DATA(63:0)	contains up to 8 data bytes. Byte order: LSB byte is transmitted first. The first byte of a frame (Destination address) must be aligned with the 64-bit word LSB.
MAC_TX_DATA _VALID(7:0)	'1' for each meaningful byte in MAC_TX_DATA. For example: 0x03 when the two LSB bytes of MAC_TX_DATA have meaning. Only valid values are 0x00,01,03,07,0F,1F,3F,7F ,FF.
MAC_TX_SOF	1 CLK pulse marking the first word in a frame
MAC_TX_EOF	1 CLK pulse marking the last (partial) word in a frame
MAC_TX_CTS	'Clear To Send' input. The MAC drives this flow control signal to indicates that it is ready to accept user words at the next clock period.



Throughout this document **CTS** refers to the flow control signal "**C**lear **T**o **S**end". CTS is generated by the data sink to indicate it can process and/or store incoming data.

XGMII Interface

The COM-5501SOFT interfaces with an external 10G Ethernet PHY through a standard XGMII Media Independent Interface using 64-bit wide data words.

An external PHY is managed via a two-wire standard MDIO interface. The state machine *PHY_CONFIG.vhd* is fairly generic, but the actual registers values are specific to the Microsemi VSC8486-11 PHY integrated circuits. For any other PHY integrated circuits, the configuration register values must be customized manually.

XAUI Interface

VHDL components are also included to perform the translation between XGMII and XAUI signals

Configuration

Pre-synthesis configuration parameters

The following configuration parameters are set prior to synthesis in the generic section of the *COM5501.vhd* component declaration.

Generic	*Description*
PHY IC MDIO address	The MDIO bus can be shared among several peripheral devices. The external 10G PHY is addressed through EXT_PHY_MDIO_ADDR
Receive Maximum Transmission Unit (MTU)	Maximum Ethernet payload size in Bytes. Typically 1500 Bytes for regular frames or 9000 Bytes for jumbo frames. A frame will be deemed invalid if its payload size exceeds this MTU value. Maximum: 16360 RX_MTU
Receive output buffer	'1' to instantiate a receive output buffer to cross clock domains and discard bad frames. '0' for very low latency operation (see the low latency section) RX_BUFFER When enabled, the buffer size is defined by its address width RX_BUFFER_ADDR_NBITS. Data width is always 74 bits. Example: when RX_BUFFER_ADDR_NBITS = 10, the receive buffer size is 74*2^10 = 75776 bits
User clock frequency	The user-supplied CLK serves as time reference for internal timers/delays. Declare the frequency in MHz (156 for 156.25 MHz, etc) CLK_FREQUENCY
Transmit Maximum Transmission Unit (MTU)	Maximum Ethernet payload size in Bytes. Typically 1500 Bytes for regular frames or 9000 Bytes for jumbo frames. Maximum: 16360 TX_MTU
Transmit output buffer	'1' to instantiate a transmit output buffer to cross clock domains and perform flow control. '0' for very low latency operation (see the low latency section) TX_BUFFER When enabled, the buffer size is defined by its address width TX_BUFFER_ADDR_NBITS. Data width is always 73 bits.
MAC control pause	Enable(1)/Disable(0) a short transmit pause upon receiving a MAC control PAUSE message. See 802.3-2015

	Clause 31. MAC_CONTROL_PAUSE_ENABLE

Run-time configuration parameters

The user can set and modify the following controls at run-time. All controls are synchronous with the user-supplied global CLK.

MAC transmit configuration	*Description*
Auto-padding	1 = Automatic padding of short frames. Requires that auto-CRC insertion be enabled too. 0 = Skip padding. User is responsible for adding padding to meet the minimum 60 byte payload size. MAC_TX_CONFIG (0)
Auto-CRC	1 = Automatic appending of 32-bit CRC at the end of the frame 0 = Skip CRC insertion. User is responsible for including the frame check sequence. MAC_TX_CONFIG(1)
MAC receive configuration	*Description*
MAC address	This network node 48-bit MAC address. The receiver checks incoming packets for a match between the destination address field and this MAC address. The user is responsible for selecting a unique 'hardware' address for each instantiation. Natural bit order: enter x0123456789ab for the MAC address 01:23:45:67:89:ab
Promiscuous mode	1 = all valid frames are accepted, regardless of their destination address. 0 = destination addresses are checked. MAC_RX_CONFIG(0)
Allow rx broadcast packets	0 = mark packets with the broadcast destination address FF:FF:FF:FF:FF:FF as invalid. 1 = accepts broadcast packets. MAC_RX_CONFIG(1)
Allow rx multi-cast packets	0 = mark packets with the multicast bit set in the destination address as invalid. 1 = accepts multicast packets. Destination addresses are identified as "multicast" when bit 0 of the destination most significant byte is '1'. For example 01:00:5E:xx:xx:xx or 33:33:xx:xx:xx:xx. MAC_RX_CONFIG(2)
Check MTU	1 = mark frames with payload sizes greater than the user-specified MTU size (typically 1500 Bytes, or 9000 Bytes for jumbo frames) as invalid. 0 = No payload size verification MAC_TX_CONFIG(4)
PHY configuration	*Description*
PHY test mode	00 = normal mode (default) 01 = loopback mode (at the phy) 10 = remote loopback 11 = led test mode
PHY reset	1 = PHY software reset, 0 = no reset
PHY power down	1 = power down enabled 0 = disabled

To enact any PHY configuration, a pulse must be sent to PHY_CONFIG_CHANGE.

MAC Receive Packets Check

The MAC receive section performs the following checks on the incoming packets:

- frame size >= 64 bytes
- frame size <= 1518, 1522, 9018 or 9022 bytes depending on the presence of IEEE 802.1Q field and whether the user allows Jumbo frames.
- destination address matches the user-specified MAC address, or
- destination address is a broadcast or multicast address
- Frame check sequence (CRC) is verified.

When a receive output buffer is instantiated (RX_BUFFER = '1'), bad frames are automatically discarded.

When no receive output buffer is instantiated (RX_BUFFER = '0'), the user is responsible for

discarding frames marked as invalid at the end of frame: MAC_RX_EOF = '1' and MAC_RX_DATA_VALID = '0'.

Low receive latency

Very low receive latency (4 clock periods = 25.6ns) can be achieved on the receive path. This requires

- Not instantiating a receive output buffer: set RX_BUFFER = '0'
- Using the same 156.25 MHz synchronous clock for the PHY side (CLK156g) and user side (CLK)
- letting the user keep or discard the received frame at the end of frame. The COM5501.vhd component identifies any invalid frame at the end of frame when MAC_RX_EOF = '1' and MAC_RX_DATA_VALID = '0'.

Exclusions

-

Software Licensing

The COM-5501SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable corporate license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bitstream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Reference documents

[1] IEEE Std. 802.3™-2015
Relevant clauses:

- Clause 3: MAC frame and packet specifications
- Clause 4: Media Access Control
- Clause 31: MAC control pause

[2] Xilinx XAUI IP core, v12.2, Vivado design guide, PG053

[3] ComBlock COM-1800 FPGA + DDR3 SODIMM development platform
http://www.comblock.com/com1800.html

[4] ComBlock COM-5104 10Gbits/s Ethernet Transceivers
http://www.comblock.com/com5104.html

Configuration Management

The current software revision is 3.

Directory	Contents
/	Project files for various Xilinx ISE versions.
/doc	Specifications, user manual, implementation documents
/src	.vhd source code, .ucf constraint files, .pkg packages. One component per file.
/sim	Test benches
/bin	.ngc, .bit, .mcs configuration files
/use_example	use example for Xilinx Artix-7 FPGA with XAUI interface to a Microsemi 10G Ethernet PHY (VSC8486-11)

VHDL development environment

The VHDL software was developed using the following development environment:

Xilinx Vivado v2019 for synthesis and VHDL simulation.

Ready-to-use Hardware

Ready-to-use binary is included in the /bin folder for use on the following Comblock hardware modules:

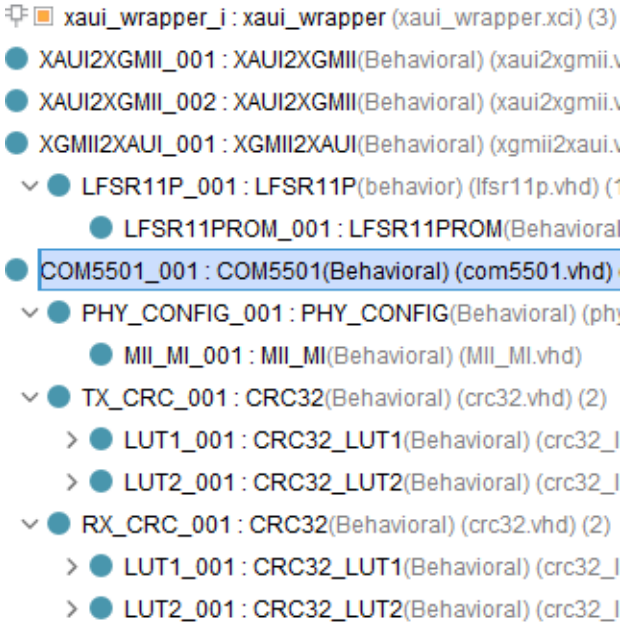
- COM-1800 Xilinx Artix7-100T FPGA + DDR3 SODIMM + ARM development platform
- COM-5104 single-Port 10G Ethernet Transceiver

The relevant hardware schematics can be downloaded from
comblock.com/download/com_1800schematics.pdf
comblock.com/download/com_5104schematics.pdf

Acronyms

Directory	Contents
CTS	Clear To Send (flow control signal)
LSB	Least Significant Byte in a word
MSB	Most Significant Byte in a word
MTU	Maximum Transmission Unit (frame length)
RX	Receive
TX	Transmit

Top-Level VHDL hierarchy



The code is stored with one, and only one, component per file.

The root entity (highlighted above) is *COM5501.vhd*. It comprises the tx and rx elastic buffers, tx state machine and tx packet construction.

The root also includes the following components:

- The *PHY_CONFIG.vhd* component to configure the PHY.
- The *CRC32.vhd*, instantiated twice, computes the CRC32 to be appended to tx packets and to check rx. The CRC32 computation is performed 64 data bits at a time for a maximum throughput of 10Gbits/s. This is the most time-critical circuit.

The components *XGMII2XAUI.vhd* and *XAUI2XGMII.vhd* translate the XGMII signals into a 4-lane XAUI interface. These are only needed when the FPGA transceiver speed is not sufficient to reach 10 Gbits/s (for example Xilinx Artix-7). The 10Gbits/s throughput is achieved through 4 parallel transceivers operating at 3.125 GHz.

Clock / Timing

The software uses one or two global clocks:

- A 156.25 MHz clock (CLK156g) generated by the PHY.
- A user-supplied interface clock (CLK) to read and write packets from/to the MAC. CLK frequency can be independent of the PHY clock but should be high enough to support the expected data throughput. Using the same 156.25 MHz clock for the PHY and the MAC user helps minimize latency. See Low receive latency

Quick Start

This section describes a few tips to quickly establish a working, albeit simple, baseline.

Quick start using ComBlock modules

The purpose is to load the ready-to-use FPGA configuration for Ethernet MAC into off-the-shelf hardware consisting of a COM-1800 FPGA development platform and a COM-5104 plug-in 10G Ethernet adapter. The associated source code is in the folder /use_example/src/.

Connect the SFP+ transceiver and the fiber/coax LAN cable between the ComBlock SFP+ connector and a PC.

FPGA programming:
Connect a USB cable between a PC and the COM-1800. Power up the assembly. From the ComBlock Control Center software, detect the modules  .

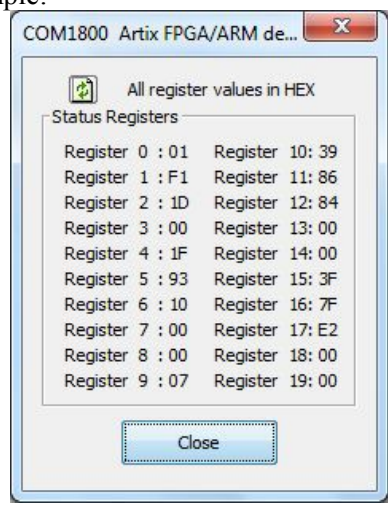
Click on the swiss army knife button  and program the ready-to-use FPGA firmware COM1800_TOP.bit located in /use_example/bin/

FPGA configuration:
From the ComBlock Control Center, click on the settings button  and make sure all control registers are set to 00.

LINK check: LED D2 will blink upon receiving Ethernet frames, whereas LED D3 will blink upon transmitting.

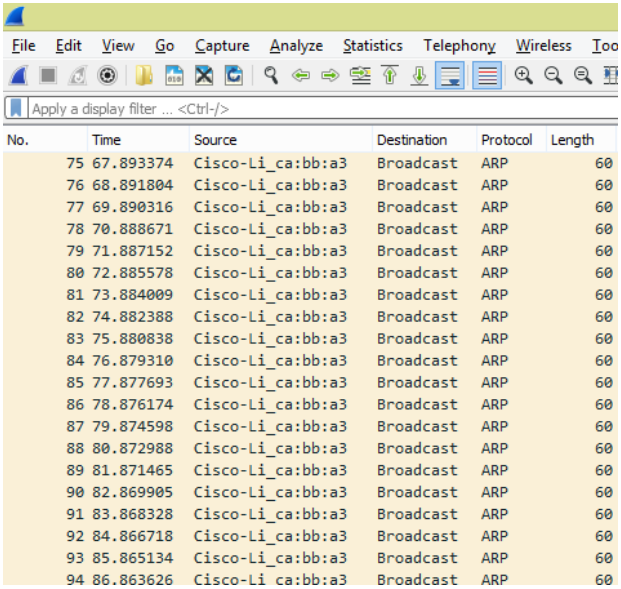
Receive check:
From the ComBlock Control Center, click on the  status button.
A description of the status registers is found here.

For example:



Start a LAN analyzer like Wireshark on the PC.

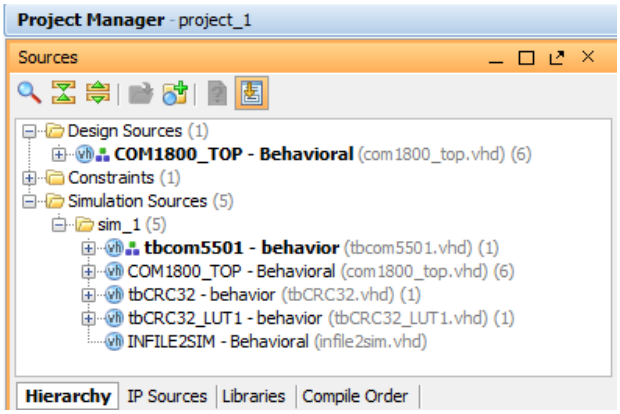
Transmit check: the LAN analyzer will detect short broadcast messages sent by the ComBlock once every second. This frame is defined in the *COM1800_TOP.vhd* component.



Quick start with VHDL simulation

Several testbenches located in the /sim directory can be used to validate the VHDL code. Some focus on detailed areas (CRC32, MDIO timing, PHY configuration), while others create stimulus to exercise the entire Ethernet MAC.

The easiest way to start is to use the Xilinx Vivado tools which include a VHDL simulator.



Under "Simulation Sources", highlight one of the testbenches, right-click "Set as top" and click on the run simulation button.

For example, the tbCOM5501.vhd testbench sends an Ethernet frame to the XGMII where it is looped back. This allows one to visualize the PHY interface signals, padding and CRC insertion by the MAC layer and the frame verification upon reception.

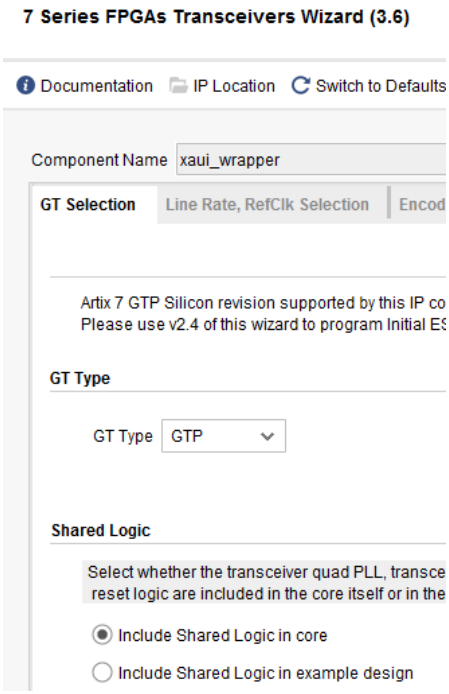
The SIMULATION constant (typically at the tope level) should be set to '1' to enable configurations specific to the VHDL simulation, shorten long timers for example. These constants should revert to '0' prior to synthesis.

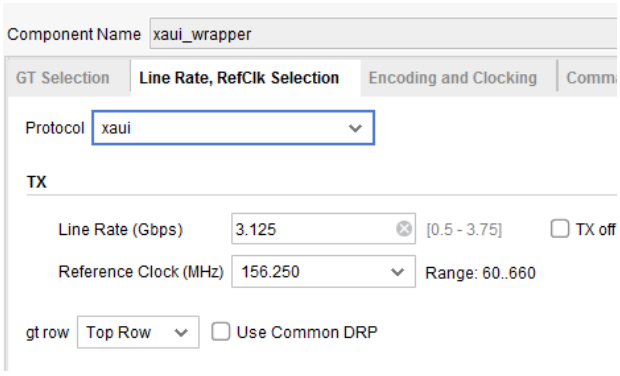
Xilinx-specific code

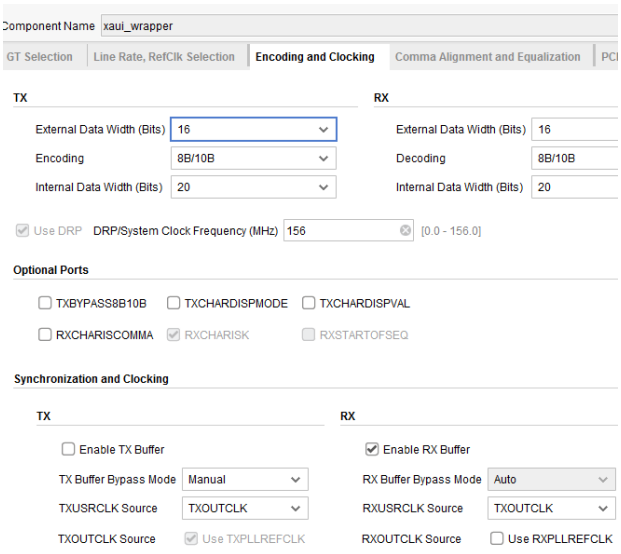
The VHDL source code between the XGMII interface and the MAC user interface is written in generic VHDL and is thus portable to any FPGA capable of sustaining the 156.25 MHz clock speed.

The component between the XAUI interface and the external PHY is FPGA-specific. The code example uses the Xilinx 7 series transceivers IP core configured as XAUI and is thus specific to the 7-series Xilinx family of FPGAs.

For Vivado 2019, the Xilinx 7 series transceivers core is configured as follows:

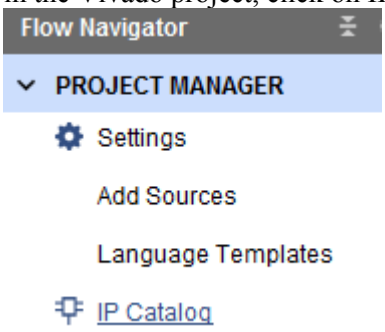




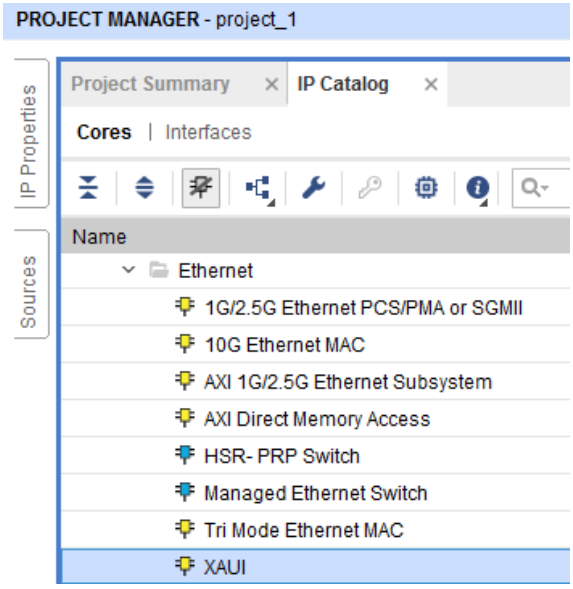


For Vivado 2018.3 and earlier, the Xilinx XAUI core is configured as follows:

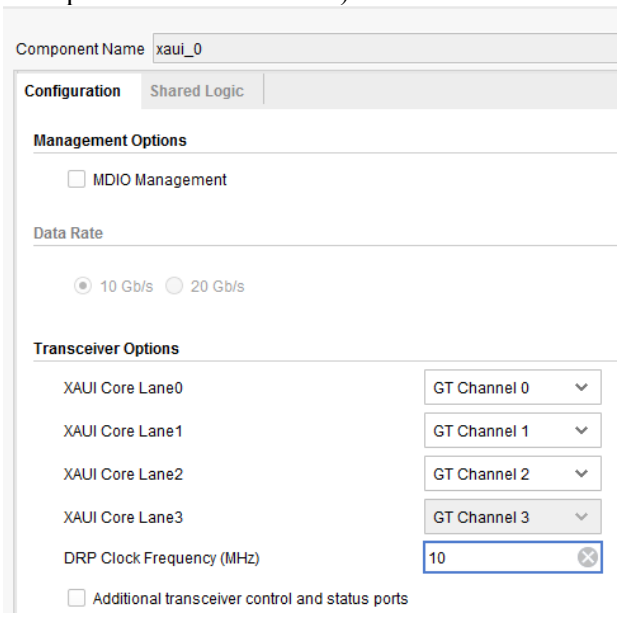
1. in the Vivado project, click on IP Catalog



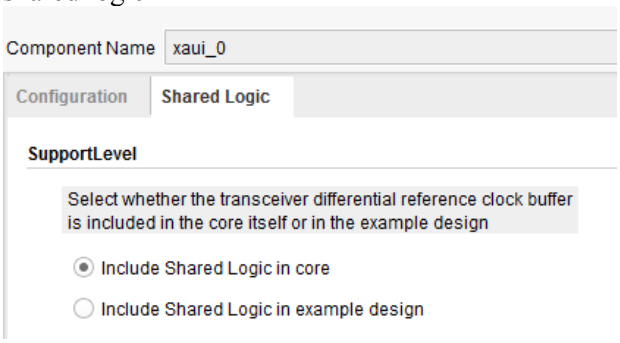
2. In the IP Catalog, select the Communication & Networking | Ethernet | XAUI core



3. Customize the XAUI core. Select the DCLK dedicated clock frequency to be the FPGA reference oscillator frequency (in the example code 10 MHz clock)



4. In the shared logic tab, select "include shared logic"



5. OK to complete the configuration.

6. Open \project_1\project_1.ip_user_files\ip\xaui_0 \xaui_0.vho to cut and paste the component declaration and component instantiation into the VHDL top level.

```
------------ Begin Cut here for COMPONENT Declaration
COMPONENT xaui_0
  PORT (
    dclk : IN STD_LOGIC;
    reset : IN STD_LOGIC;
    clk156_out : OUT STD_LOGIC;
------------ Begin Cut here for INSTANTIATION Template
your_instance_name : xaui_0
  PORT MAP (
    dclk => dclk,
    reset => reset,
    clk156_out => clk156_out,
```

Use example

A Xilinx Vivado project is provided in the /use_example/project_1/ folder. It serves two purposes:
(a) as a VHDL source code example, and
(b) as ready-to-use code on the ComBlock COM-1800 + COM-5104 development platforms.

The ComBlock control center provides a Graphical User Interface to set control registers and monitor status.

Control registers

Parameters	Configuration
Internal/External frequency reference	0 = internal TCXO as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J6 coaxial connector as frequency reference. CREG0(7)
XGMII local loopback	1 = loopback the XGMII transmit words to the XGMII receive input in the Xilinx 0 = no loopback CREG1(0)
PHY local loopback	1 = loopback the transmit path to the receive input at the PHY 0 = no loopback CREG1(1)
PHY power down	CREG1(4)
PHY soft reset	CREG1(6)

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: 01 F1 1D xx 1F 93 10 00 00 07.
10G transceiver status	bit0: LASI bit1: RXALARM bit2: TXALARM bit3: SFP+ALARM bit4: power good +1.2V bit5: power good +3.3V Expecting 0x3F SREG(10)
10G transceiver PHY ID	VSC8486-11 PHY ID read over MDIO. Expecting 0x8486 SREG11(LSB) -SREG12(MSB)
10G transceiver SFP+ status	Expecting 0x0F SREG13
10G transceiver XAUI status	bit0: all PHY XAUI rx lanes in sync bit1: PHY XAUI rx PLL in lock bit2: PHY XAUI rx lane0 signal present bit3: PHY XAUI rx lane1 signal present bit4: PHY XAUI rx lane2 signal present bit5: PHY XAUI rx lane3 signal present Expecting 0x3F SREG14
FPGA XAUI status	bit5: FPGA XAUI receiver is synchronized across all 4 lanes Expecting 0x20 SREG15
Number of received frames	16-bit counter SREG17(LSB)-SREG18(MSB)
Number of frames with bad CRC	16-bit counter SREG19(LSB)-SREG20(MSB)
Inter Packet Gap	InterPacket Gap (in Bytes) between the last two successive packets (min is typically 12 Bytes, but can be as low as 5 Bytes for 10G) SREG21
Local MAC address	Displays the 48-bit MAC address generated from the FPGA DNA_ID. SREG22(MSB)-27(LSB)

ComBlock Compatibility List

FPGA development platform
COM-1800 FPGA + DDR3 SODIMM socket + GbE + ARM development platform
Network adapter
COM-5104 1-port 10 Gigabit Ethernet Transceiver
Software
COM-5502SOFT Low-latency IP/TCP Server/UDP for 10G Ethernet, VHDL Source / IP Core
COM-5503SOFT Low-latency IP/TCP Client/UDP for 10G Ethernet, VHDL Source / IP Core

ComBlock Ordering Information

COM-5501SOFT 10G Ethernet MAC, VHDL SOURCE CODE

ECCN: EAR99

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