**UB Commencement System**

**(UB CommenceSys)**

Technical Manual

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# Chapter 1

## Functional Overview

This chapter describes the functional overview of the alarm clock. It contains the following sections:

* + *About the System…………………………………………………………… 1.1*
  + *Architectural Overview …………………………………………………… 1.2*
  + *Features ……………………………………………………………… 1.3*
  + *Parts List…… ……………………………………………………………… 1.4*
  + *Circuit Diagram …………………………………………………………… 1.5*

### 1.1 About

### 1.2 Architectural Overview

This unit consists of

### 1.3 Features

### 1.4 Parts List

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Part** | **Qty** | **Manufacturer** | **Manu. Part #** | **Picture** | **Description** |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

1.5 Circuit Diagram

The following figure shows the basic circuit diagram…

**Figure 1.2 – Circuit Diagram**

# Chapter 2

## Memory

This chapter describes the memory overview of the system. It contains the following sections:

* *Memory Map Overview …………………………………………………… 2.1*
  + *Other AHB Peripherals Map …………………………………… 2.1.1*
  + *APB Peripheral Map …………………………………………… 2.1.2*
* *SRAM ………………………………………………………………………… 2.2*
* *ROM ………………………………………………………………………… 2.3*
* *Memory Control Logic Diagram ………………………………………… 2.4*

[4]

### 2.1 title

The

#### 2.1.1 Subsection

#### 2.1.2 Subsection

The

#### 2.1.3 Subsection

A

### 2.2 title

On-chip SRAM may be used for code and/or storage. The 2MB of SRAM may be accessed as byte-addressed memory. Word and halfword accesses to the memory ignore the alignment of the address and access the naturally-aligned value that is addressed (so a memory access ignores address bits 0 and 1 for word accesses, and ignores bit 0 for halfword accesses). Therefore valid reads and writes require data accessed as halfwords to originate from addresses with address line 0 being 0 (addresses ending with 0, 2, 4, 6, 8, A, C, and E in hexadecimal notation) and data accessed as words to originate from addresses with address lines 0 and 1 being 0 (addresses ending with 0, 4, 8, and C in hexadecimal notation). This rule applies to both off and on-chip memory usage.

### 2.3 title

The on-chip ROM beginning at memory address 0x00000000 and spans XXXMB.

### 2.4 title

# Chapter 3

## Chapter Title

This chapter describes the functions…..:

* *Block Diagram …………………………………………………… 3.1*

### 3.1 TITLE

The

#### 3.2.1 subtitle:

The

#### 3.2.2 subtitle:

The

# Chapter 4

## Chapter Title

This chapter describes…….

### 4.1 Title

#### 4.1.1 Subtitle

Four

#### 4.1.2 Subtitle

#### 4.1.3 Subtitle

The

# Chapter 5

## Chapter Title

This chapter offer an example of ……... It contains the following sections:

* ….…………………………………………… 5.1
  + ………………..…………………. 5.1.1
  + ……………………..……………. 5.1.2
  + ……………………….………… 5.1.3

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### 5.1 Title

#### 5.1.1 subtitle

This

#### 5.1.2 subtitle

The

#### 5.1.3 subtitle

This

### 5.2 Title

[34]