CSC 220

Computer Organization

Final Lab Project

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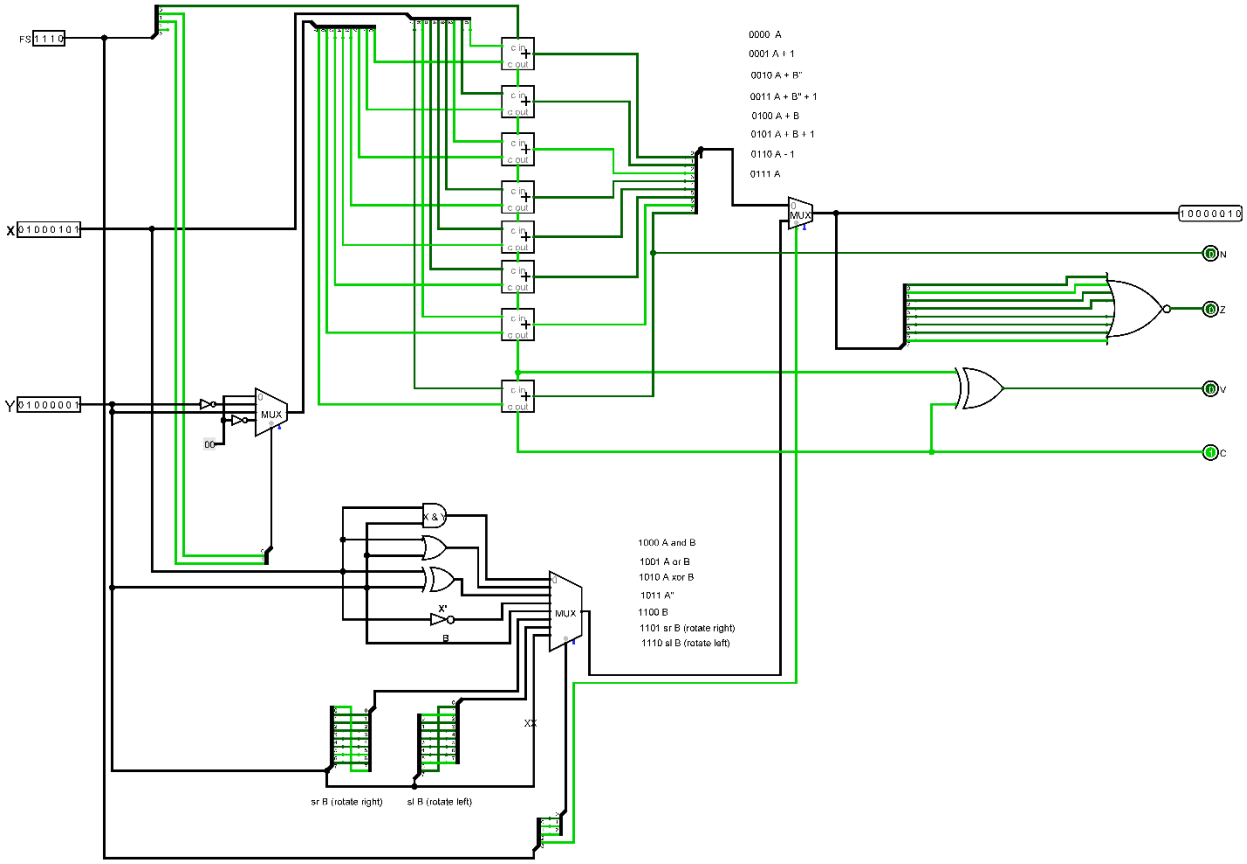
- Introduction:
  For this final lab project, I will design and implement an 8-bit Arithmetic Logic Unit with a shifter using Logisim. This project will put in the knowledge and skills I have gained from all the previous labs, including working with combinational and sequential circuits. The goal is to demonstrate my understanding of how to build and simulate a complex digital system.

- Project:


FS 1110
X 01000101
Y 01000001
MUX
00
0000 A
0001 A + 1
0010 A + B'
0011 A + B' + 1
0100 A + B
0101 A + B + 1
0110 A - 1
0111 A
MUX
10000010
N
Z
V
C
X & Y
X'
B
1000 A and B
1001 A or B
1010 A xor B
1011 A'
1100 B
1101 sr B (rotate right)
1110 sl B (rotate left)
MUX
XX
sr B (rotate right)
sl B (rotate left)

- Test Cases:

S3	S2	S1	S0	Operations	X	Y	F	C	V	N	Z
0	0	0	0	F = A	0000 0011	-	0000 0011	0	0	0	0
0	0	0	1	F = A + 1	0000 0011	-	0000 0100	0	0	0	0
0	0	1	0	F = A + B’	0000 0011	0000 0010	0000 0000	1	0	0	1
0	0	1	1	F = A + B’ + 1	0000 0011	0000 0010	0000 0001	1	0	0	0
0	1	0	0	F = A + B	0000 0011	0000 0010	0000 0101	0	0	0	0
0	1	0	1	F = A + B + 1	0000 0011	0000 0010	0000 0110	0	0	0	0
0	1	1	0	F = A – 1	0000 0011	-	0000 0001	1	0	0	0
0	1	1	1	F = A	0000 0011	-	0000 0011	0	0	0	0
1	0	0	0	F = A and B	0000 0011	0000 0010	0000 0010	-	-	-	-
1	0	0	1	F = A or B	0000 0011	0000 0010	0000 0011	-	-	-	-
1	0	1	0	F = A xor B	0000 0011	0000 0010	0000 0001	-	-	-	-
1	0	1	1	F = A’	0000 0011	-	1111 1100	-	-	-	-
1	1	0	0	F = B	-	0000 0010	0000 0010	-	-	-	-
1	1	0	1	F = sr B	-	0000 0010	0000 0001	-	-	-	-
1	1	1	0	F = sl B	-	0000 0010	0000 0100	-	-	-	-

Discussion:

with this being our last lab I have gained a lot of experience and now am able to design and illustrate a combination circuit and sequential circuits and also I can arithmetic logic unit and a shifter with help of my professional professor doctor MOHAMMAD WAKIL AHMED.