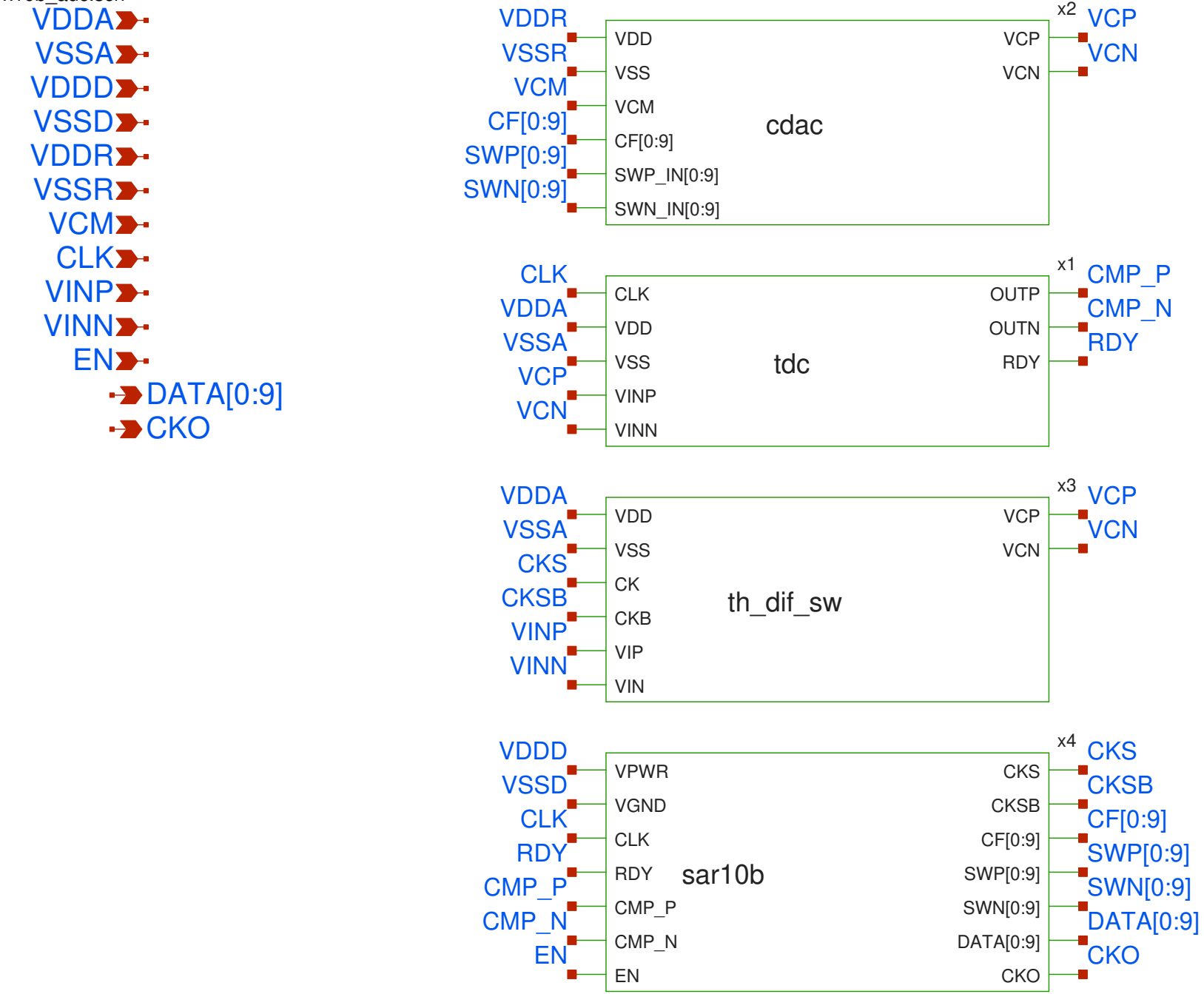
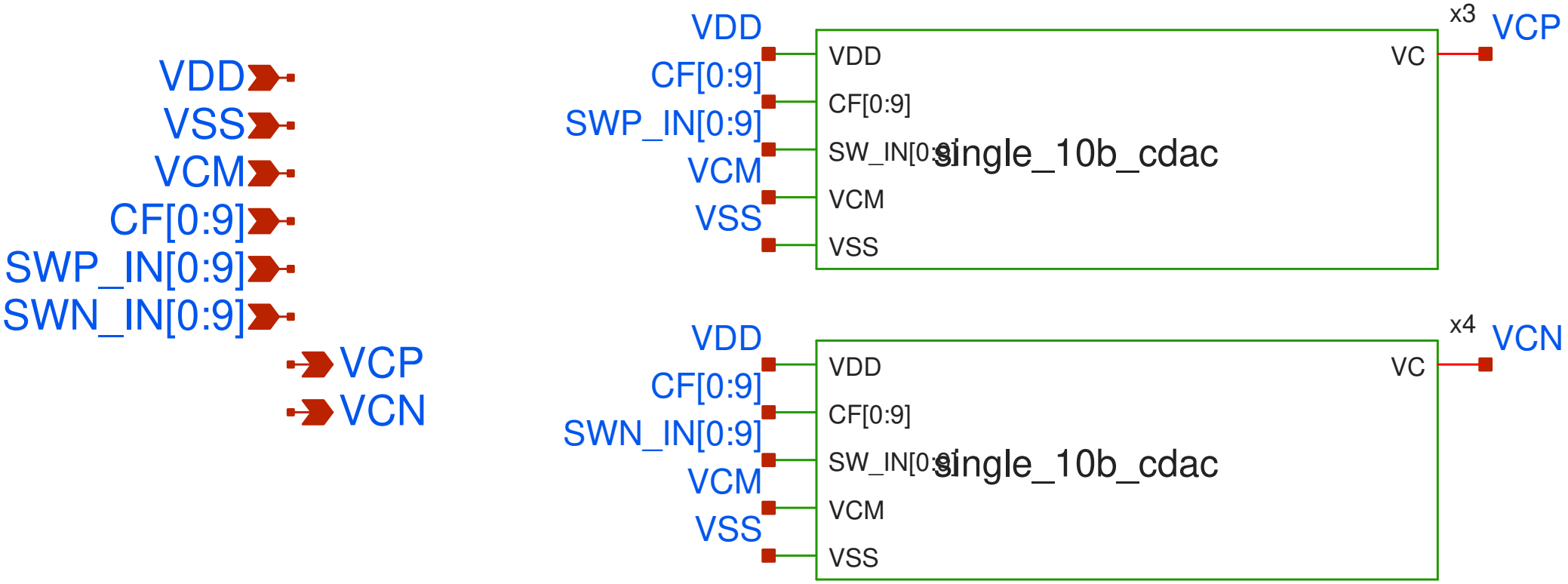
x10b_adc.sch



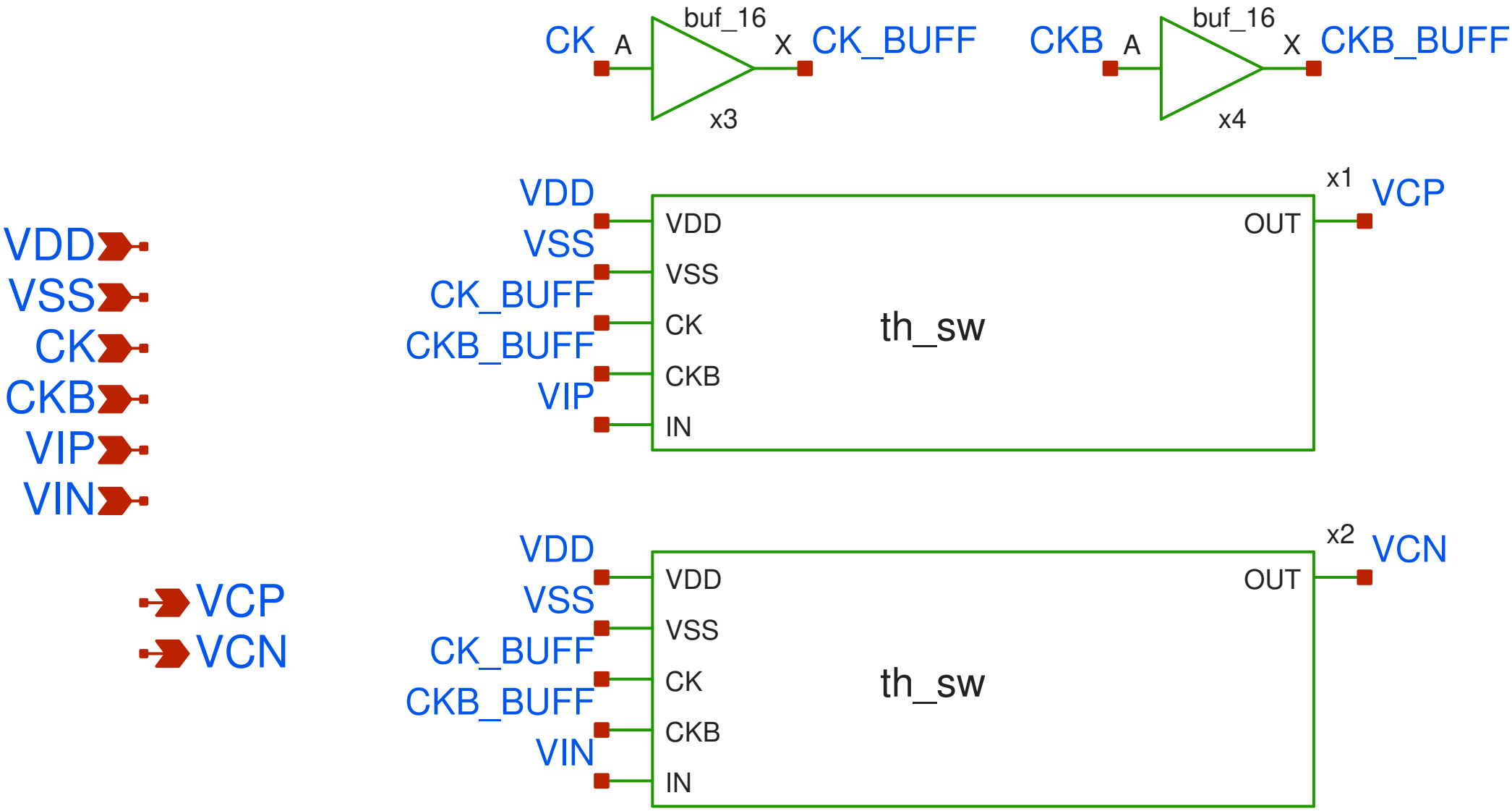
s1

```
.include /usr/local/share/pdk/sky130A/libs.ref/sky130_fd_sc_hs/spice/sky130_fd_sc_hs.spice
```

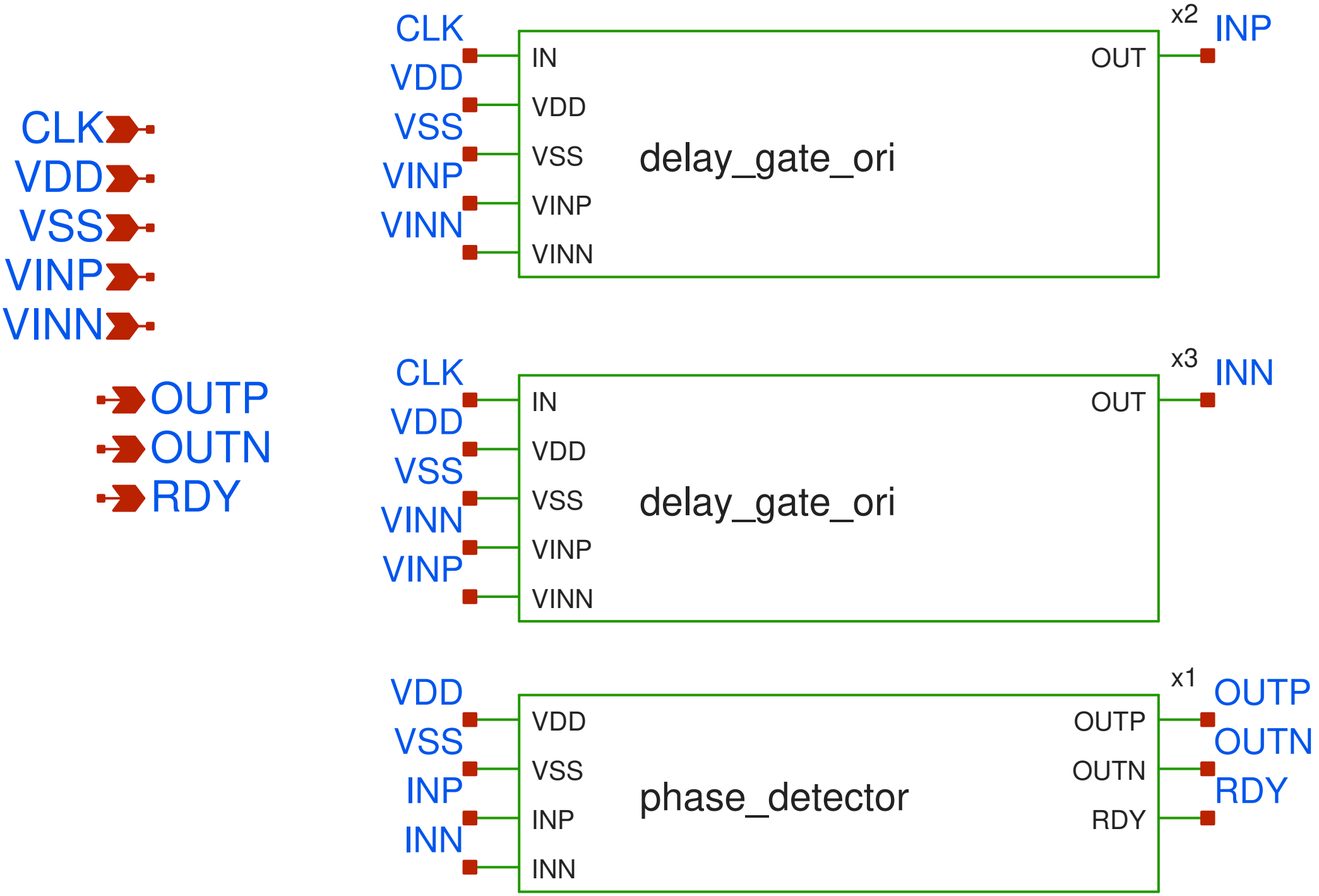
cdac.sch


VDD
VSS
VCM
CF[0:9]
SWP_IN[0:9]
SWN_IN[0:9]
VCP
VCN
VDD
CF[0:9]
SWP_IN[0:9]
VCM
VSS
VDD
CF[0:9]
SW_IN[0:9]
VCM
VSS
single_10b_cdac
VC
x3
VCP
VDD
CF[0:9]
SWN_IN[0:9]
VCM
VSS
VDD
CF[0:9]
SW_IN[0:9]
VCM
VSS
single_10b_cdac
VC
x4
VCN

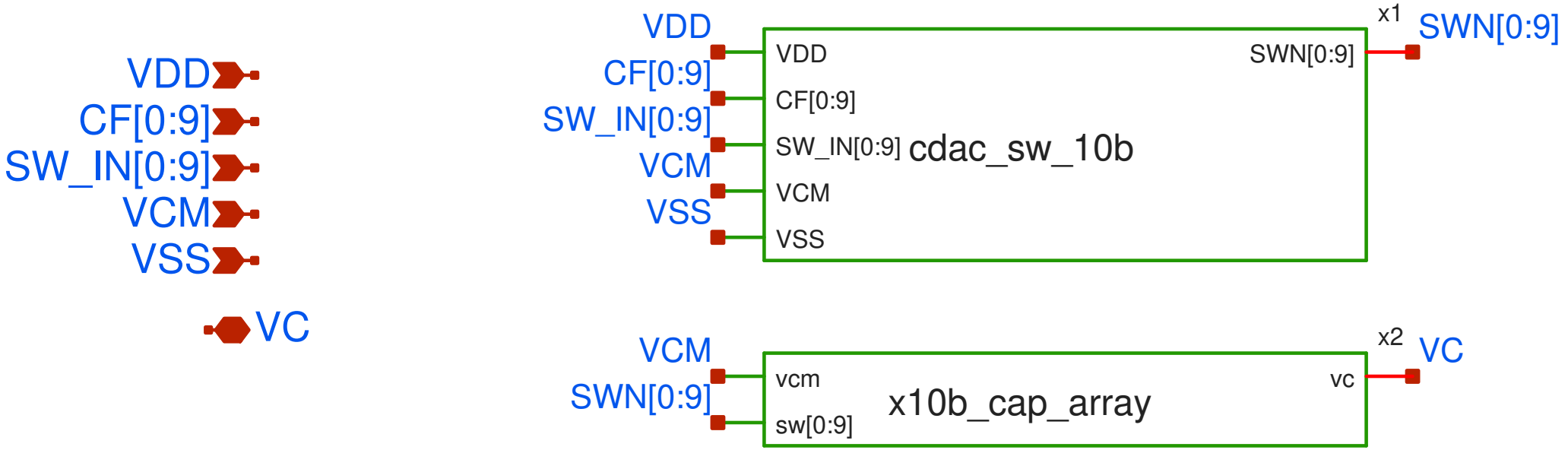
th_dif_sw.sch


CK
A
buf_16
X
CK_BUFF
x3
CKB
A
buf_16
X
CKB_BUFF
x4
VDD
VSS
CK
CKB
VIP
VIN
VDD
VSS
CK_BUFF
CKB_BUFF
VIP
VDD
VSS
CK_BUFF
CK
CKB
IN
th_sw
OUT
x1
VCP
VCP
VCN
VDD
VSS
CK_BUFF
CKB_BUFF
VIN
VDD
VSS
CK_BUFF
CK
CKB
IN
th_sw
OUT
x2
VCN

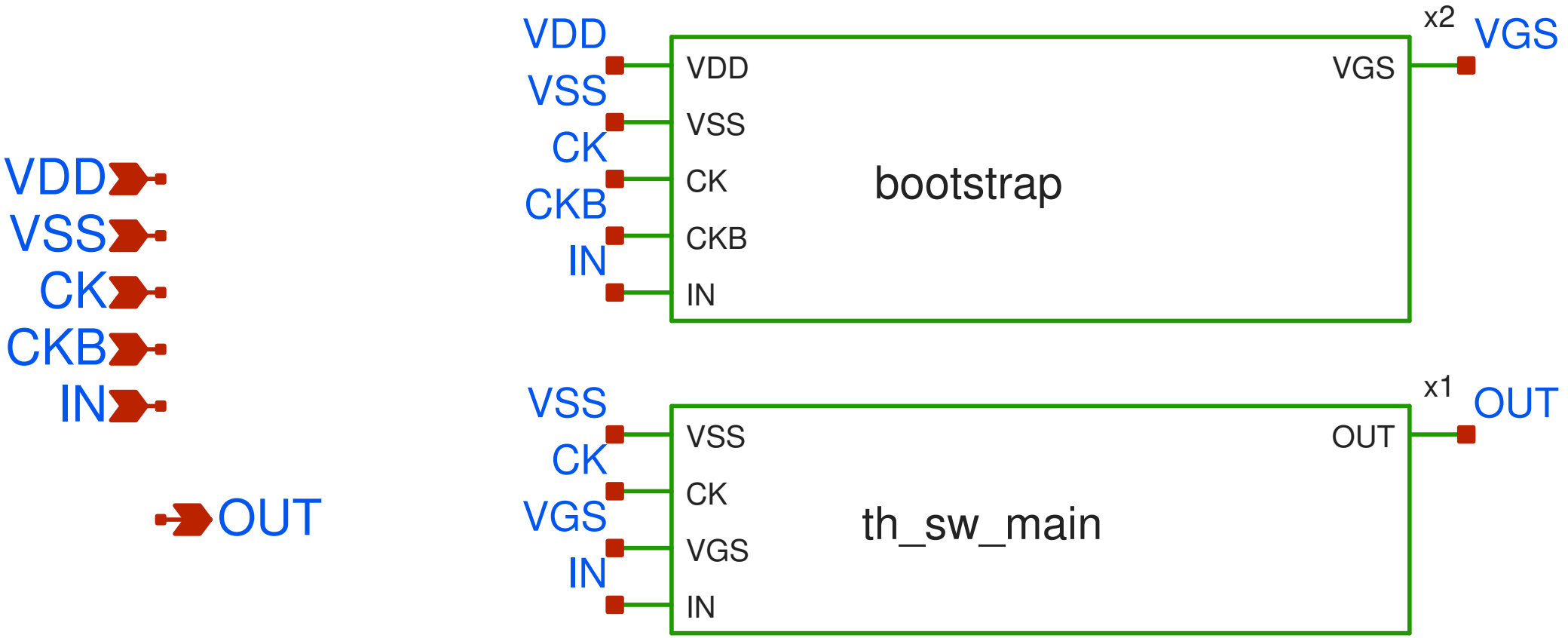
tdc.sch


CLK
VDD
VSS
VINP
VINN
OUTP
OUTN
RDY
CLK
VDD
VSS
VINP
VINN
IN
VDD
VSS
VINP
VINN
delay_gate_ori
OUT
x2
INP
CLK
VDD
VSS
VINN
VINP
IN
VDD
VSS
VINP
VINN
delay_gate_ori
OUT
x3
INN
VDD
VSS
INP
INN
VDD
VSS
INP
INN
phase_detector
OUTP
OUTN
RDY
x1
OUTP
OUTN
RDY

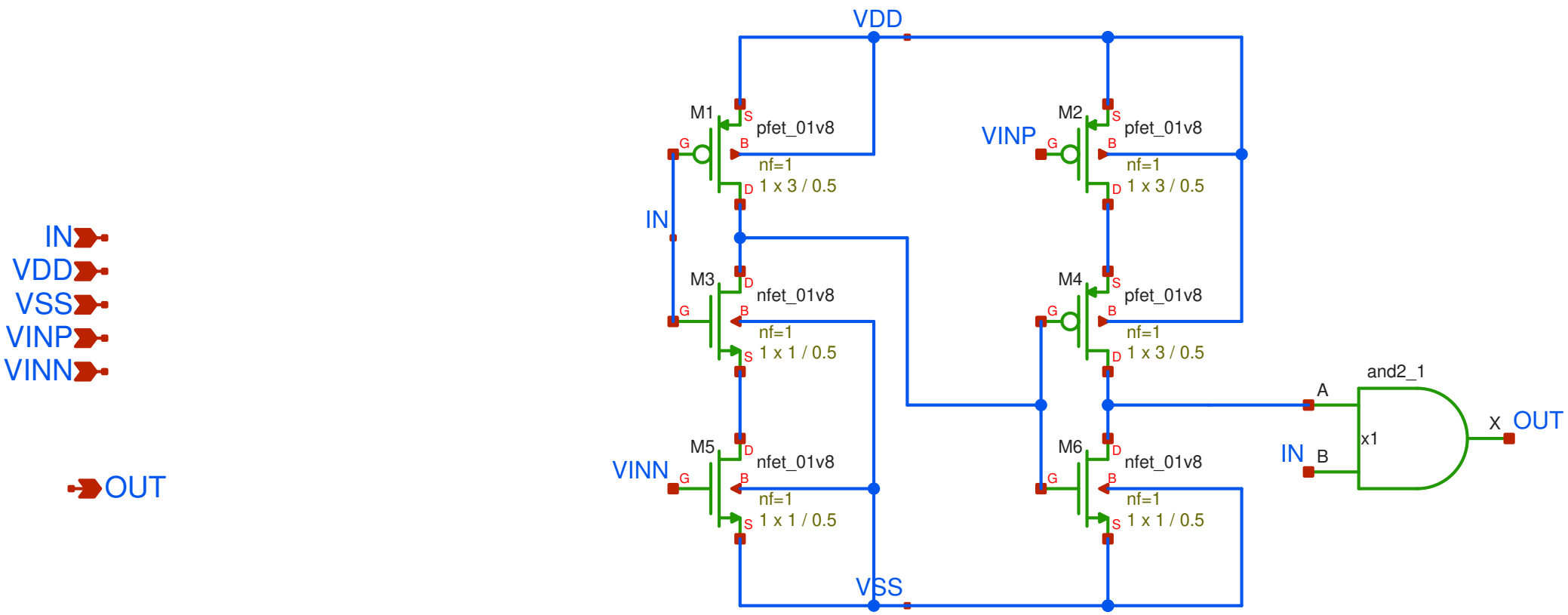
single_10b_cdac.sch

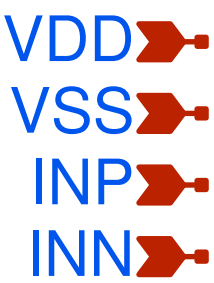


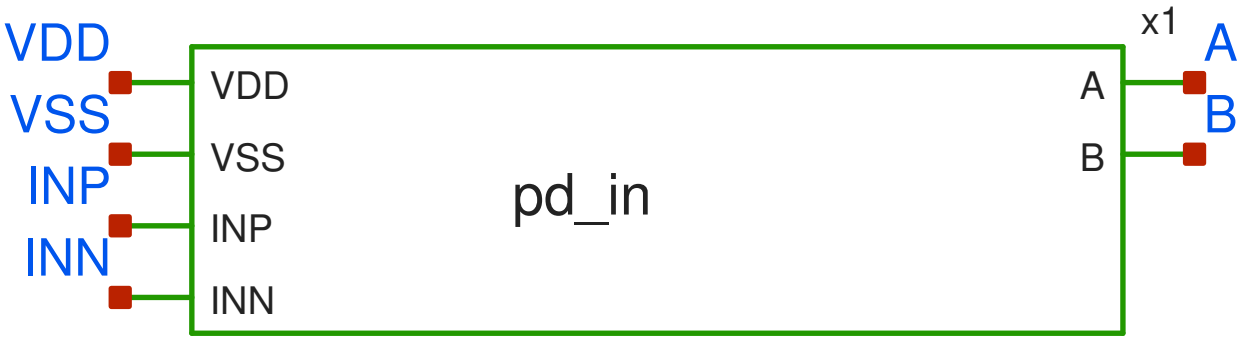
th_sw.sch


VDD
VSS
CK
CKB
IN
OUT
VDD
VSS
CK
CKB
IN
VDD
VSS
CK
CKB
IN
bootstrap
x2
VGS
VGS
VSS
CK
VGS
IN
VSS
CK
VGS
IN
th_sw_main
x1
OUT
OUT

delay_gate_ori.sch



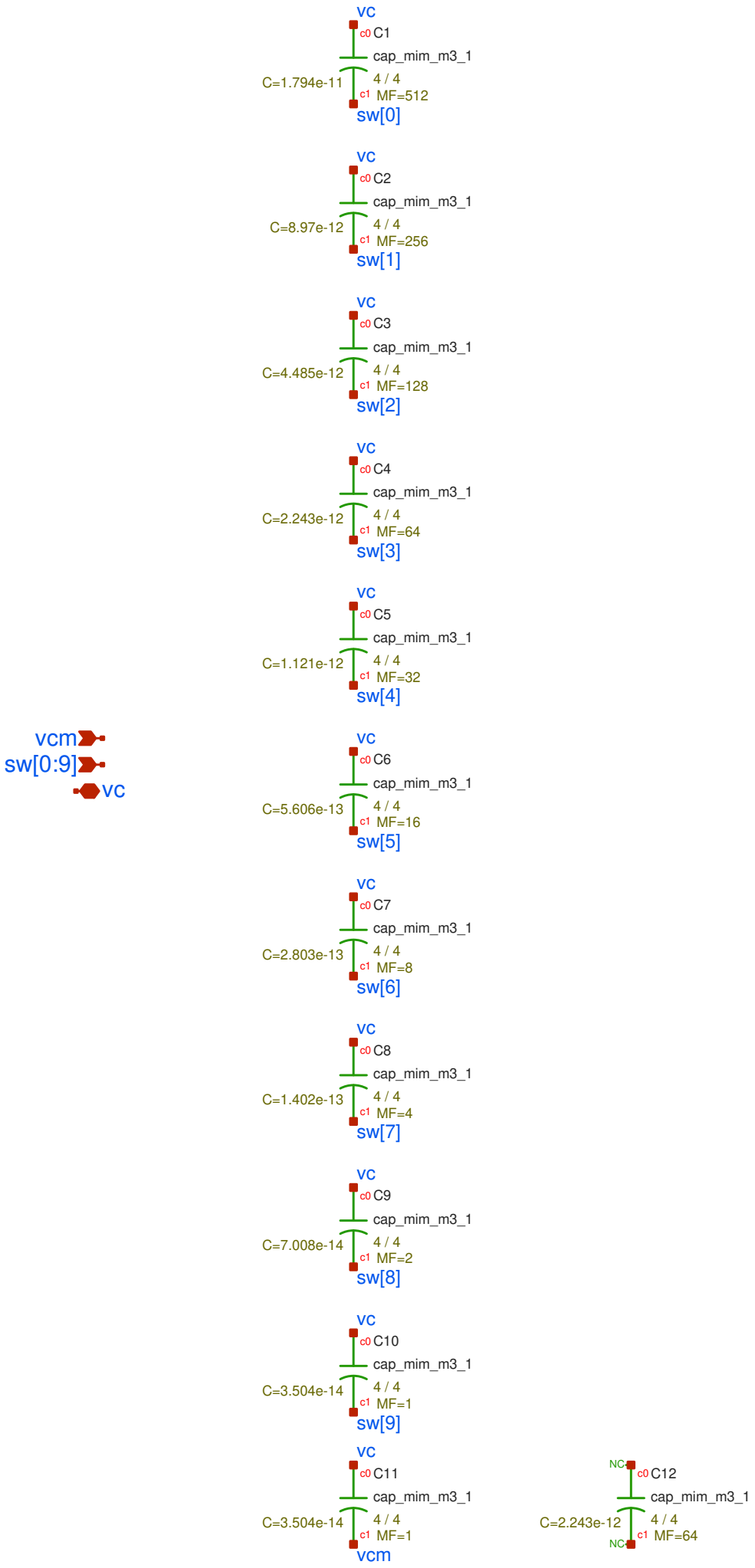

VDD
VSS
INP
INN


VDD
VSS
INP
INN
VDD
VSS
INP
INN
pd_in
x1
A
B
A
B

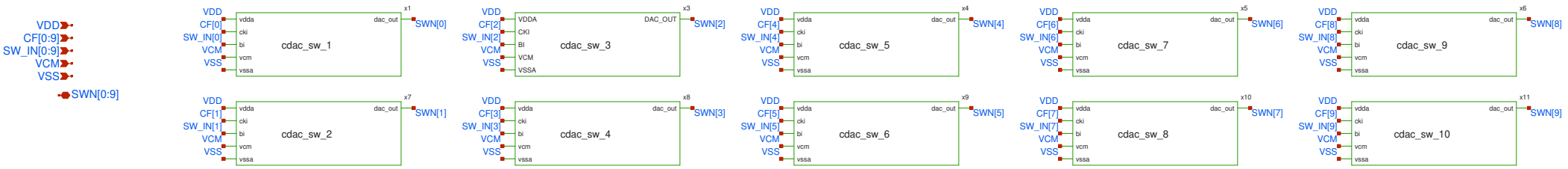
OUTP
OUTN
RDY

VDD
VSS
A
B
VDD
VSS
A
B
pd_out
x2
OUTP
OUTN
RDY
OUTP
OUTN
RDY

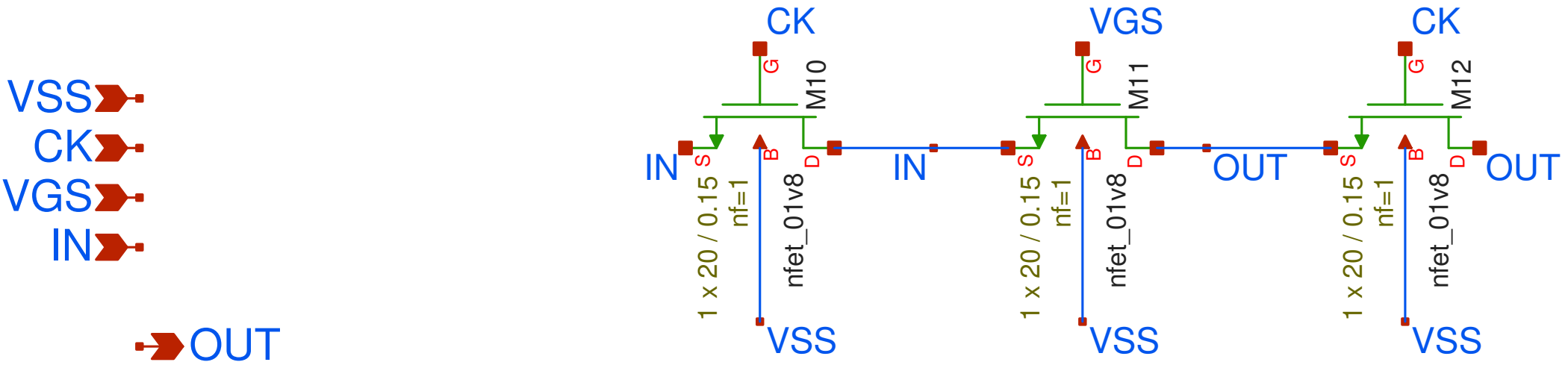
x10b_cap_array.sch



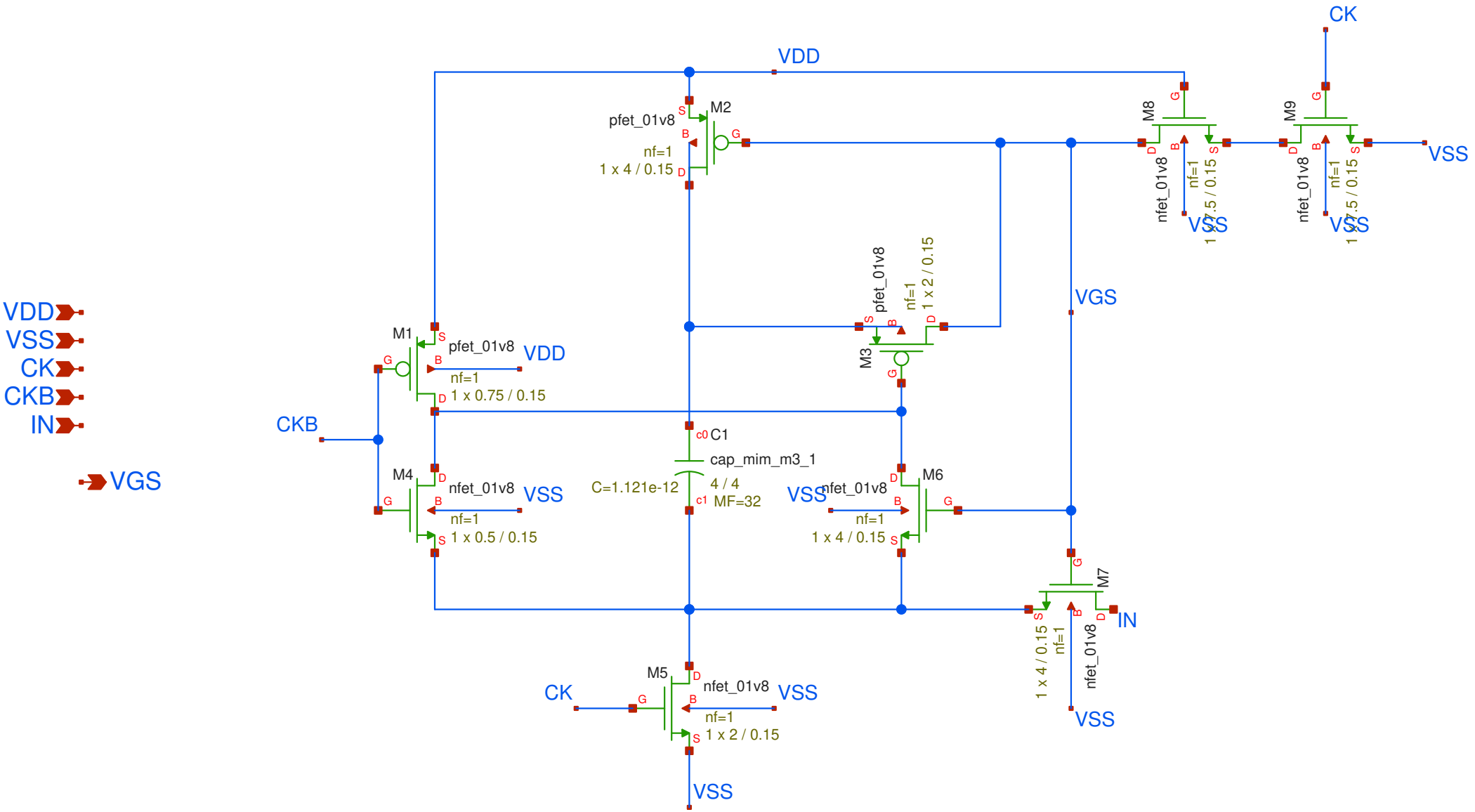
cdac_sw_10b.sch



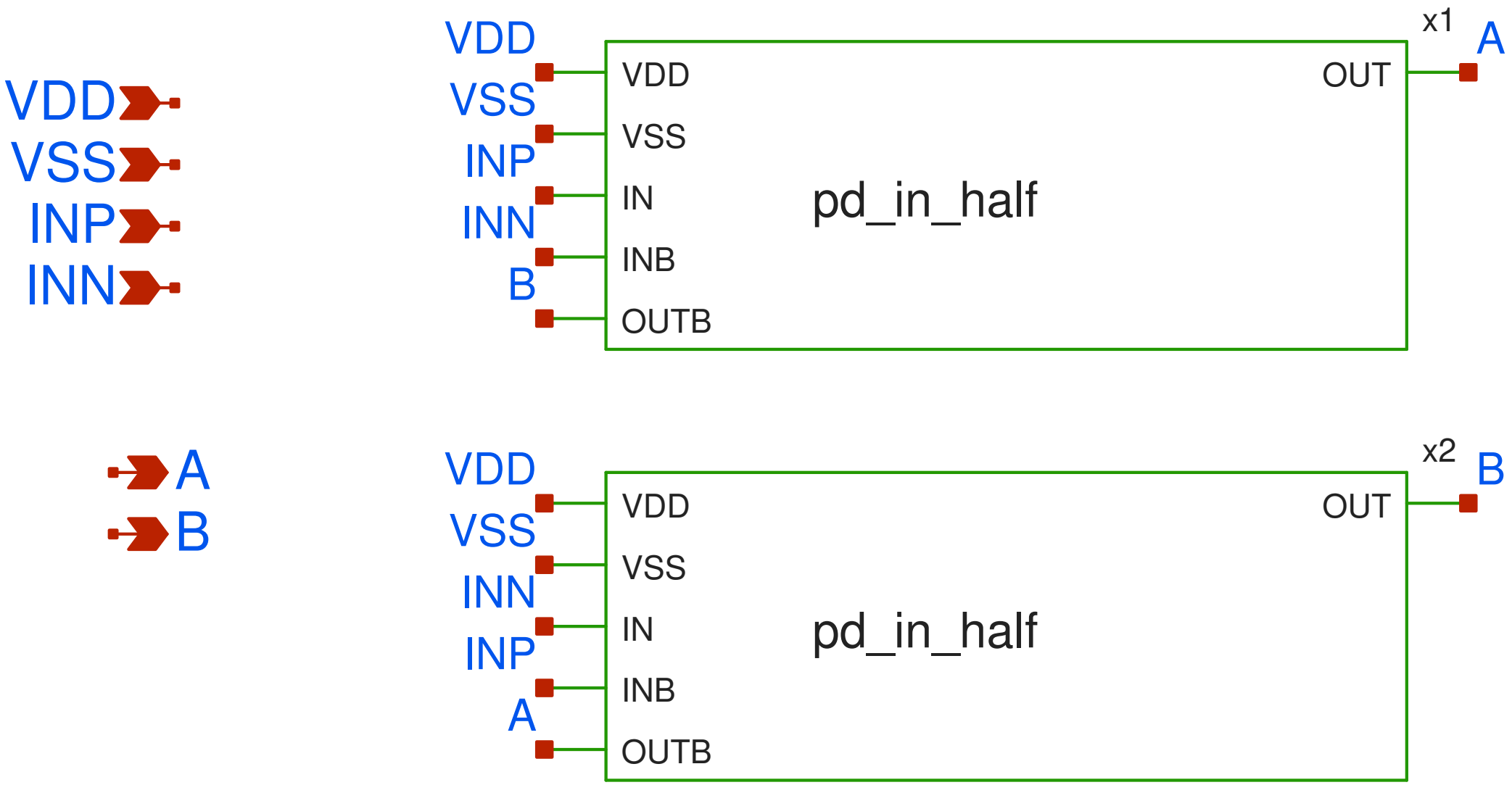
th_sw_main.sch



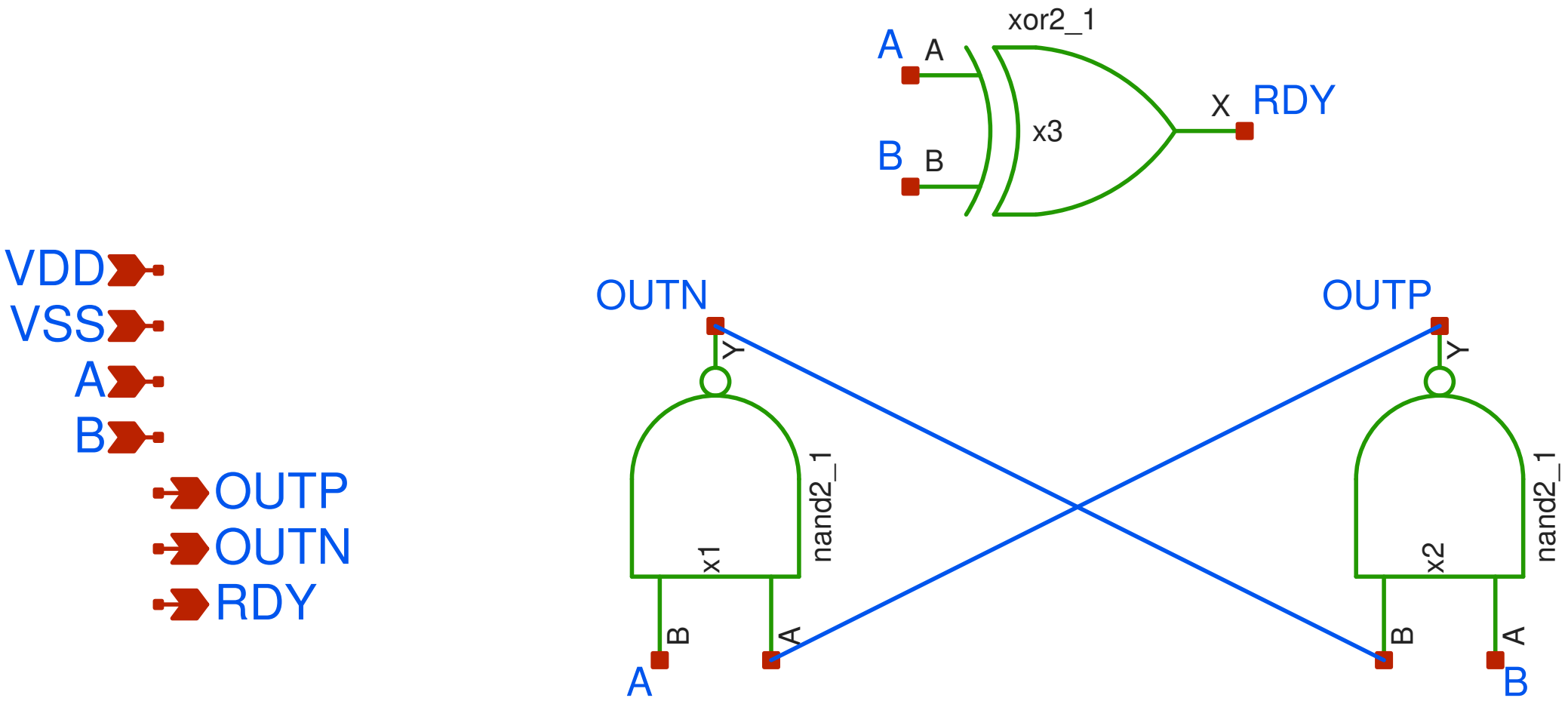
bootstrap.sch



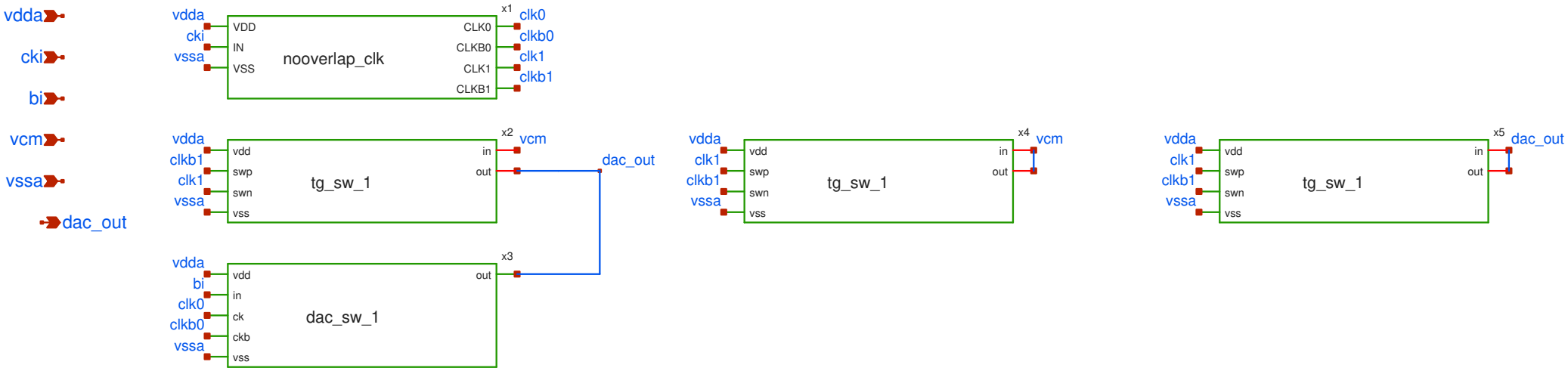
pd_in.sch


VDD
VSS
INP
INN
VDD
VSS
INP
INN
B
VDD
VSS
IN
INB
OUTB
pd_in_half
OUT
x1
A
A
B
VDD
VSS
INN
INP
A
VDD
VSS
IN
INB
OUTB
pd_in_half
OUT
x2
B

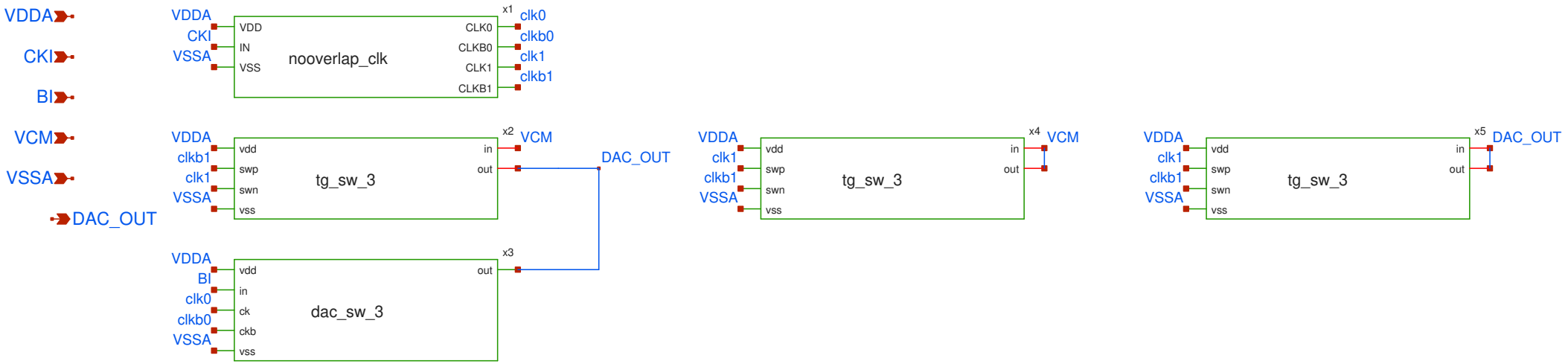
pd_out.sch


xor2_1
A
A
B
B
x3
X
RDY
VDD
VSS
A
B
OUTP
OUTN
RDY
OUTN
OUTP
Y
nand2_1
x1
x2
B
A
A
B

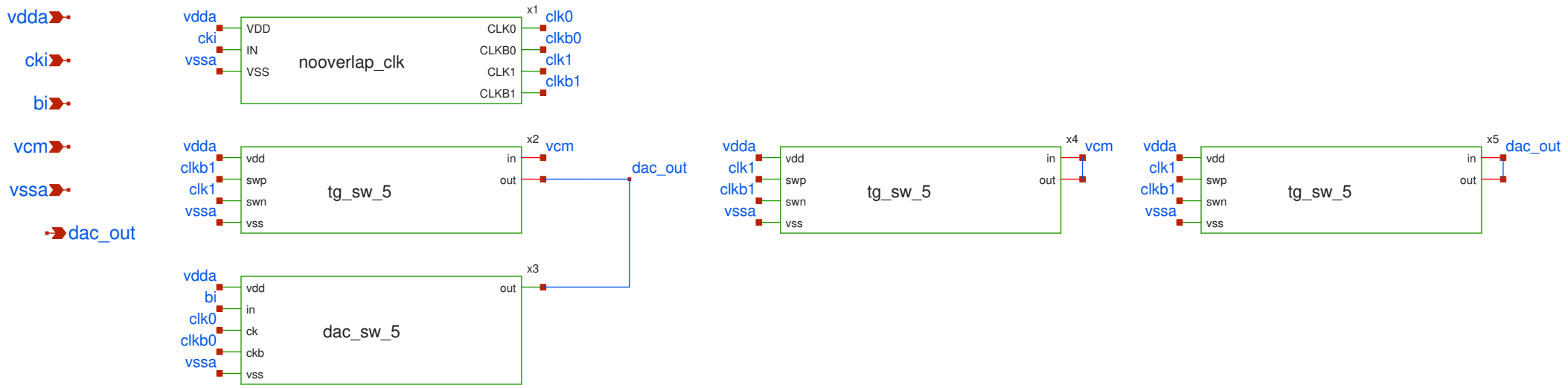
cdac_sw_1.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
nooverlap_clk
VDD
IN
VSS
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
tg_sw_1
vdd
swp
swn
vss
in
out
x3
dac_sw_1
ck
ckb
x4
x5

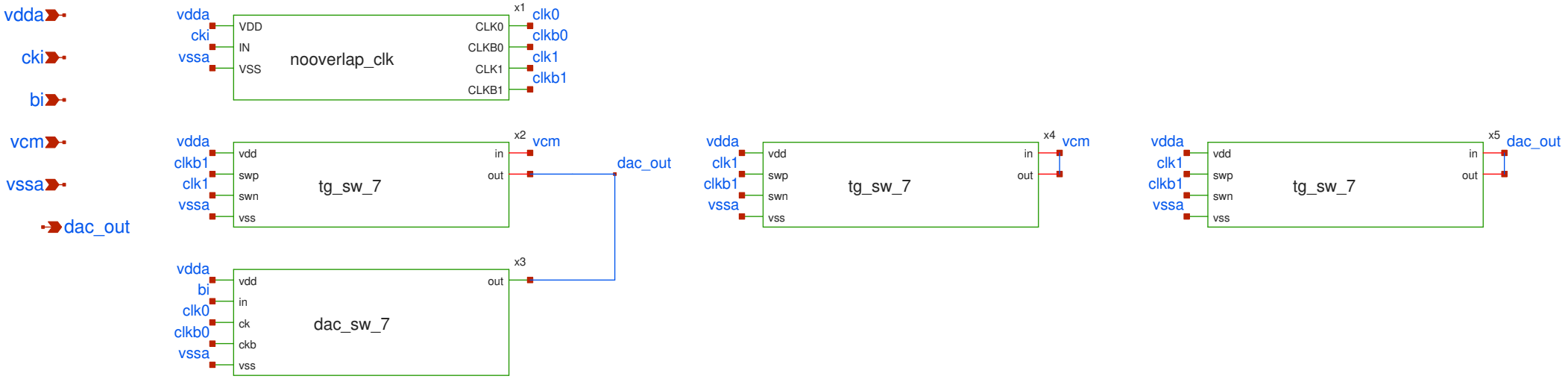
cdac_sw_3.sch


VDDA
CKI
BI
VCM
VSSA
DAC_OUT
x1
nooverlap_clk
VDD
IN
VSS
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
tg_sw_3
vdd
swp
swn
vss
in
out
x3
dac_sw_3
ck
ckb
x4
x5

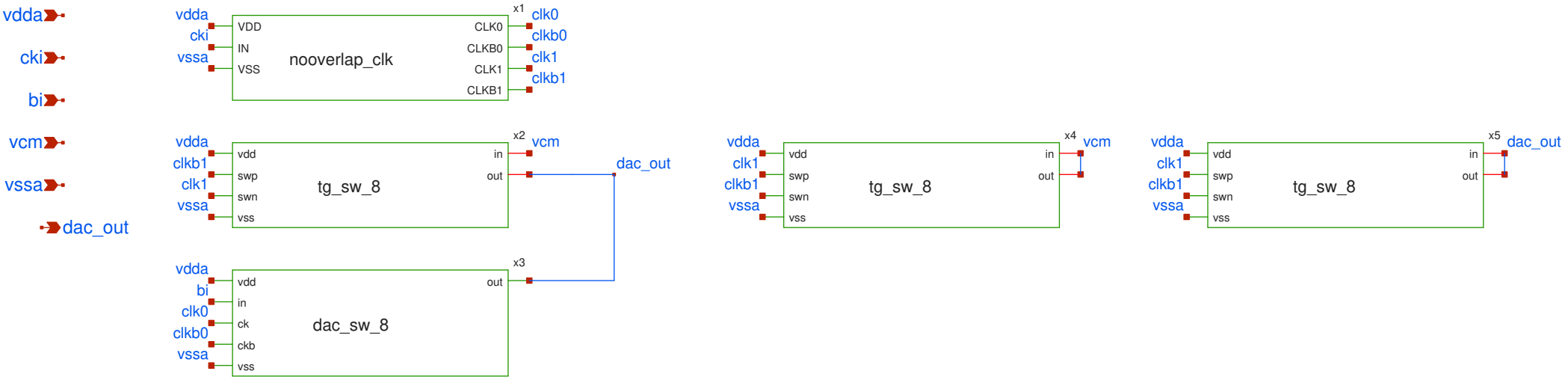
cdac_sw_5.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
nooverlap_clk
VDD
IN
VSS
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
tg_sw_5
vdd
swp
swn
vss
in
out
x3
dac_sw_5
ck
ckb
x4
x5

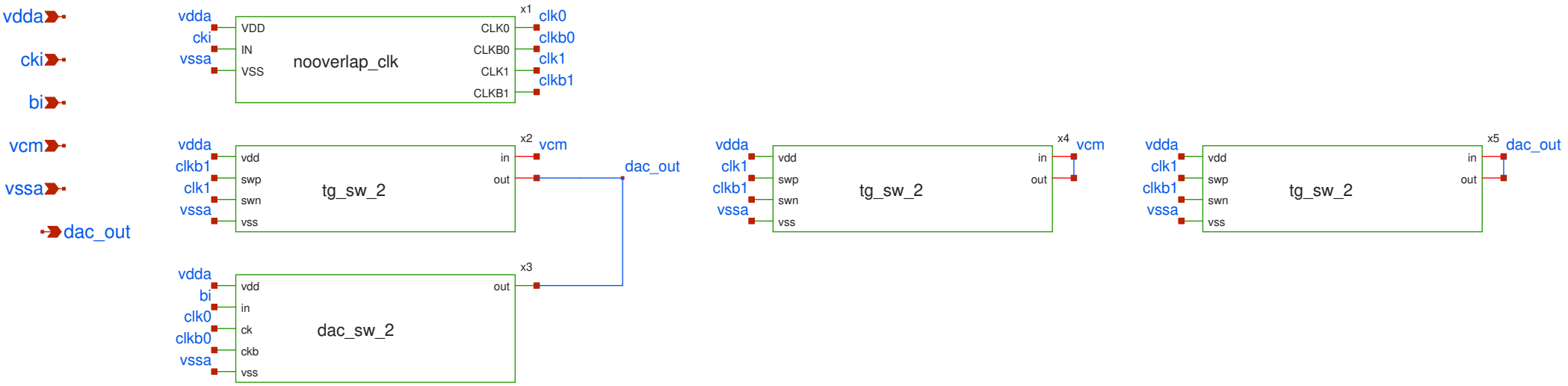
cdac_sw_7.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
vdda
cki
vssa
VDD
IN
VSS
nooverlap_clk
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
vdda
clkb1
clk1
vssa
vdd
swp
swn
vss
tg_sw_7
in
out
vcm
dac_out
x3
vdda
bi
clk0
clkb0
vssa
vdd
in
ck
ckb
vss
dac_sw_7
out
x4
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_7
in
out
vcm
x5
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_7
in
out
dac_out

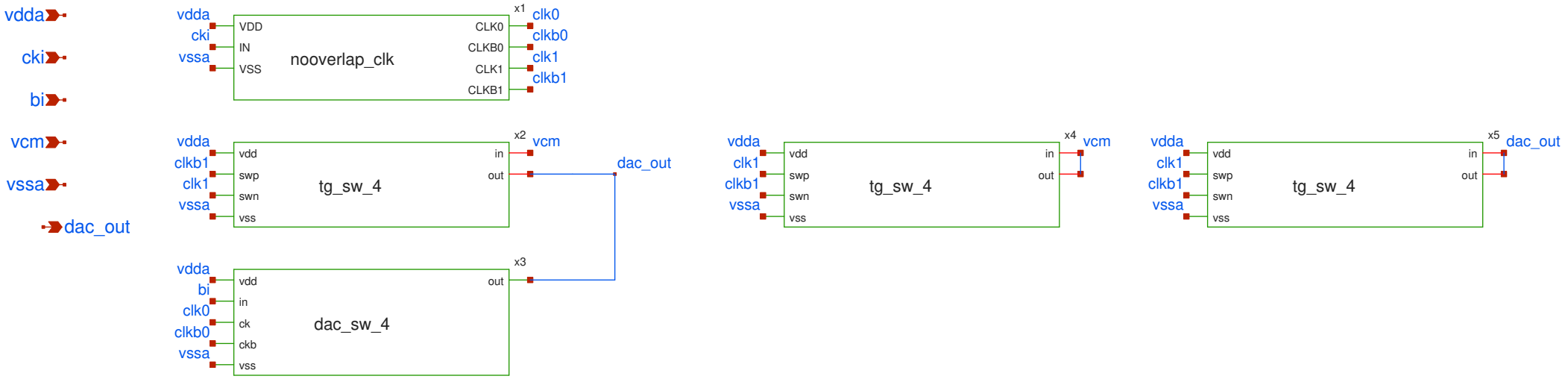
cdac_sw_9.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
vdda
cki
vssa
VDD
IN
VSS
nooverlap_clk
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
vdda
clkb1
clk1
vssa
vdd
swp
swn
vss
tg_sw_8
in
out
vcm
dac_out
x3
vdda
bi
clk0
clkb0
vssa
vdd
in
ck
ckb
vss
dac_sw_8
out
x4
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_8
in
out
vcm
x5
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_8
in
out
dac_out

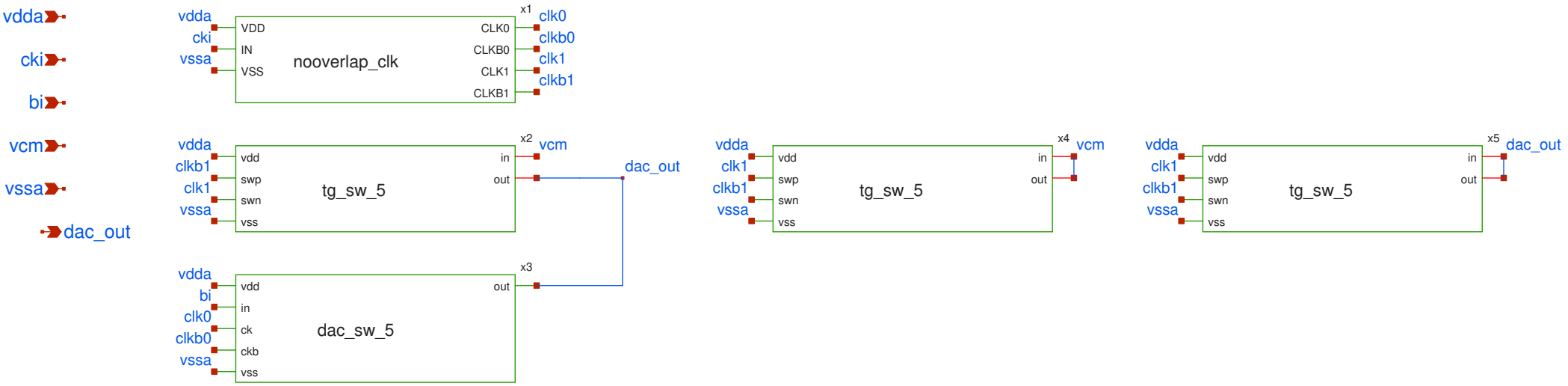
cdac_sw_2.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
vdda
cki
vssa
VDD
IN
VSS
nooverlap_clk
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
vdda
clkb1
clk1
vssa
vdd
swp
swn
vss
tg_sw_2
in
out
vcm
dac_out
x3
vdda
bi
clk0
clkb0
vssa
vdd
in
ck
ckb
vss
dac_sw_2
out
x4
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_2
in
out
vcm
x5
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_2
in
out
dac_out

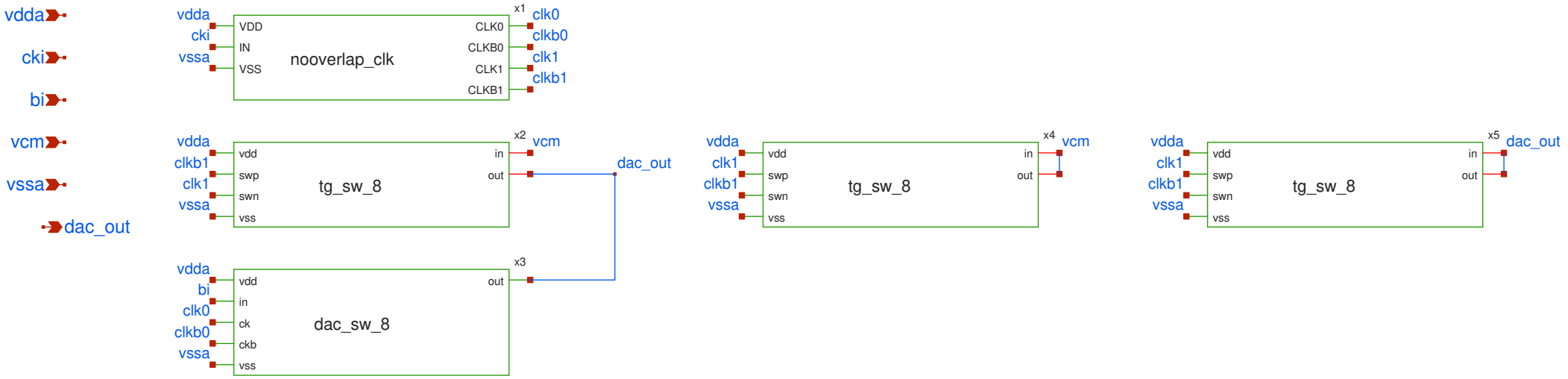
cdac_sw_4.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
vdda
cki
vssa
VDD
IN
VSS
nooverlap_clk
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
vdda
clkb1
clk1
vssa
vdd
swp
swn
vss
tg_sw_4
in
out
vcm
dac_out
x3
vdda
bi
clk0
clkb0
vssa
vdd
in
ck
ckb
vss
dac_sw_4
out
x4
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_4
in
out
vcm
x5
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_4
in
out
dac_out

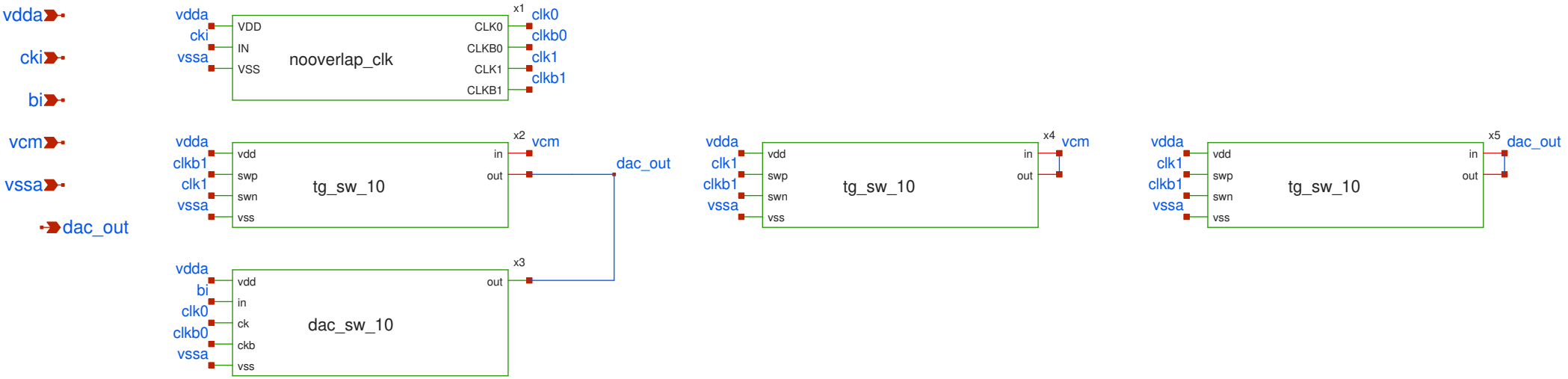
cdac_sw_6.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
vdda
cki
vssa
VDD
IN
VSS
nooverlap_clk
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
vdda
clkb1
clk1
vssa
vdd
swp
swn
vss
tg_sw_5
in
out
vcm
dac_out
x3
vdda
bi
clk0
clkb0
vssa
vdd
in
ck
ckb
vss
dac_sw_5
out
x4
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_5
in
out
vcm
x5
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_5
in
out
dac_out

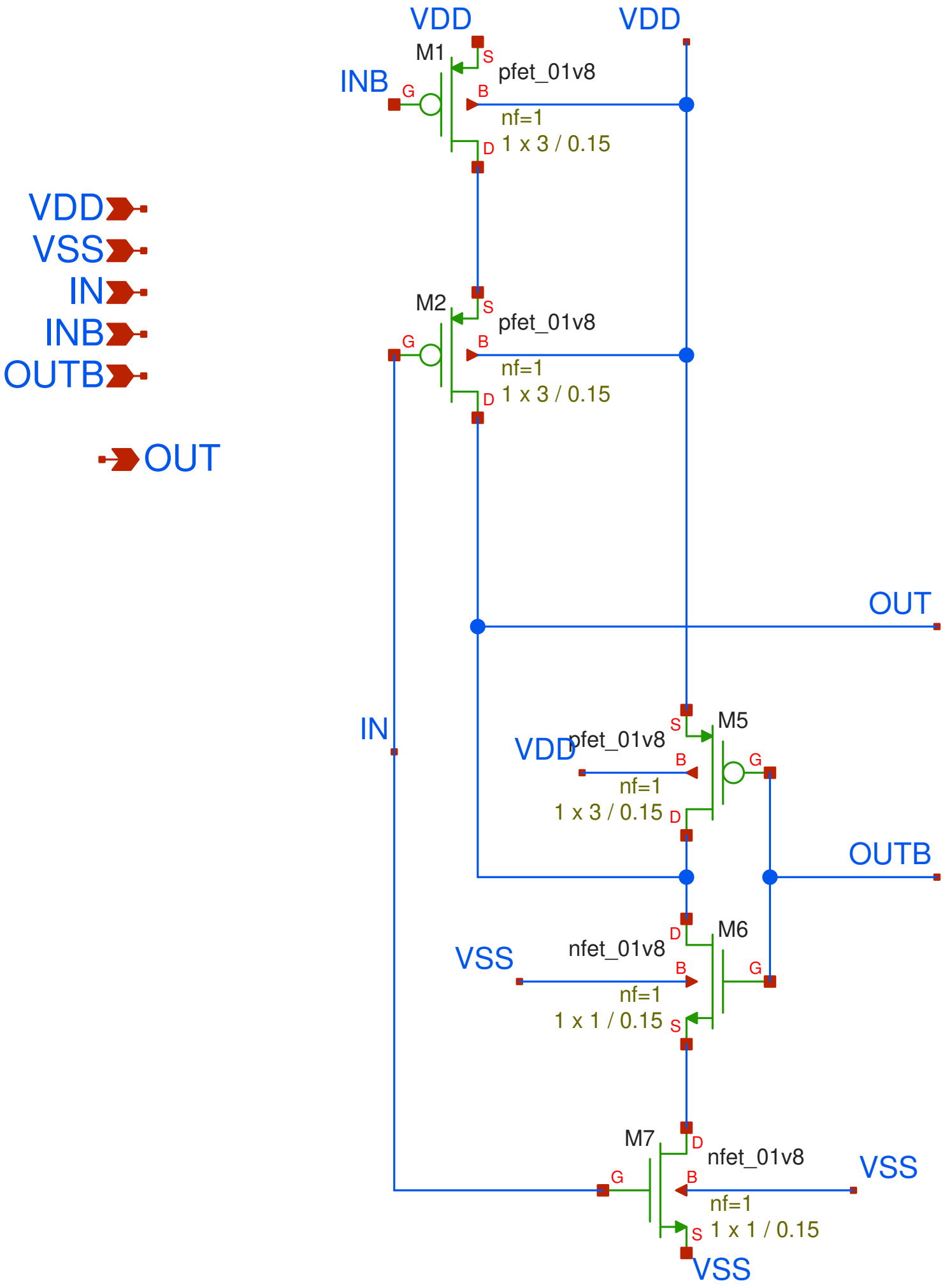
cdac_sw_8.sch


vdda
cki
bi
vcm
vssa
dac_out
x1
vdda
cki
vssa
VDD
IN
VSS
nooverlap_clk
CLK0
CLKB0
CLK1
CLKB1
clk0
clkb0
clk1
clkb1
x2
vdda
clkb1
clk1
vssa
vdd
swp
swn
vss
tg_sw_8
in
out
vcm
dac_out
x3
vdda
bi
clk0
clkb0
vssa
vdd
in
ck
ckb
vss
dac_sw_8
out
x4
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_8
in
out
vcm
x5
vdda
clk1
clkb1
vssa
vdd
swp
swn
vss
tg_sw_8
in
out
dac_out

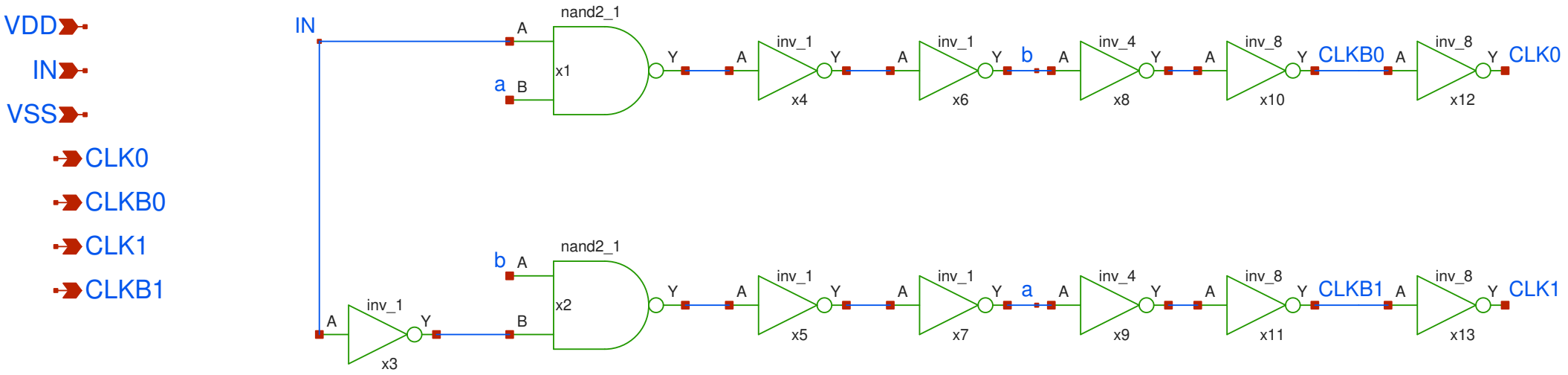
cdac_sw_10.sch



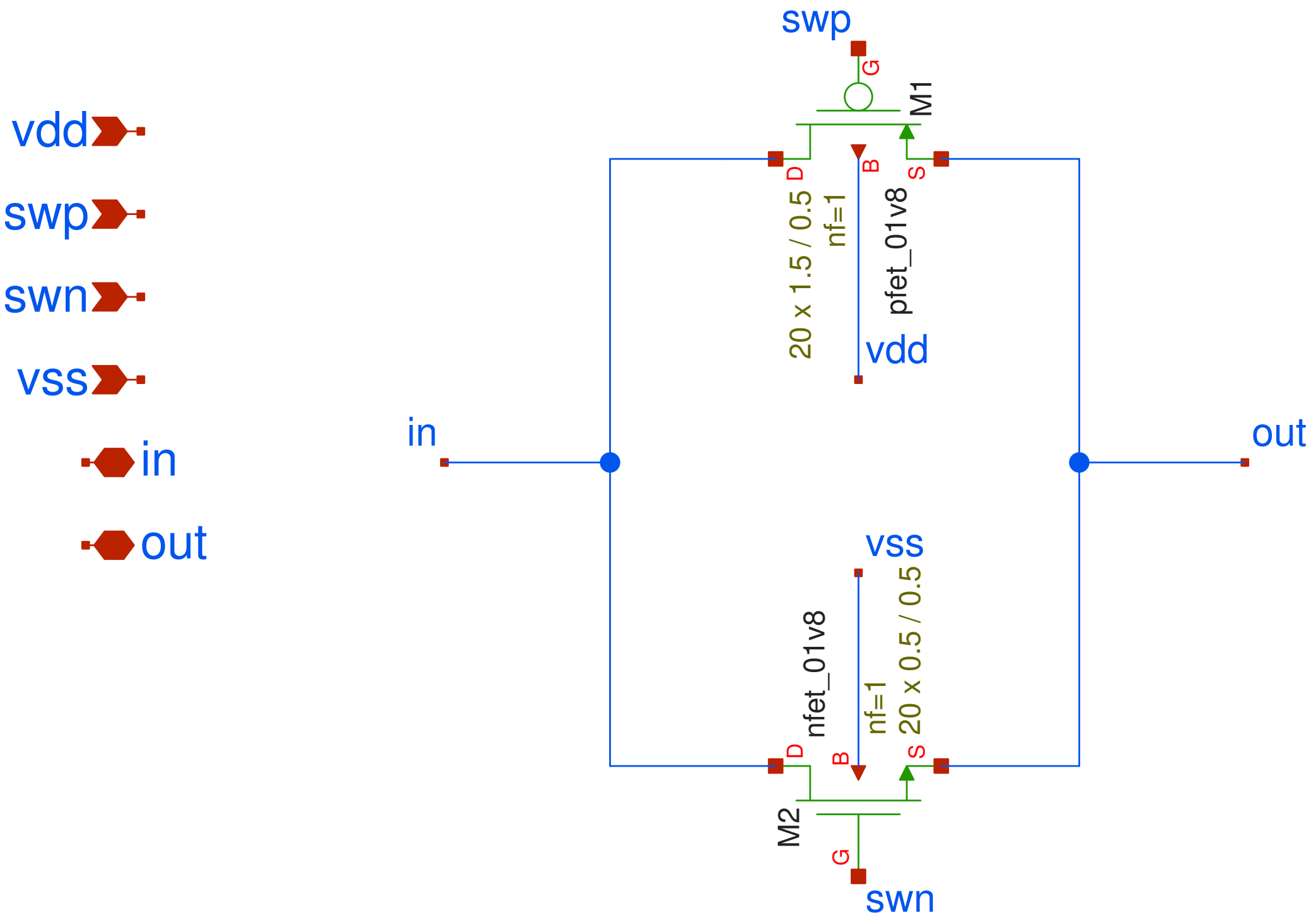
pd_in_half.sch



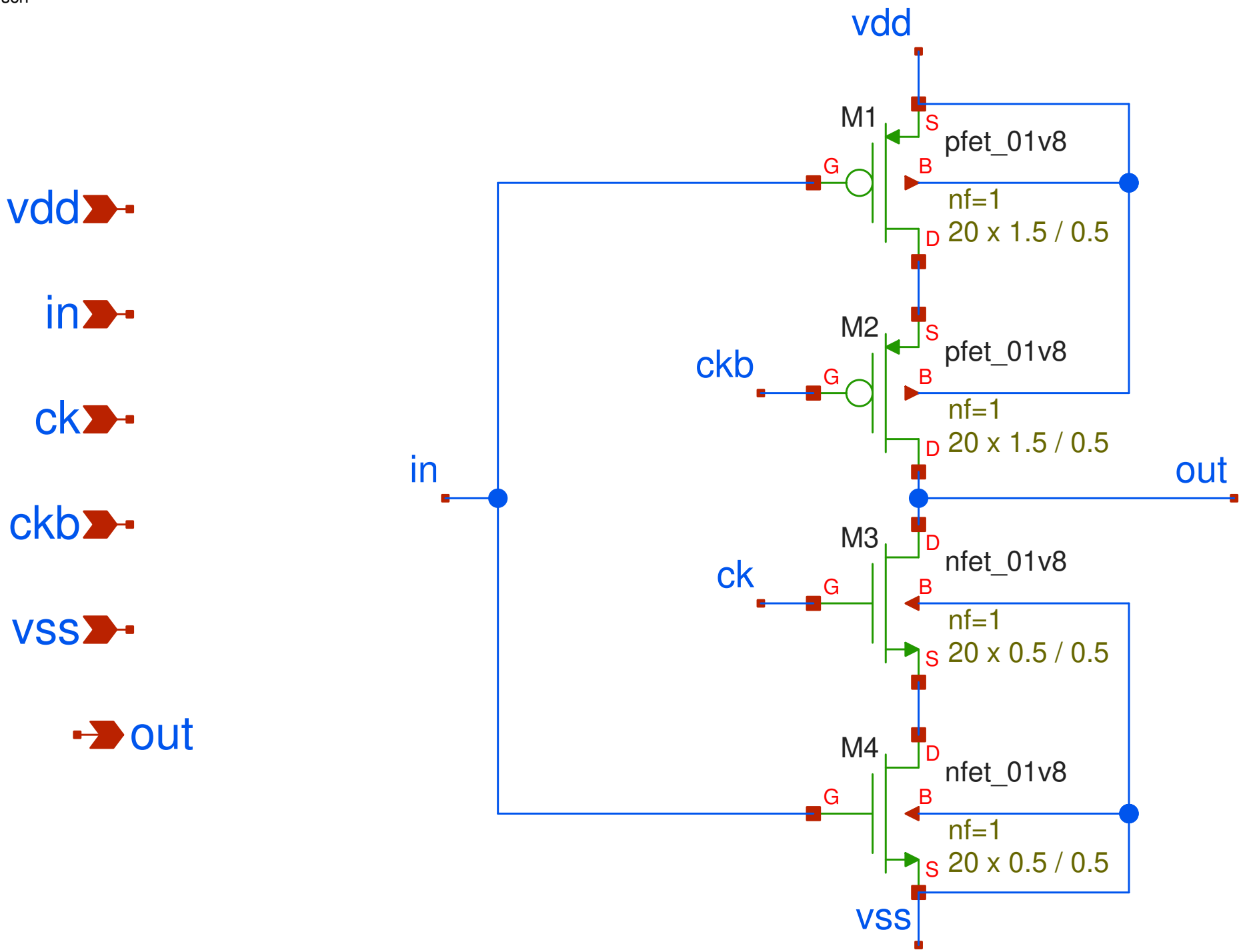
nooverlap_clk.sch



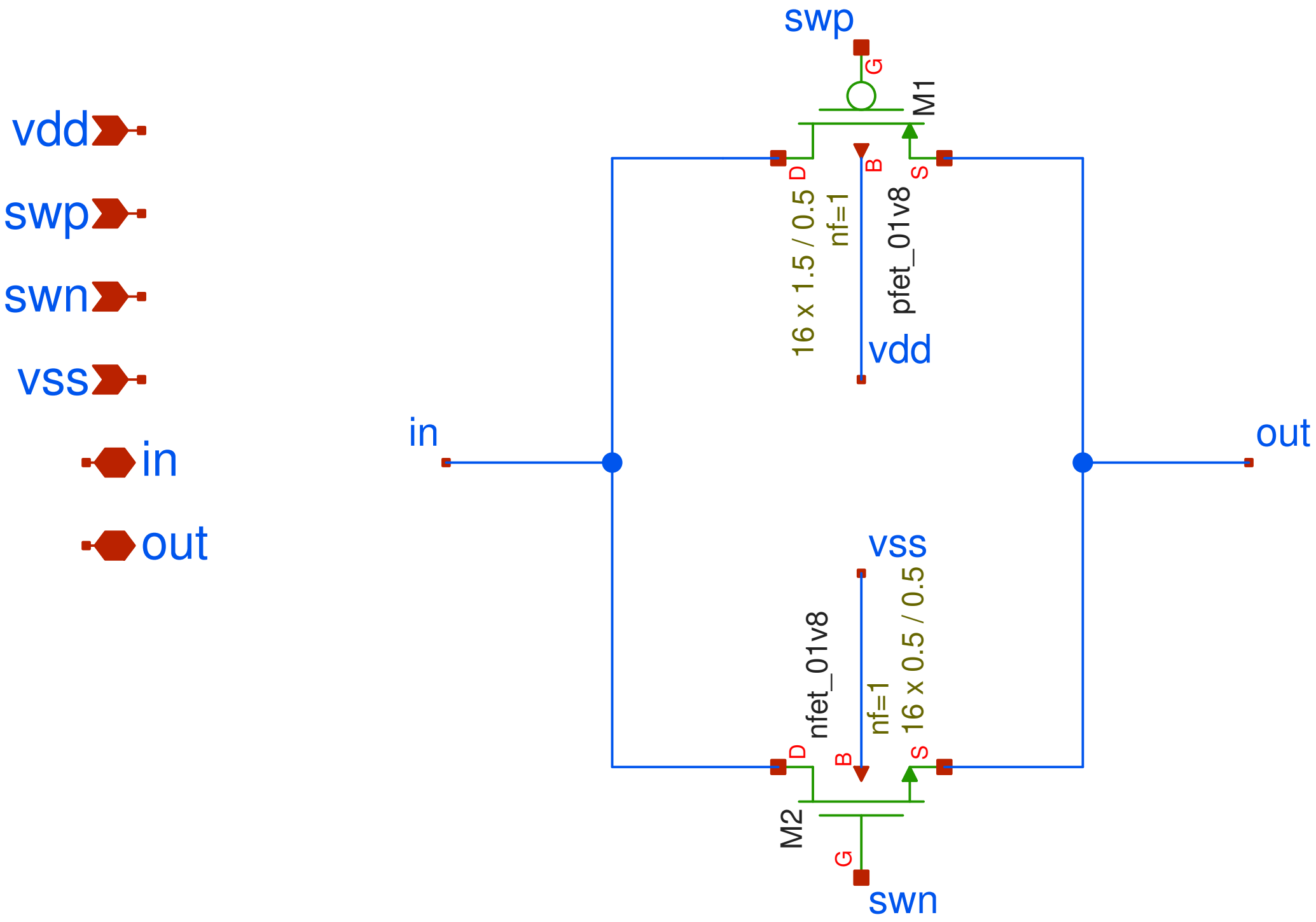
tg_sw_1.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
20 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
20 x 0.5 / 0.5
D
B
S
M2
G
swn

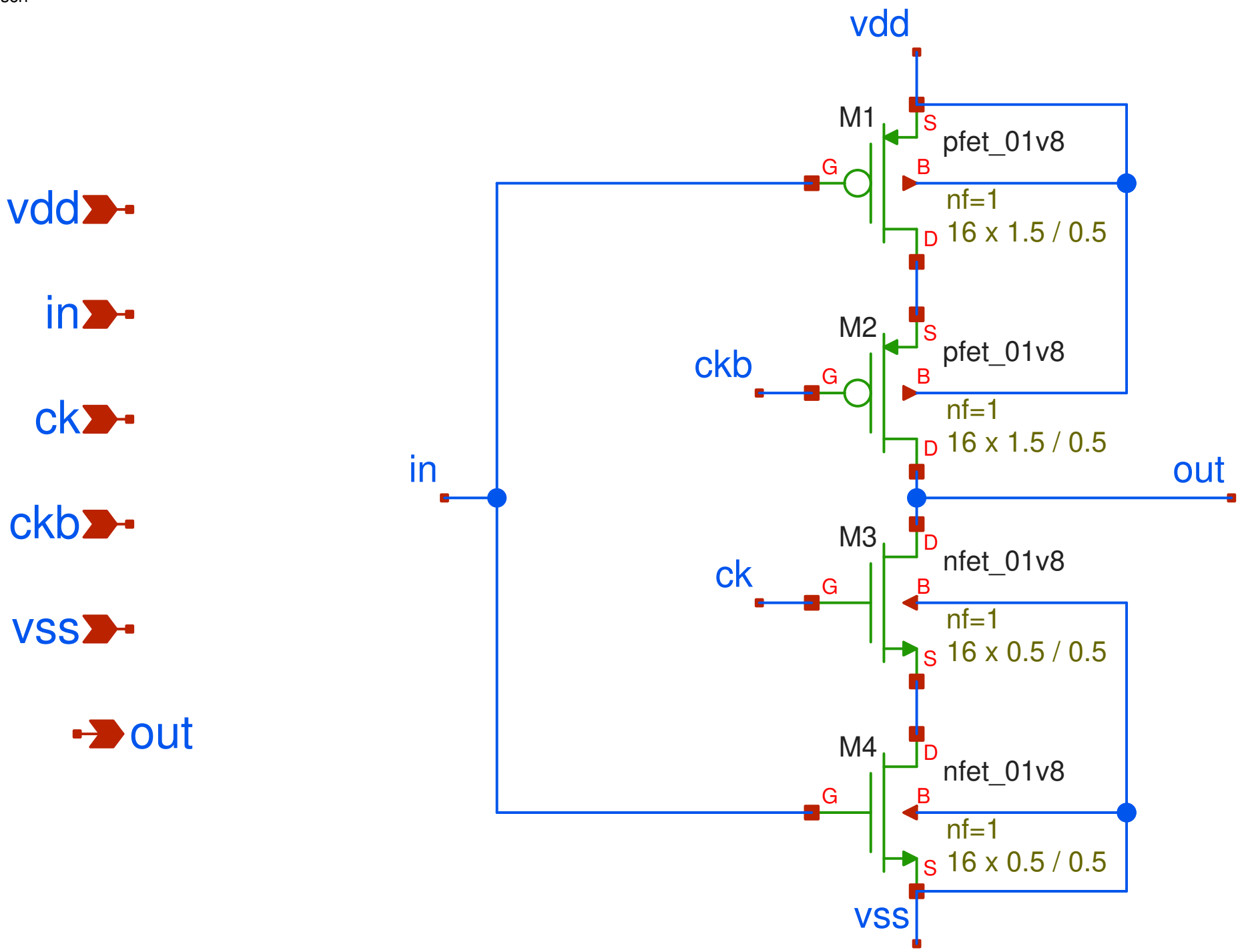
dac_sw_1.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
20 x 1.5 / 0.5
D
M2
S
ckb
pfet_01v8
G
B
nf=1
20 x 1.5 / 0.5
D
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
20 x 0.5 / 0.5
S
M4
D
nfet_01v8
G
B
nf=1
20 x 0.5 / 0.5
S
vss

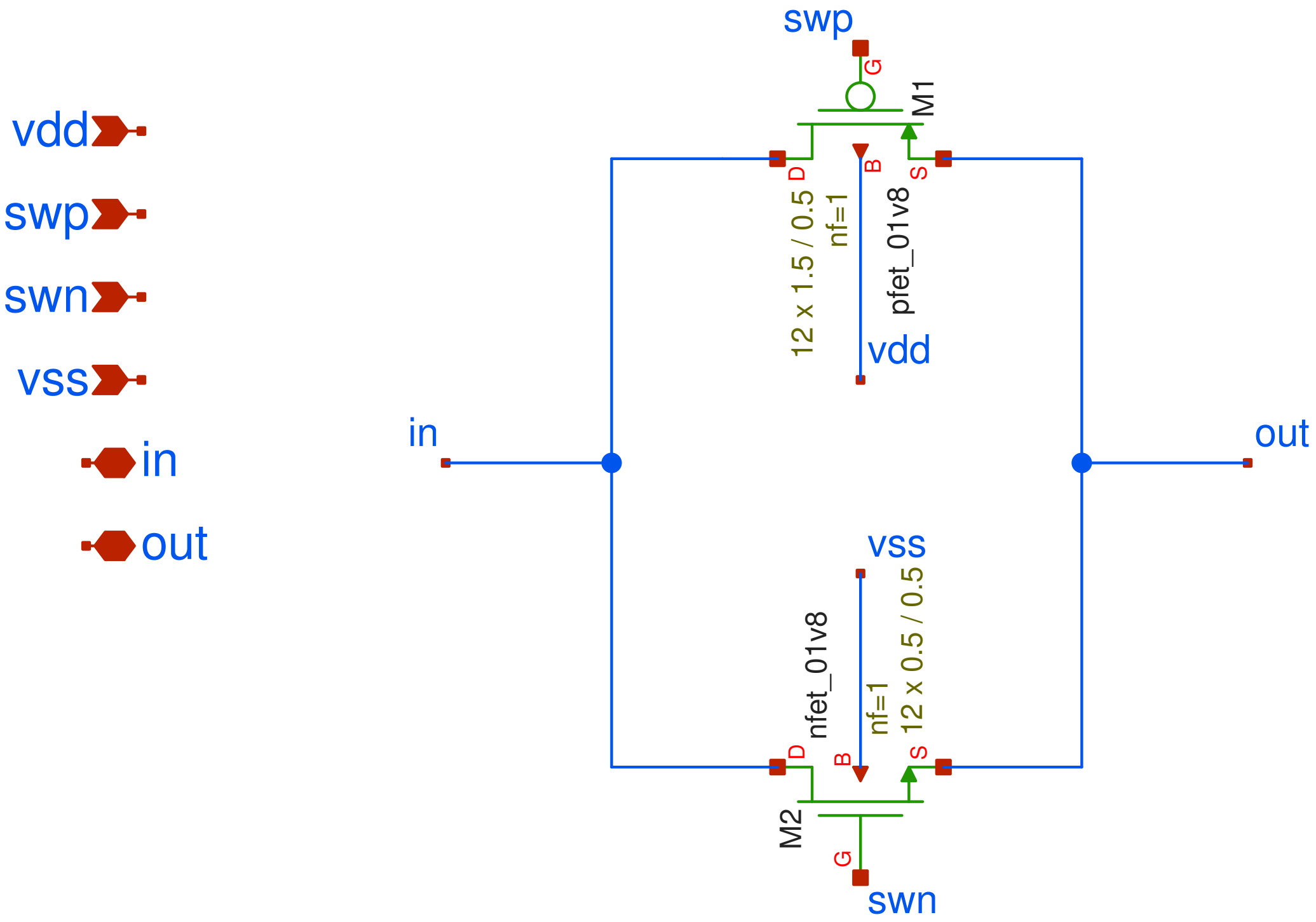
tg_sw_3.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
16 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
16 x 0.5 / 0.5
D
B
S
M2
G
swn

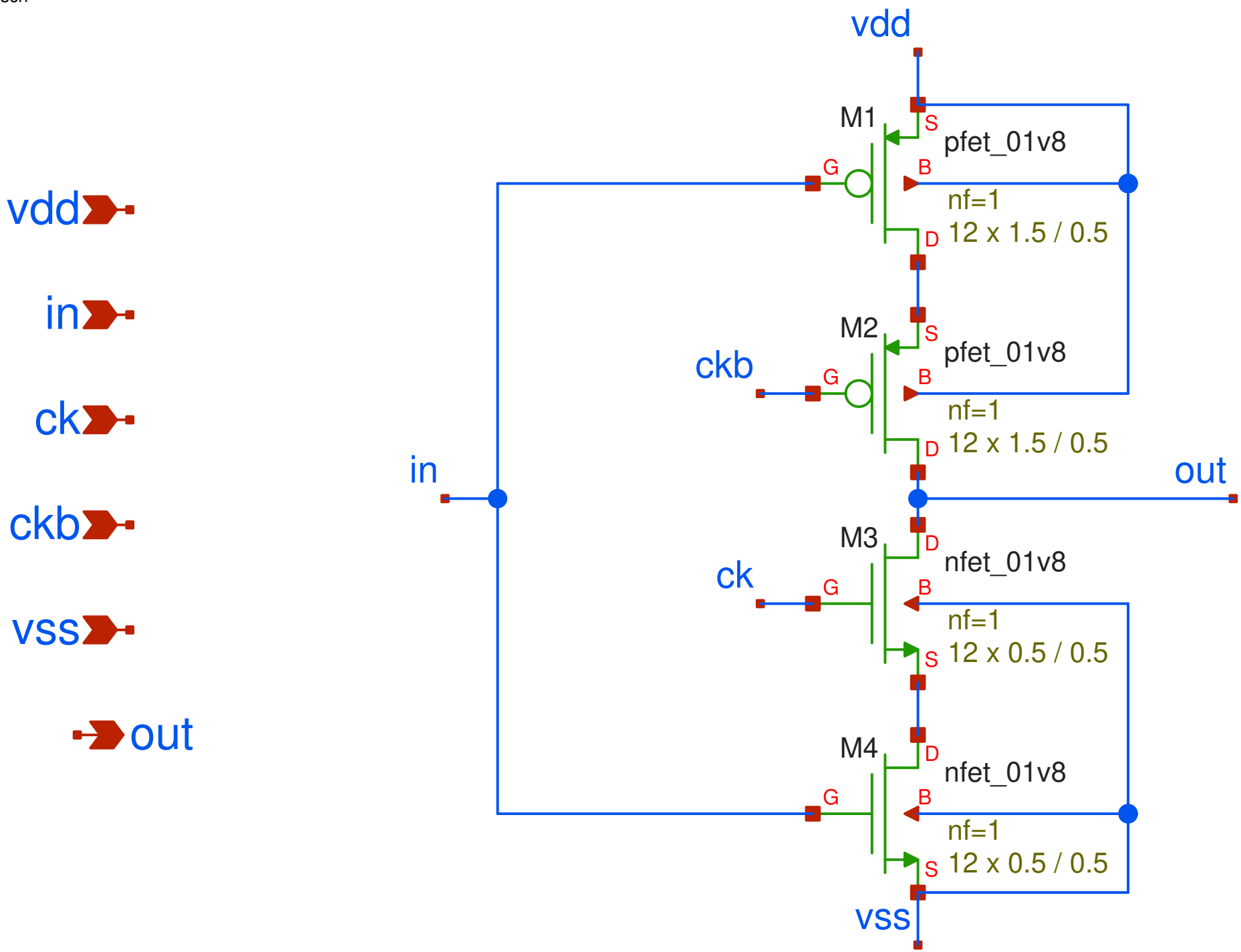
dac_sw_3.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
16 x 1.5 / 0.5
D
M2
S
ckb
pfet_01v8
G
B
nf=1
16 x 1.5 / 0.5
D
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
16 x 0.5 / 0.5
S
M4
D
nfet_01v8
G
B
nf=1
16 x 0.5 / 0.5
S
vss

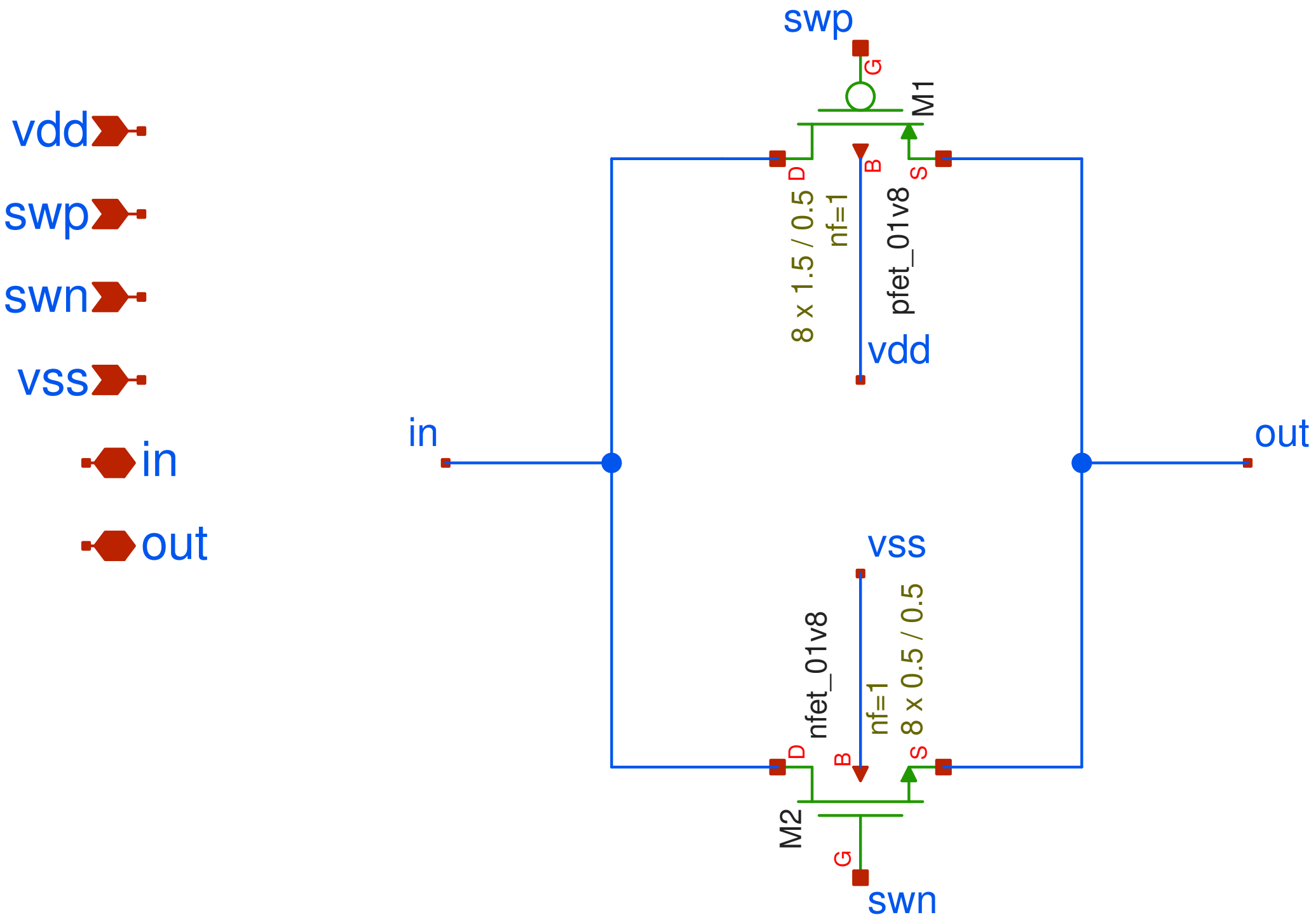
tg_sw_5.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
12 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
12 x 0.5 / 0.5
D
B
S
M2
G
swn

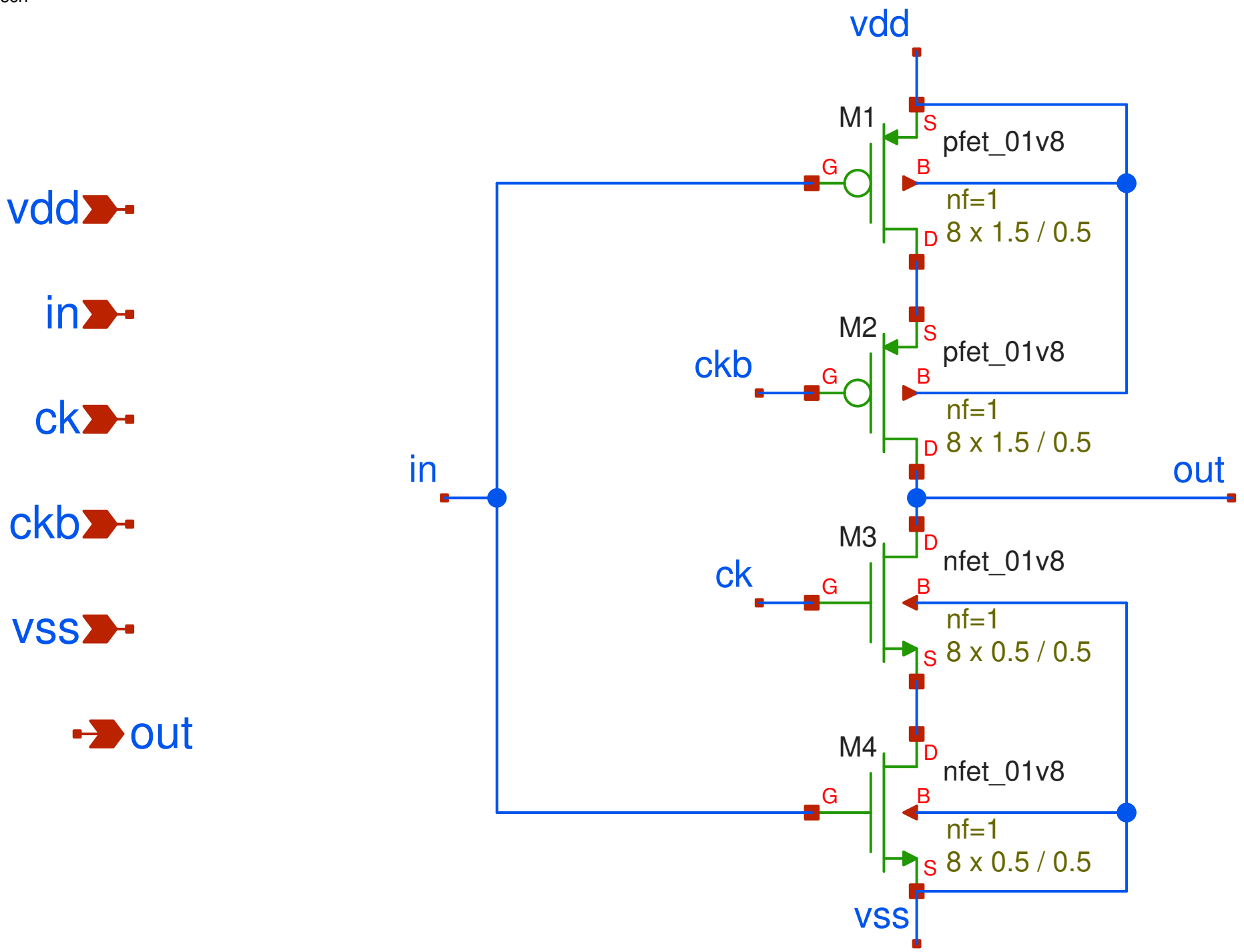
dac_sw_5.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
12 x 1.5 / 0.5
D
M2
S
ckb
pfet_01v8
G
B
nf=1
12 x 1.5 / 0.5
D
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
12 x 0.5 / 0.5
S
M4
D
nfet_01v8
G
B
nf=1
12 x 0.5 / 0.5
S
vss

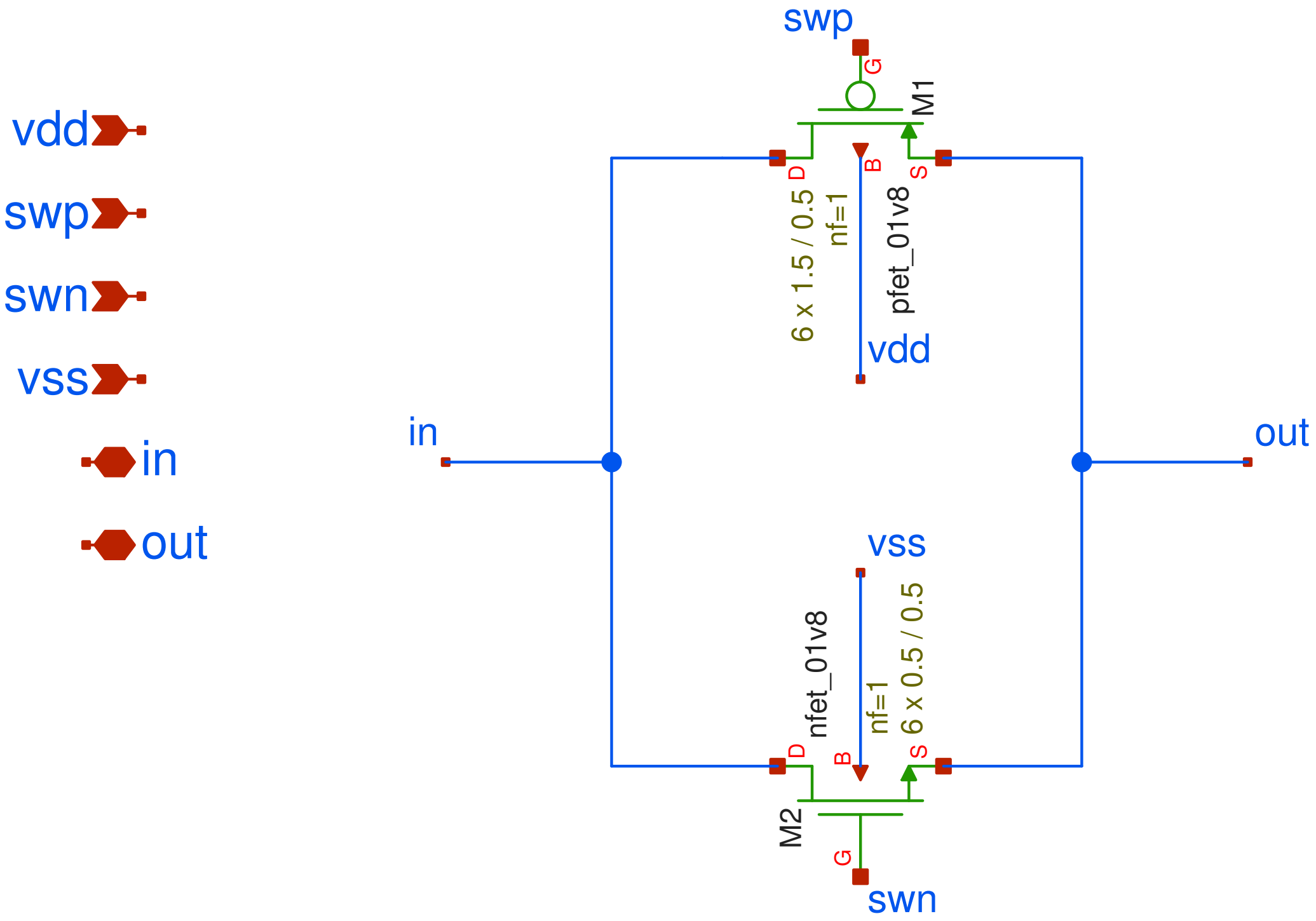
tg_sw_7.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
8 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
8 x 0.5 / 0.5
D
B
S
M2
G
swn

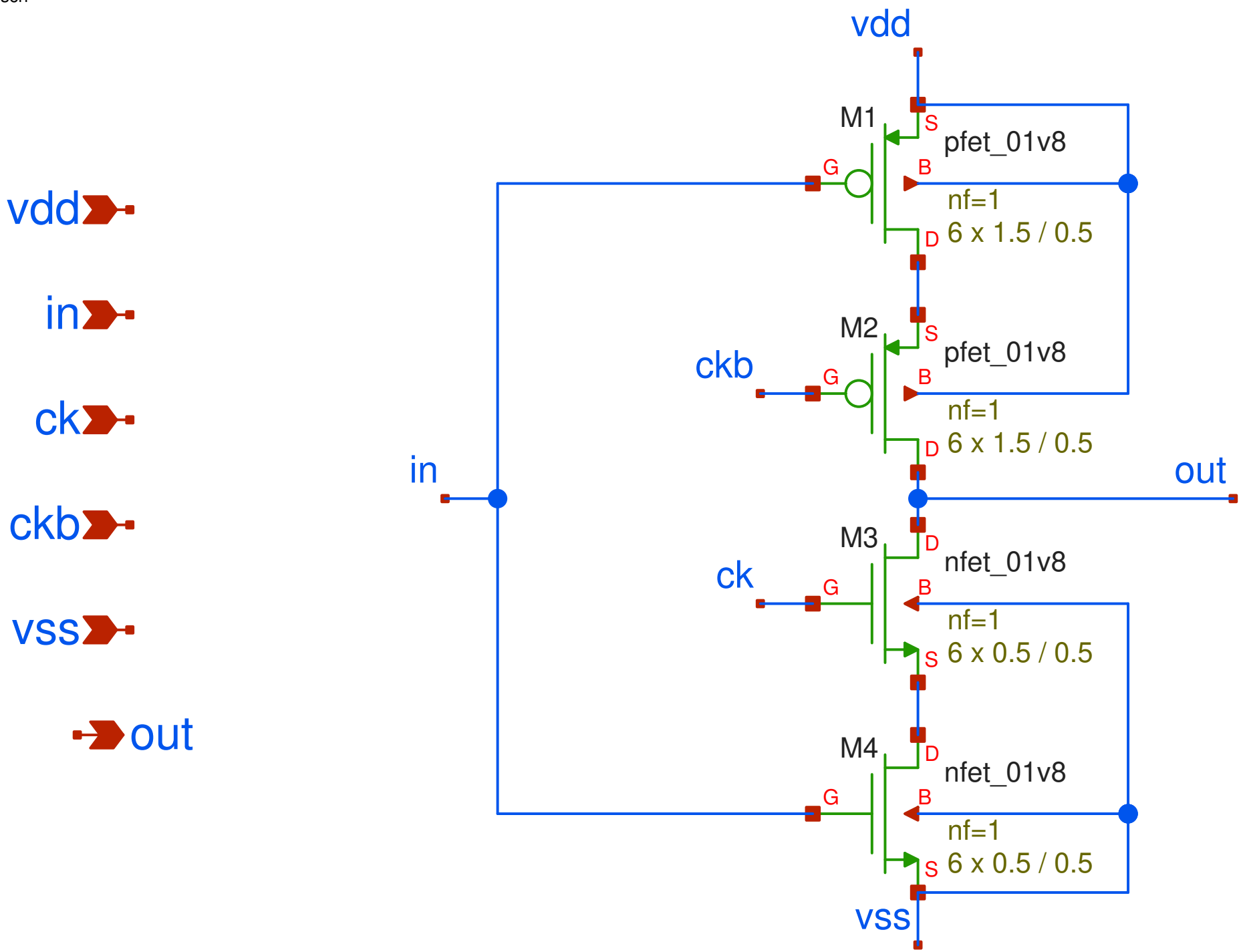
dac_sw_7.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
D
8 x 1.5 / 0.5
M2
S
ckb
pfet_01v8
G
B
nf=1
in
D
8 x 1.5 / 0.5
out
M3
D
nfet_01v8
ck
G
B
nf=1
S
8 x 0.5 / 0.5
M4
D
nfet_01v8
G
B
nf=1
S
8 x 0.5 / 0.5
vss

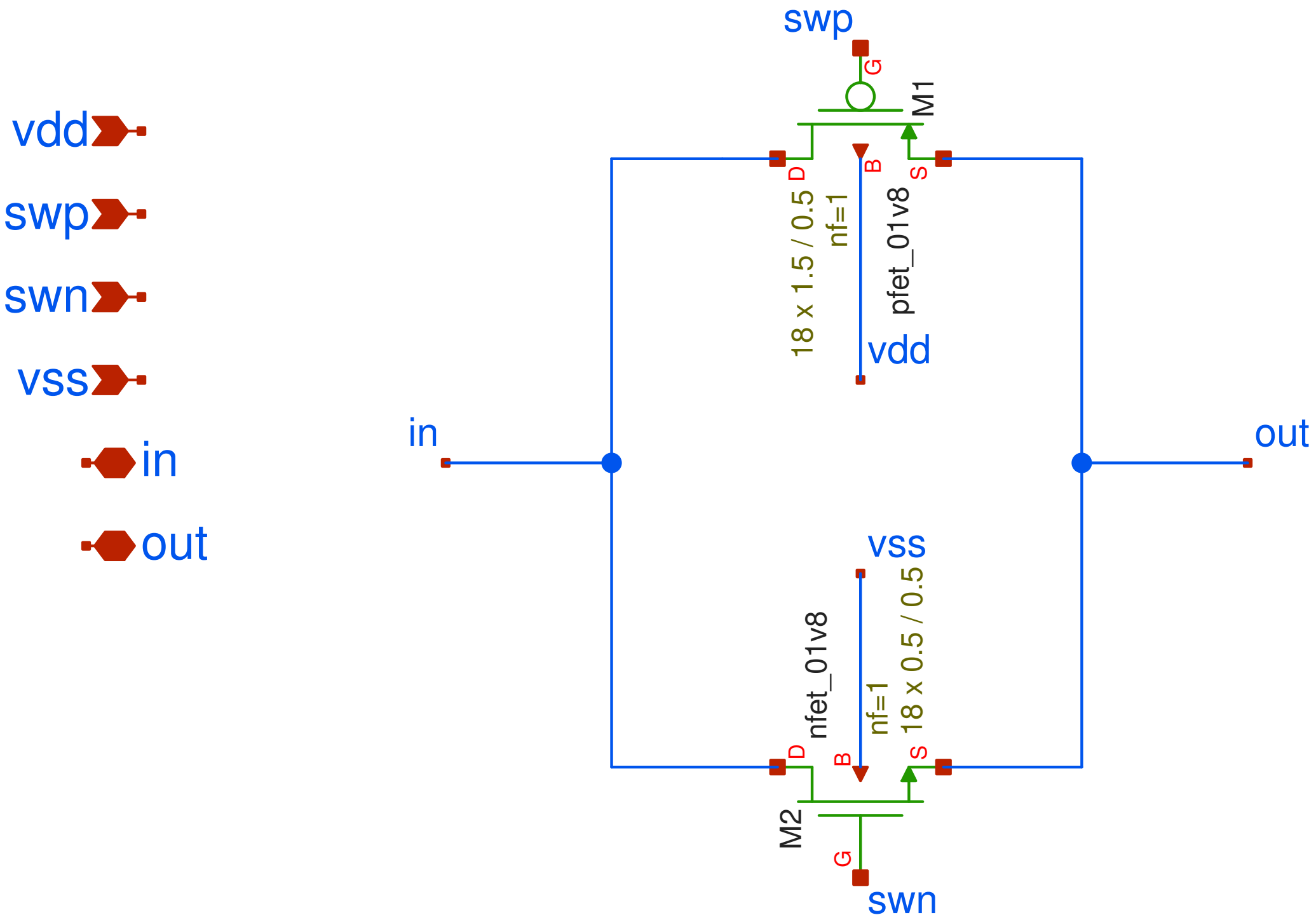
tg_sw_8.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
6 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
6 x 0.5 / 0.5
D
B
S
M2
G
swn

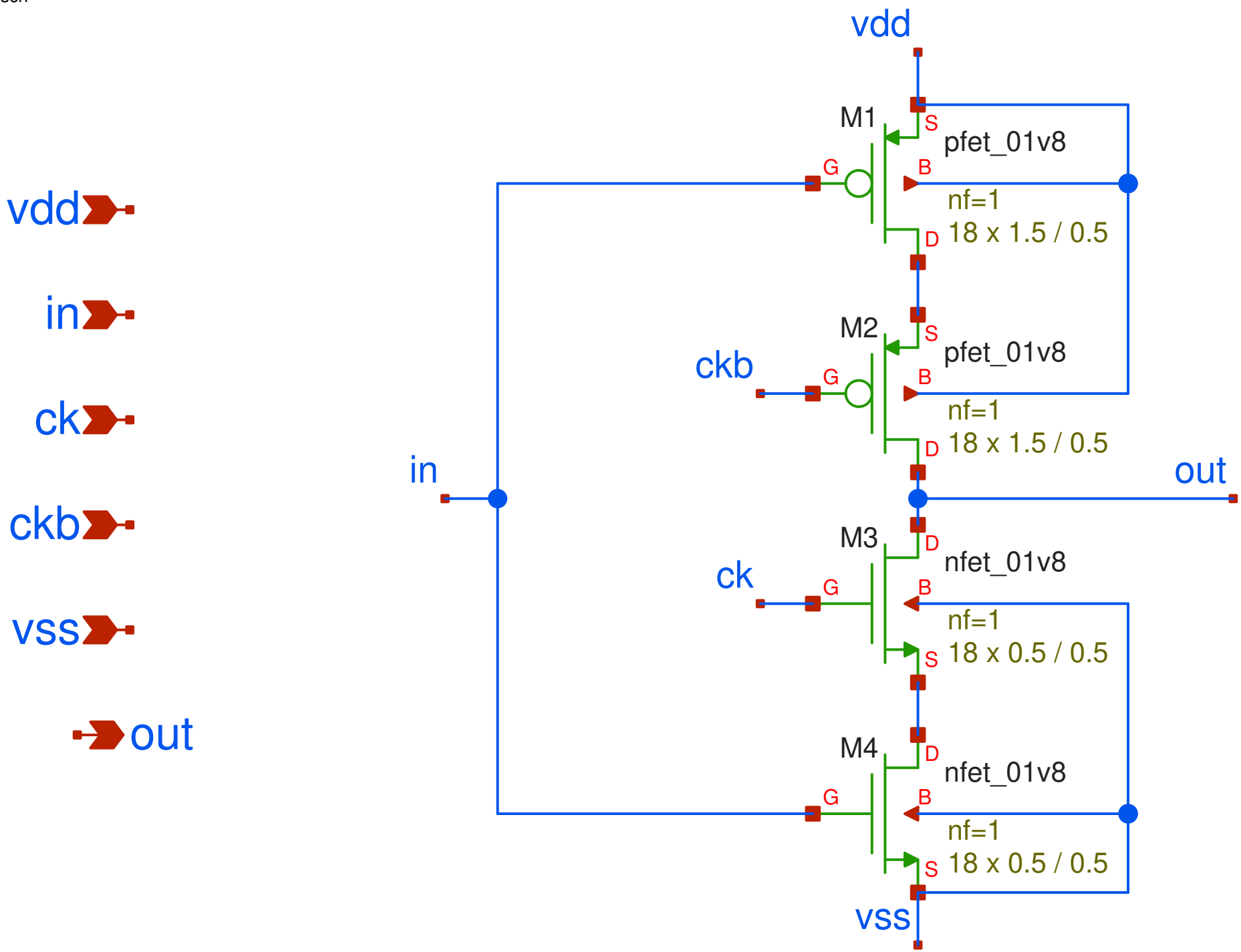
dac_sw_8.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
6 x 1.5 / 0.5
D
M2
S
ckb
pfet_01v8
G
B
nf=1
6 x 1.5 / 0.5
D
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
6 x 0.5 / 0.5
S
M4
D
nfet_01v8
G
B
nf=1
6 x 0.5 / 0.5
S
vss

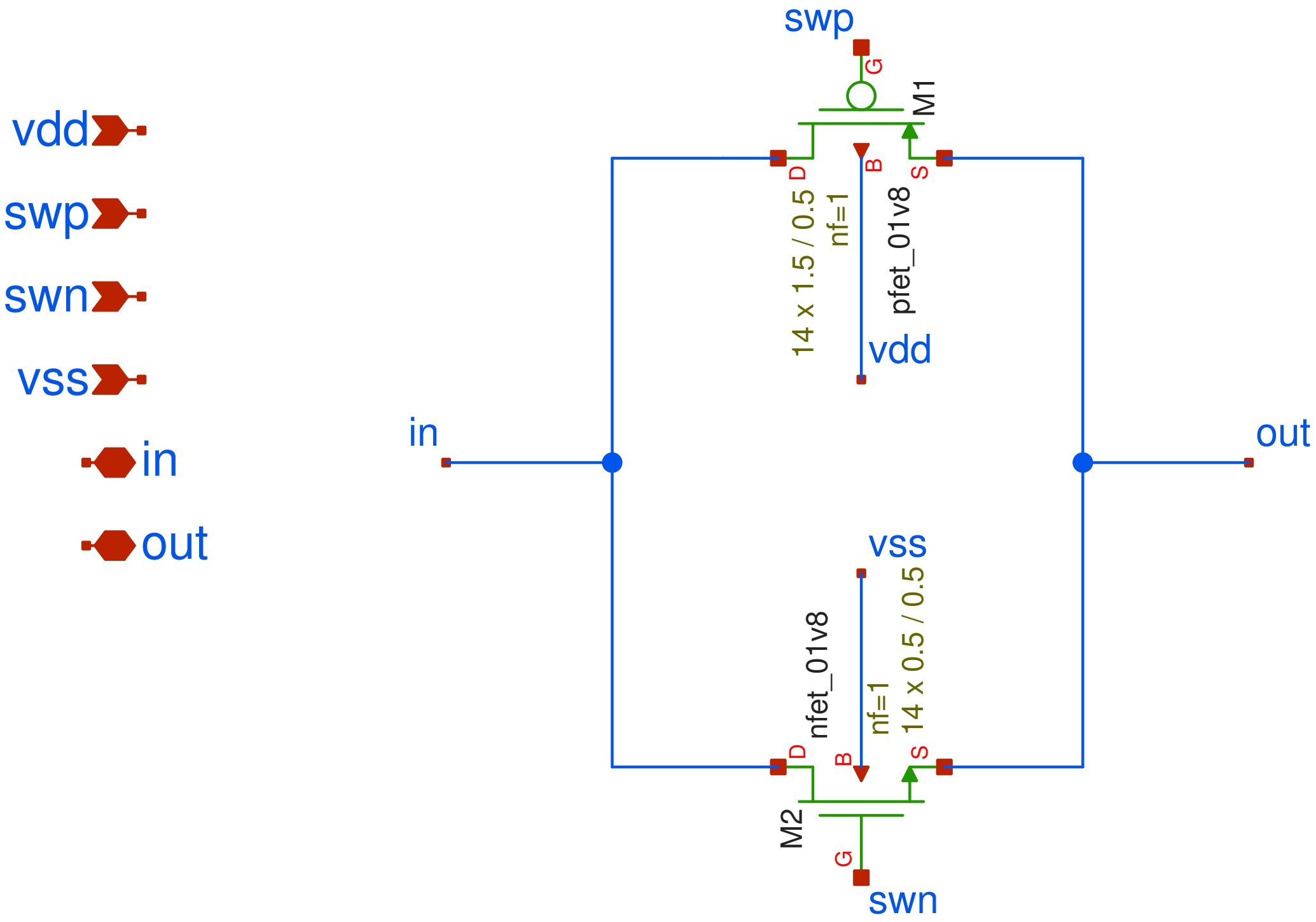
tg_sw_2.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
18 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
18 x 0.5 / 0.5
D
B
S
M2
G
swn

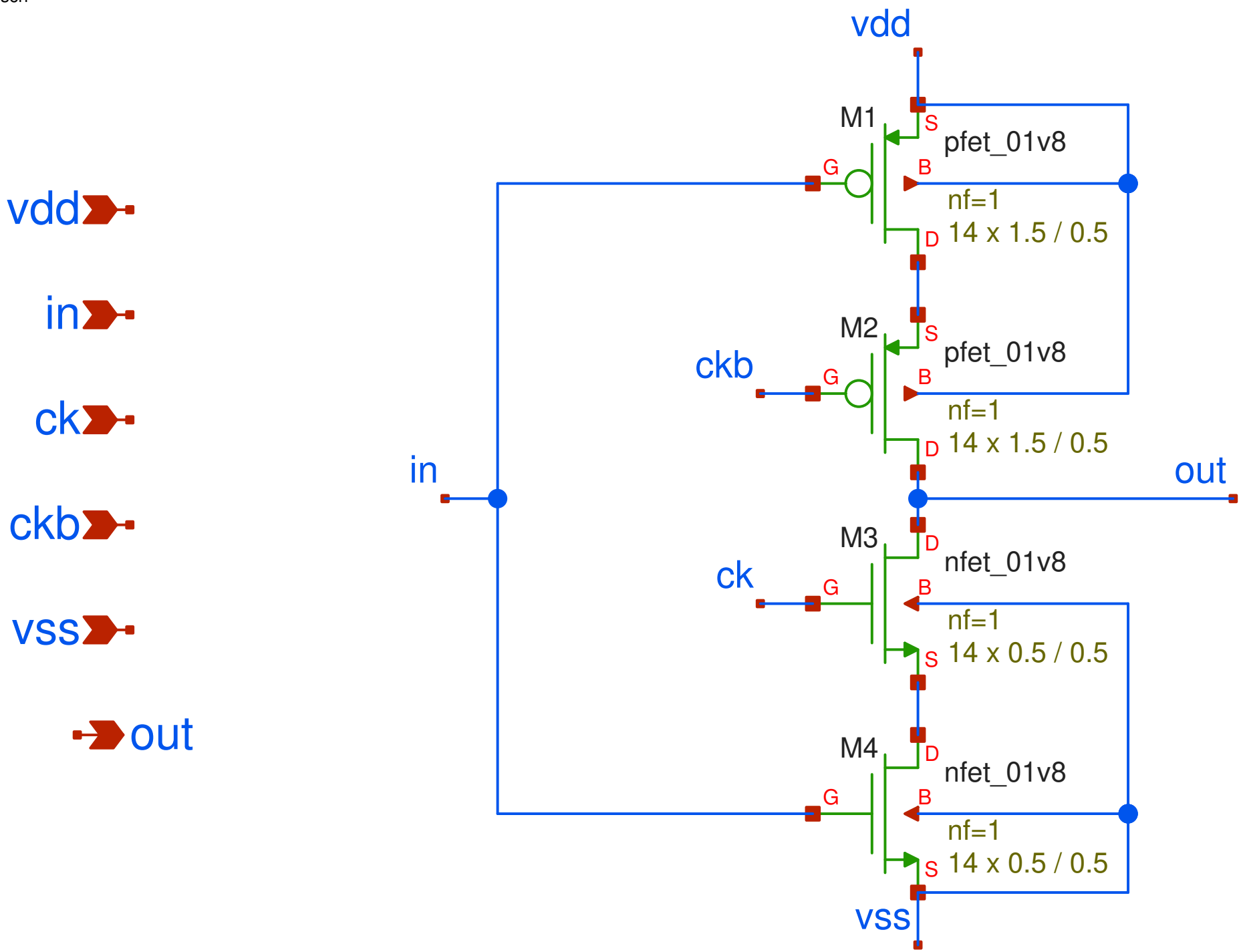
dac_sw_2.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
18 x 1.5 / 0.5
D
M2
S
ckb
pfet_01v8
G
B
nf=1
18 x 1.5 / 0.5
D
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
18 x 0.5 / 0.5
S
M4
D
nfet_01v8
G
B
nf=1
18 x 0.5 / 0.5
S
vss

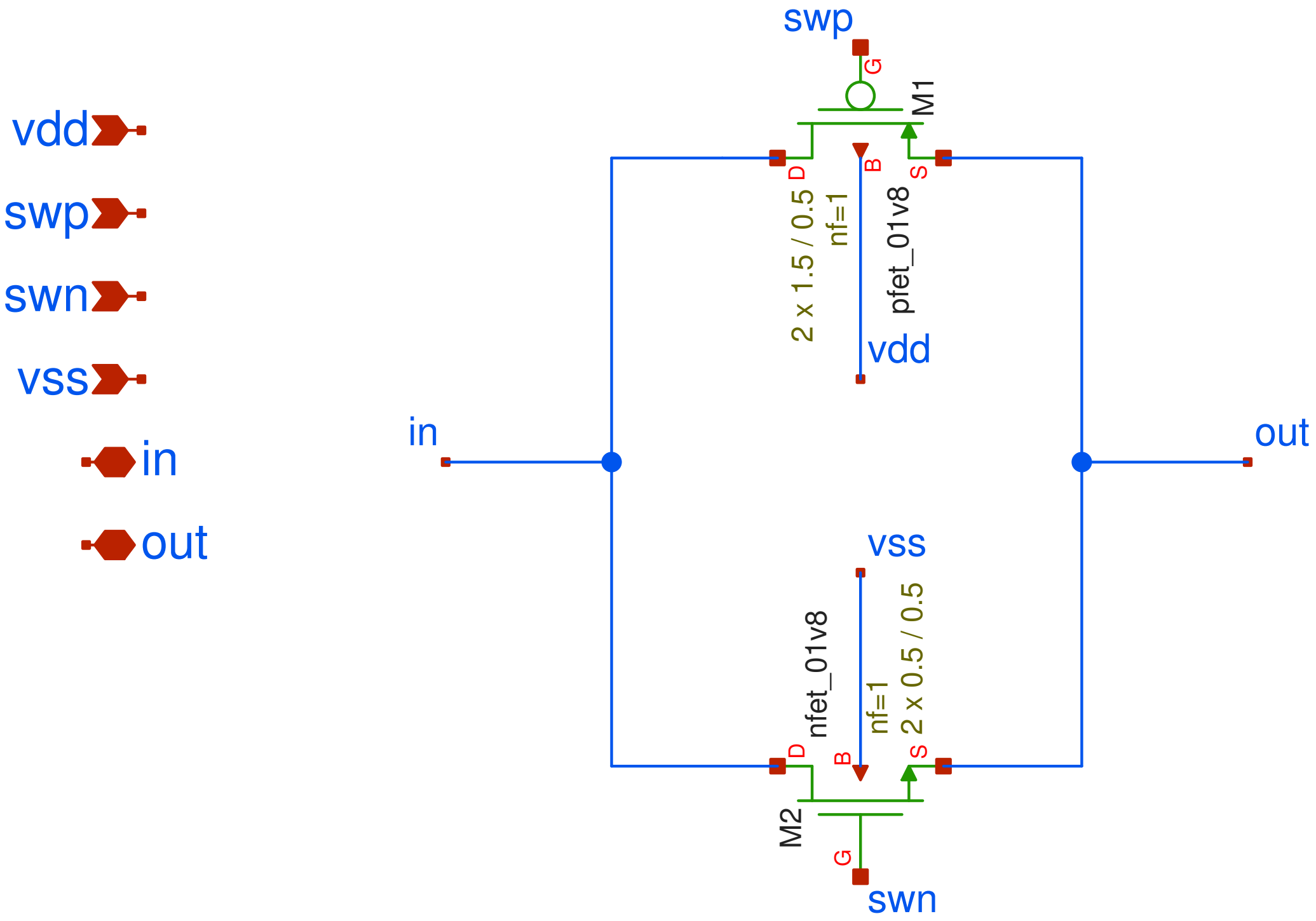
tg_sw_4.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
14 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
14 x 0.5 / 0.5
D
B
S
M2
G
swn

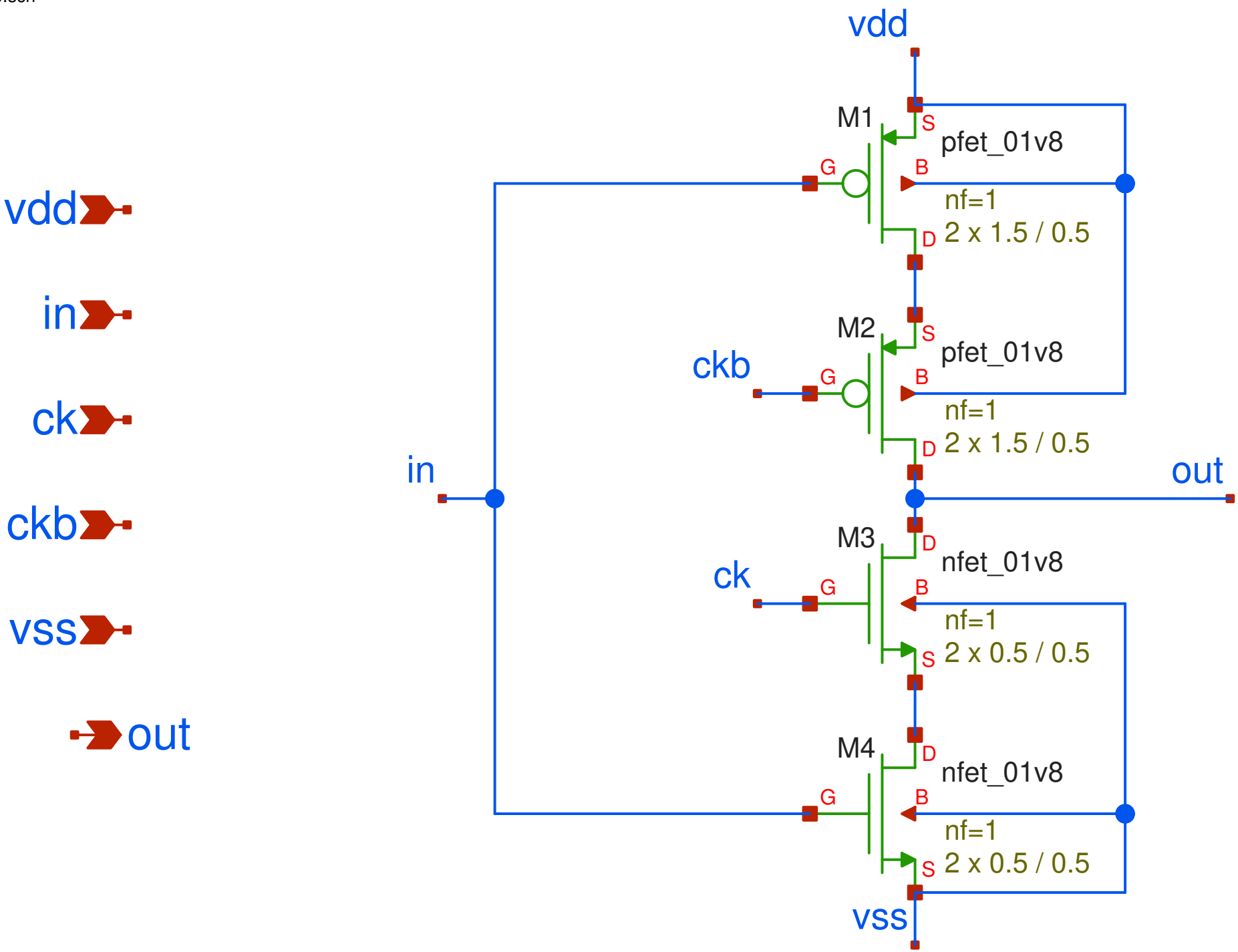
dac_sw_4.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
14 x 1.5 / 0.5
D
M2
S
ckb
pfet_01v8
G
B
nf=1
14 x 1.5 / 0.5
D
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
14 x 0.5 / 0.5
S
M4
D
nfet_01v8
G
B
nf=1
14 x 0.5 / 0.5
S
vss

tg_sw_10.sch


vdd
swp
swn
vss
in
out
swp
G
M1
D
B
S
2 x 1.5 / 0.5
nf=1
pfet_01v8
vdd
in
out
vss
nfet_01v8
nf=1
2 x 0.5 / 0.5
D
B
S
M2
G
swn

dac_sw_10.sch


vdd
in
ck
ckb
vss
out
vdd
M1
S
pfet_01v8
G
B
nf=1
D
2 x 1.5 / 0.5
M2
S
ckb
pfet_01v8
G
B
nf=1
D
2 x 1.5 / 0.5
in
out
M3
D
nfet_01v8
ck
G
B
nf=1
S
2 x 0.5 / 0.5
M4
D
nfet_01v8
G
B
nf=1
S
2 x 0.5 / 0.5
vss