2003-02-27

PRODUKTINFORMATION

Vi reserverar oss mot fel samt förbehåller oss rätten till ändringar utan föregående meddelande

ELFA artikelnr
75-511-61 LCD 16x1 TN LED

S P E C I F I C A T I O N S

Description LCM

Model name GTC-16011-TS6L0C

HEBEI GEM-TECH ELECTRONICS CO., LTD.

Contents

1. BASIC SPECIFICATION

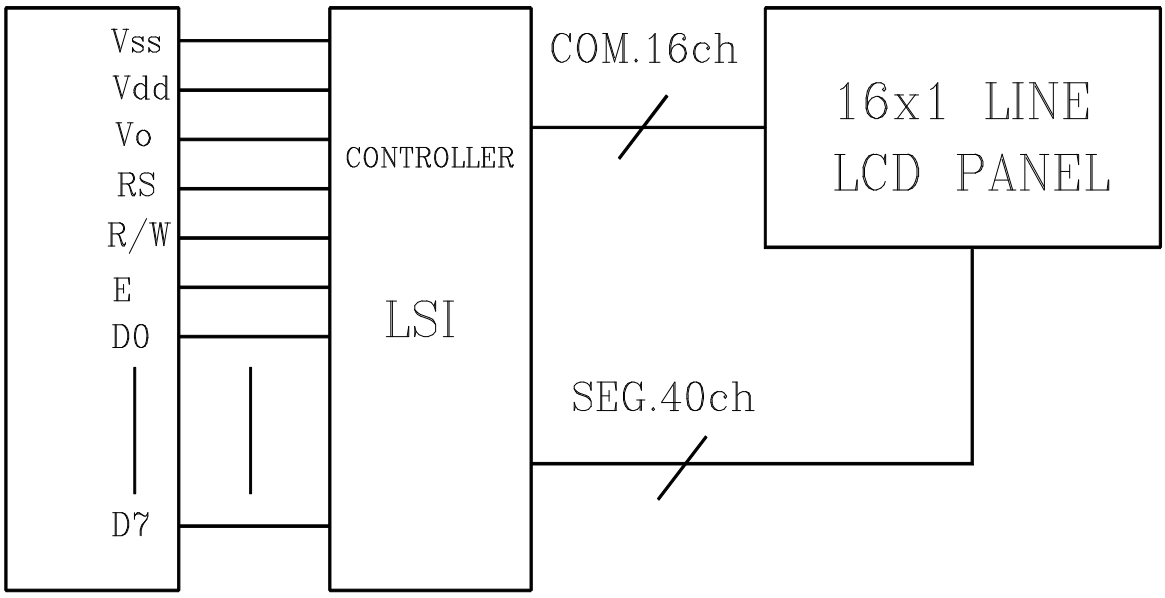
1-1 DISPLAY SPECIFICATIONS

. DISPLAY MODE : TN-TRANSFLECTIVE-POSITIVE
. DISPLAY FORMAT : 16 CHARACTERS X 1 LINES
. INPUT DATA : 8-BITS PARALLEL DATA INPUT FROM A MPU
. MULTIPLEXING : 1/16 DUTY
. VIEWING DIRECTION : 6 O'CLOCK
. DRIVED IC : KS0066U
. BEZEL : 0.6T
. OTHERS :

1-2. MECHANICAL SPECIFICATION

ITEM	SPECIFICATIONS	UNIT	REMARK
DIMENSIONAL OUTLINE	80.0(W)×36.0(H)×10.5MAX.(T)	mm	*REFERENCE DIMENSIONAL OUTLINE
VIEW AREA	64.5(W)×13.8(H)		
EFFECTIVE V/AREA	59.62(W)×6.56(H)		
NUMBER OF CHARACTERS	16 CHARACTERS×1LINES	--	
DOT PITCH	0.63(W)×0.83(H)	mm	
DOT SIZE	0.55(W)×0.75(H)	mm	

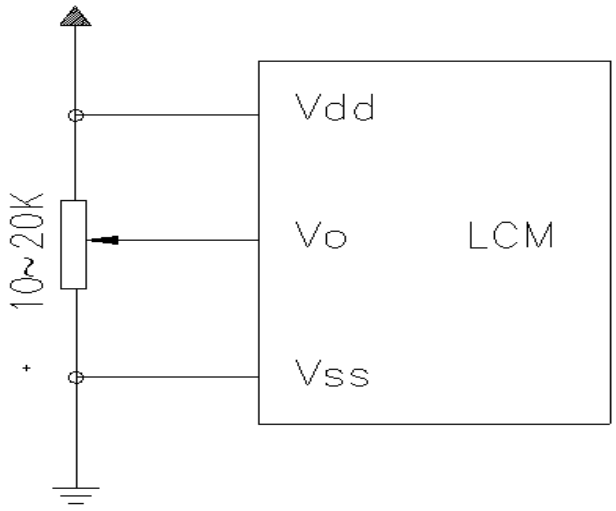
1-3 BLOCK DIAGRAM



1-4 TERMINAL FUNCTIONS

PIN NO	SYMBOL	LEVEL	DESCRIPTION
1	Vss	-	GROUND
2	VDD	-	POWER SUPPLY FOR LOGIC
3	Vo	-	POWER SUPPLY FOR LCD
4	RS	H/L	REGISTER SELECTION
5	R/W	H/L	READ/WRITE
6	E	H, H/L	ENABLE SIGNAL
7	DB0	H/L	DATA BIT0
8	DB1	H/L	DATA BIT1
9	DB2	H/L	DATA BIT2
10	DB3	H/L	DATA BIT3
11	DB4	H/L	DATA BIT4
12	DB5	H/L	DATA BIT5
13	DB6	H/L	DATA BIT6
14	DB7	H/L	DATA BIT7

1-5 POWER SUPPLY CIRCUIT AND CONTRAST ADJUST



2. ABSOLUTE MAXIMUM RATINGS (Ta=25? , VSS=0V)

PARAMETER	SYMBOL	RATINGS			UNITS
		MIN.	TYP.	MAX.	
POWER SUPPLY FOR LOGIC	VDD-Vss	0	-	7.0	V
POWER SUPPLY FOR LCD DRIVER	VDD~ V0	0	-	12.0	V
INPUT VOLTAGE	VIN	Vss	-	VDD	V
OPERATING TEMPERATURE	Topr	0	-	50	^{o}C
STORAGE TEMPERATURE	Tstg	-20	-	70	^{o}C

3.ELECTRICAL & OPTICAL CHARACTERISTICS

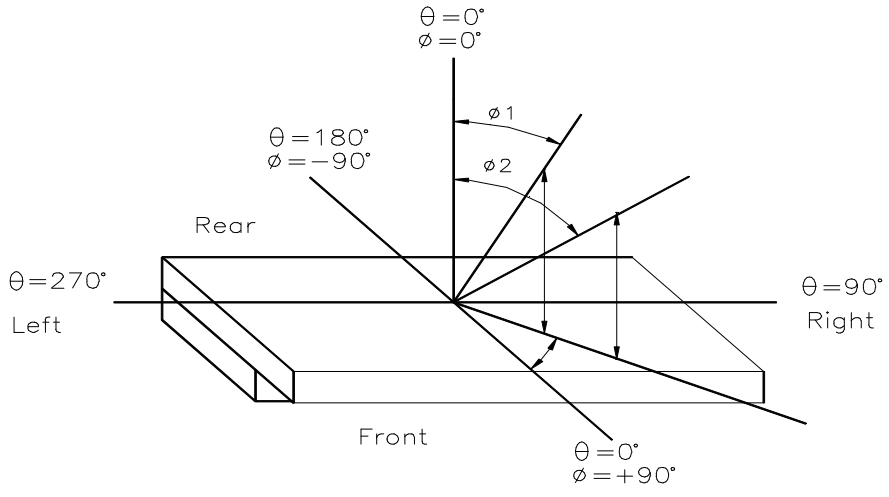
3-1 ELECTRICAL CHARACTERISTICS (Ta=25?)

ITEM	SYMBOL	CONDITION	MIN	TYPE	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	VDD-Vss	———	4.5	5.0	5.5	V
INPUT VOLTAGE	VIH	———	2.2	—	VDD	V
INPUT VOLTAGE	VIL	———	Vss	—	0.6	V
LOGIC CIRCUIT POWER SUPPLY CURRENT	IDD	VDD-Vss=5.0V	——	1.5	2.0	MA
RECOMMENDED LCD DRIVING VOLTAGE	VDD-Vo ϕ=0 θ=0	Ta=25?	——	4.5	——	V
FRAME FREQUNCY	FFLM	-	-	128	-----	HZ

3-2. ELECTRO—OPTICAL CHARACTERISTICS(Ta=25? VDD=5.0±0.25V VOP=3.8V)

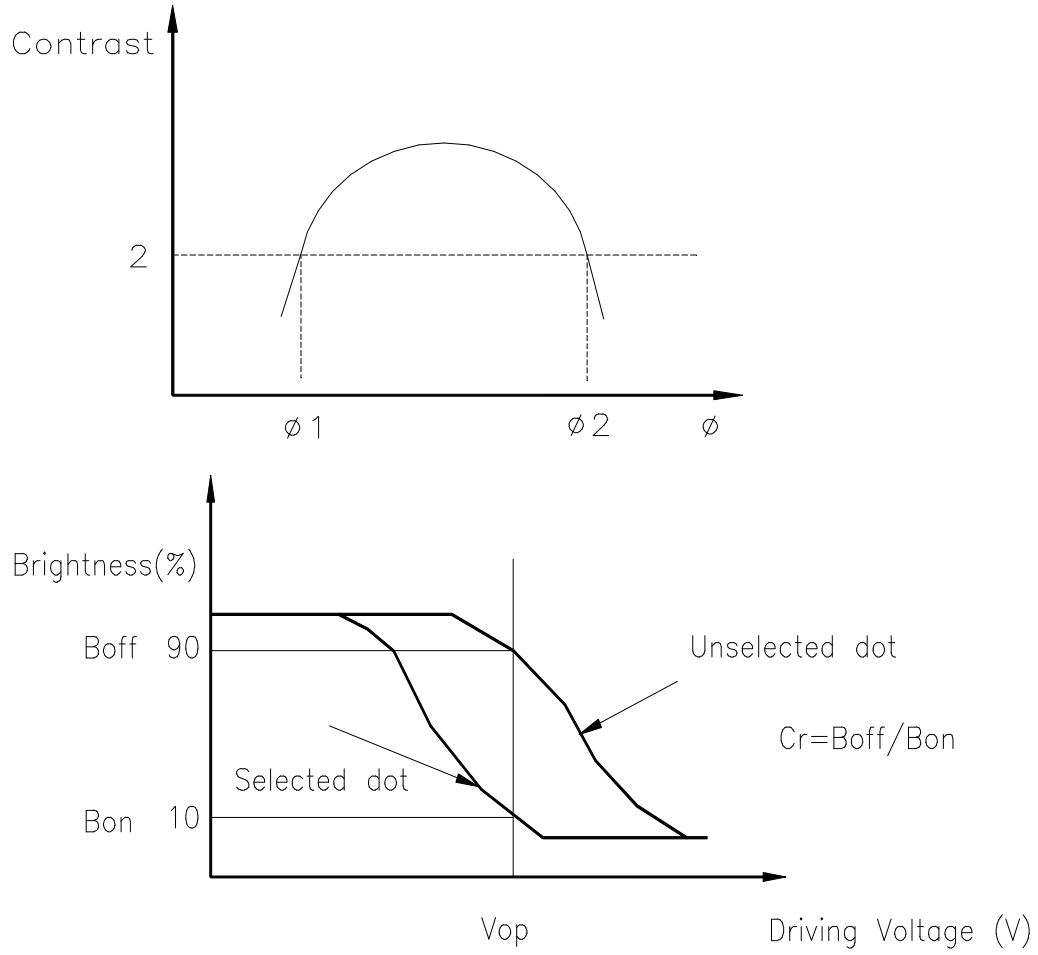
ITEM	SYMBOL	CONDITION	MIN	TYPE	MAX	UNIT
VIEW ANGLE	?φ	θ=0°(Cr≥2) 0°<φ1, φ2<90°	25	30	—	Deg
CONTRAST	Cr	φ=15°,θ=0° 6 O'CLOCK	3	5	—	—
RESPONSE TIME	tr(rise)	6 O'CLOCK	—	150	200	Ms
	tf(fall)	φ=15°,θ=0°	—	200	250	Ms

NOTE1: Definition of Viewing Angle ?,F

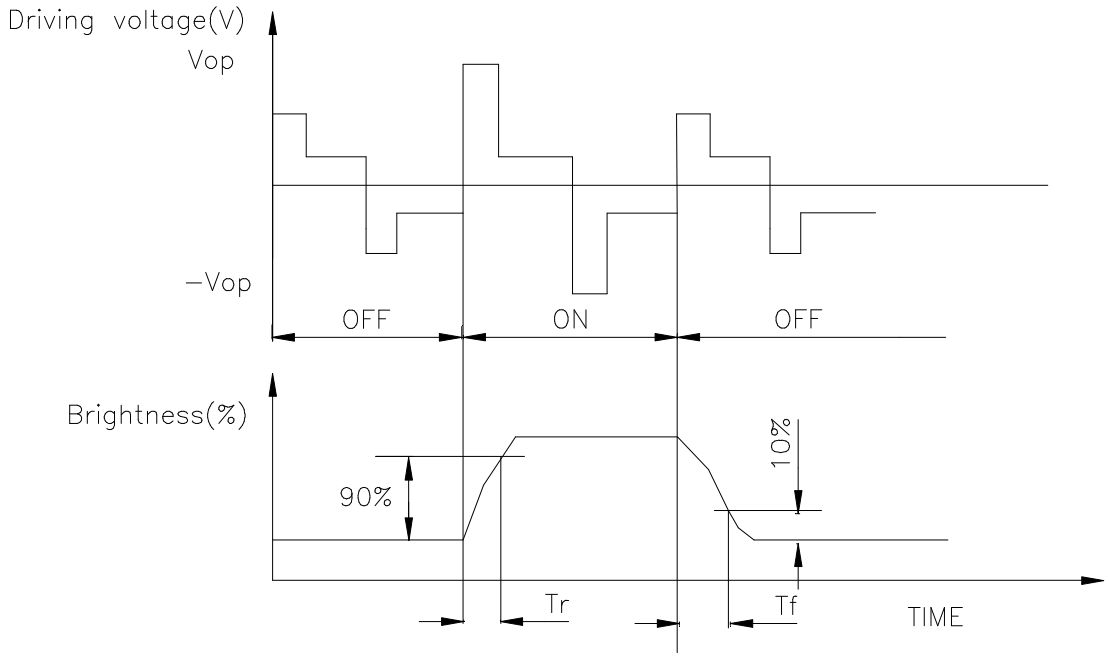


NOTE2: Definition of viewing Angle Range: ?F =|F 2-F 1|

NOTE3: Definition of Contrast



NOTE4: Definition of Response Time



3-3. LED BACK-LIGHT SPECIFICATION

3-3-1.ABSOLUTE MAXIMUM TATINGS(Ta=25 ^{o}C)

ITEM	SYMBOL	RATINGS	UNIT
PEAK FORWARD CURRENT	IF	300	ma
REVERSE VOLTAGE	VR	8	V
POWER DISSIPATION	Po	1.32	W
OPERATING TEMPERATURE	Topr	-20 TO 70	^{o}C
STORAGE TEMPERATURE	Tsto	-40 TO 80	^{o}C
SOLDER TEMPERATURE: 3 SEC. AT 2mm FROM THE REFLECTOR EDGE		260	^{o}C

3-3-2. ELECTRICAL/OPTICAL SPECIFICATIONS:

ITEM	SYMBOL	STANDARD VALUE			UNIT	CONDITIONS
		MIN.	TYP.	MAX.		
LUMINOUS INTENSITY	IV	80	120	-	cd/m2	IF =140ma Ta=25 ^{o}C
PEAK EMISSION WAVELENGTH	?f	571		576	Nm	
SPECTRAL LINE HALF WIDTH	??	-	30	-	Nm	
FORWARD VOLTAGE	VF	-	4.2	4.6	V	
REVERSE CURRENT	IR	-	-	0.2	mA	VR=8V

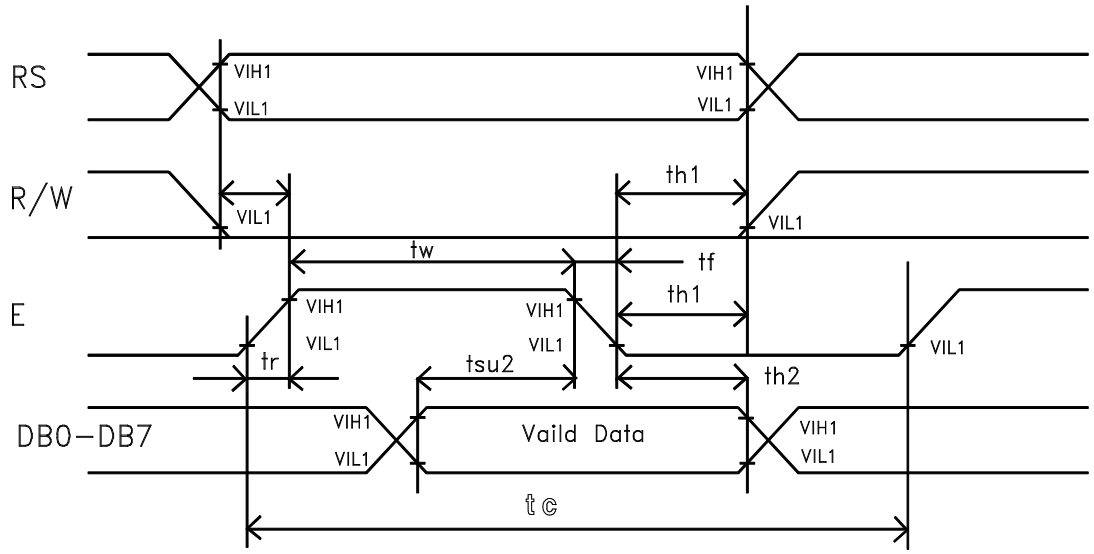
4. TERMINAL CHARACTERISTICS

4-1. TIMING OF WRITE/READ OPERATION(V_{DD}=5.0V ±10%,Ta=0 TO 50 °C)

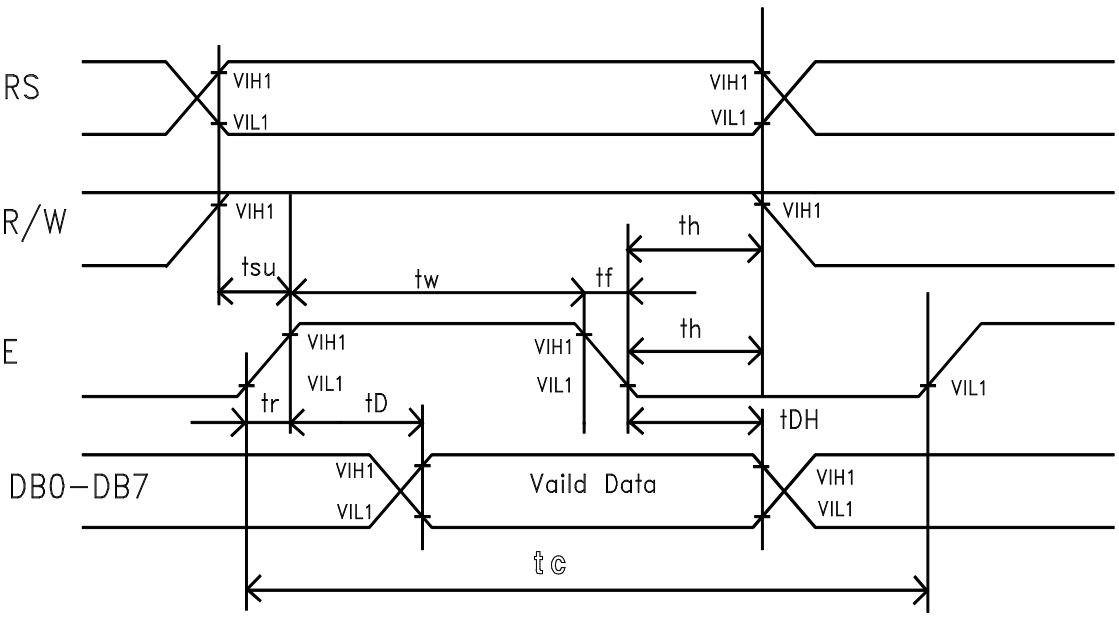
ITEM	SYMBOL	WRITE		READ		UNIT
		MIN.	MAX.	MIN.	MAX.	
ENABLE CYCLE TIME	tc	500	-	500	-	ns
ENABLE PULSE WIDTH	tw	220	-	220	-	
ENABLE RISE/FALL TIME	tr, tf	-	25	-	25	
RS, R/W SET UP TIME	tsu1/tsu	40	-	40	-	
RS, R/W HOLD TIME	th1/th	10	-	10	-	
DATA SET-UP DELAY TIME	tsu2/tD	60	-	60	120	
DATA HOLD/HOLD TIME	th2/tDH	10	-	20	-	

4-2. INTERFACE TIMING CHART

4-2-1. WRITE OPERATION



4-2-2. READ OPERATION



5. FUNCTION DESCRIPTION& INSTRUCTION SET

5-1. FUNCTION DESCRIPTION (KS0066U)

System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bits registers are used.
One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction.
Each internal operation, reading from or writing into RAM, is done automatically.
Thus, after MPU read DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction codes transferred from MPU.
MPU cannot use it to read instruction data.

To select a register, you can use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU write Instruction code into IR)
L	H	Read Busy flag(DB7) and address counter (DB0 to DB6)
H	L	Data Write operation (MPU write data into DR)
H	H	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

BF= “High”, indicates that the internal operation is being processed.
So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = “Low” and R/W = “High” (Read Instruction Operation).
Before executing the next instruction, be sure that BF is not “High”.

Address Counter (AC)

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS= “Low” and R/W= “High”, AC can be read through ports DB0 to DB6.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80X8 bits (80 characters).
DDRAM address is set in the address counter(AC) as a hexadecimal number (Refer to Fig-1.)

MSB LSB

AC6	AC5	AC4	AC3	AC2	AC1	AC0

Figure 1. DDRAM Address

16 character * 1 line

Display position	1	2	……	7	8	9	10	……	15	16
DDRAM address	00H	01H	……	06H	07H	40H	41H	……	46H	47H

CGROM (Character Generation ROM)

CGROM has a 5x8 dots 204 characters pattern and a 5x11 dots 32 characters pattern (Refer to the CGROM Character Code Table)

CGROM has 204 characters pattern of 5x8 dots, and 32 characters pattern of 5x11 dots.

CGRAM (Character Generation RAM)

CGRAM has up to 5x8 dots 8 characters.

By writing font data to CGRAM, user defined characters can be used.

Refer to follow table.

Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)	CGRAM Address	CGRAM Data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 x 0 0 0	0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	x x x 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 0 0	pattern 1
*	* * * * * *	*	*
0 0 0 0 x 1 1 1	1 1 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	x x x 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 0 0	pattern 8

5-2. INSTRUCTION SET

5-2-1. INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. Instructions can be divided largely into four groups:

1) KS0066U function set instructions (set display methods, set data length, etc.)
2) Address set instructions to internal RAM.
3) Data transfer instructions with internal RAM.
4) Others.

The address of the internal RAM is automatically increased by 1.

Note: During internal operation, Busy Flag (DB7) is read "High".

Busy Flag check must be preceded by the next instruction.

When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to "Low".

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC(address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display.

Make the entry mode increment (I/D="High").

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	—

Return home is cursor return home instruction.

Set DDRAM address to "00H" into the address counter.

Return home to its original site and return display to its original status, if shifted.

Counters of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM is decreased by 1.

* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM read (CGRAM read/write) operation or SH = "Low", shifting of entire display is not performed.

if SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "High": shift left, I/D = "Low": shift RIGHT).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display /cursor/blink ON/OFF 1 bit register.

D: display on/off control bit
When D= “High”, entire display is turned on.
When D =“Low”, entire display is turned off, but display data remains in DDRAM,

C: cursor on/off cursor bit
When C = “High”, cursor is turned on.
When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: cursor blink on/off control bit
When B =“High”, cursor blink is on which performs alternately between all the “High” data and when B = “Low”, blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	S/C	R/L	—	—

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When display data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

Shift patterns according to S/C and bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	—	—

DL: interface data length control bit
When DL= “High”, it means 8-bit bus mode with MPU.
When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data twice.
N: display line number control mode is set.
When N= “Low”, 1-line display mode is set.
When N = “High”, 2-line display mode is set.

F: display font type control bit
When F= “Low”, 5 x 8 dots format display mode is set.
When F= “High”, 5 x 11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N=Low), DDRAM address is from “00H” to “27H”.
In 2-line display mode (N=High), DDRAM address in the 1st line is from “00H”to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not.
If the resultant BF is “High”, internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/ decreased by 1, according to the entry mode.

11) Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction if the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.
After read operation, address counter is automatically increased/ decreased by 1 according to the entry mode.
After CGRAM read operation, display shift may not be executed correctly.

Note: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

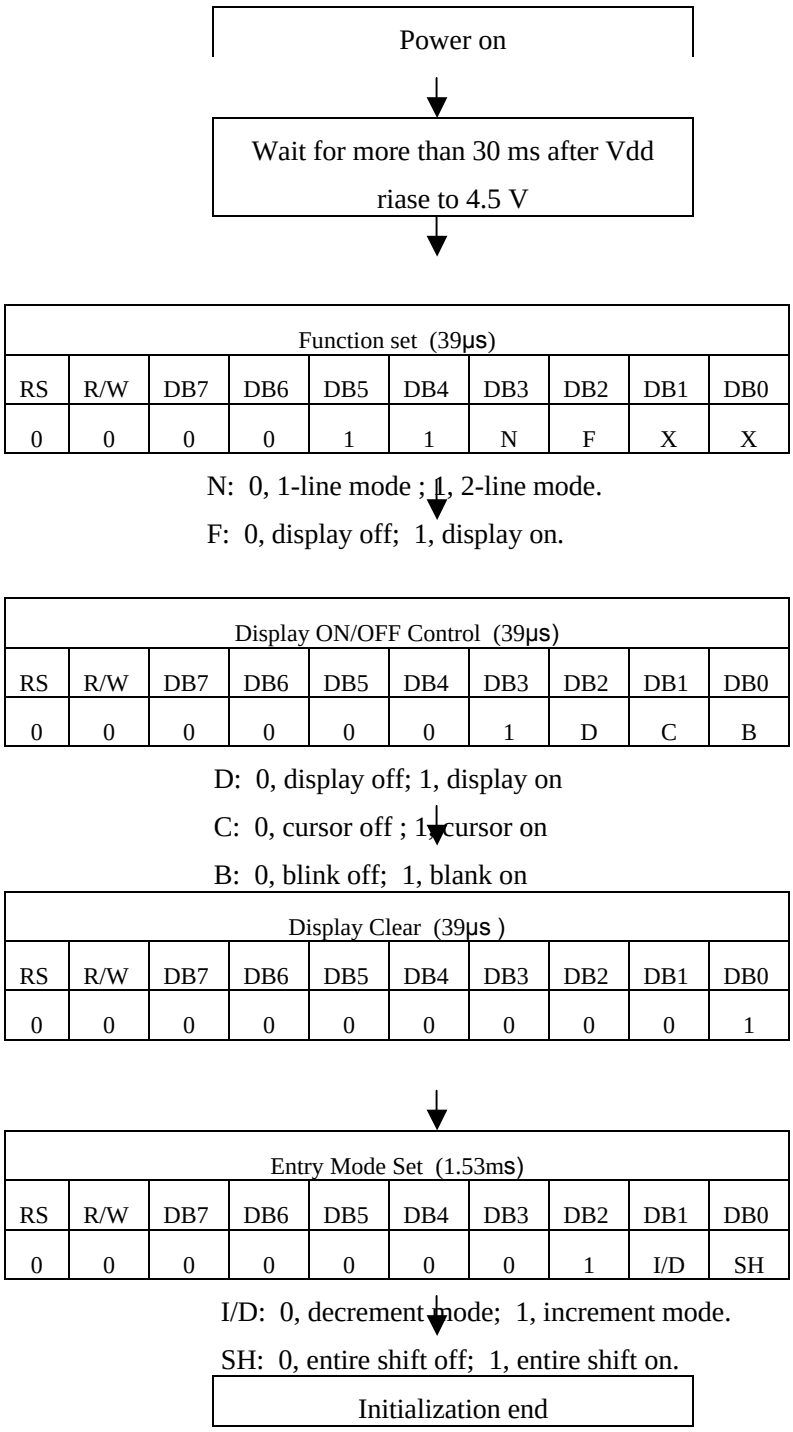
5-2-2. INSTRUCTION

Instruction	Instruction code										Description	Execution time
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		(fosc=270KHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Write 20H to DDRAM and set DDRAM address to 00H from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to 00H From AC and return cursor to its Original position if shifted. The contents of DDRAM are not Changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And enable the shift of entire display.	39us
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39us
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F: 5x11dots/5x8dots)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0us
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

*"-": don't care

5-3 EXAPLES OF DATA TRANSFER OPERATION

5-3-1 8 BIT MODE



5-3-2 4 BIT MODE

Power on

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Wait for more than 30 ms after Vdd riase to 4.5 V

↓

Function set (39μs)									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

N: 0, 1-line mode ; 1, 2-line mode.

F: 0, display off; 1, display on.

↓

Display ON/OFF Control (39μs)									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

D: 0, display off; 1, display on

C: 0, cursor off ; 1, cursor on

B: 0, blink off; 1, blank on

↓

Display Clear (39μs)									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

↓

Entry Mode Set (1.53ms)									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	SH	X	X	X	X

I/D: 0, decrement mode; 1, increment mode.

SH: 0, entire shift off; 1, entire shift on.

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Initialization end

6. CHARACTER FONT TABLE

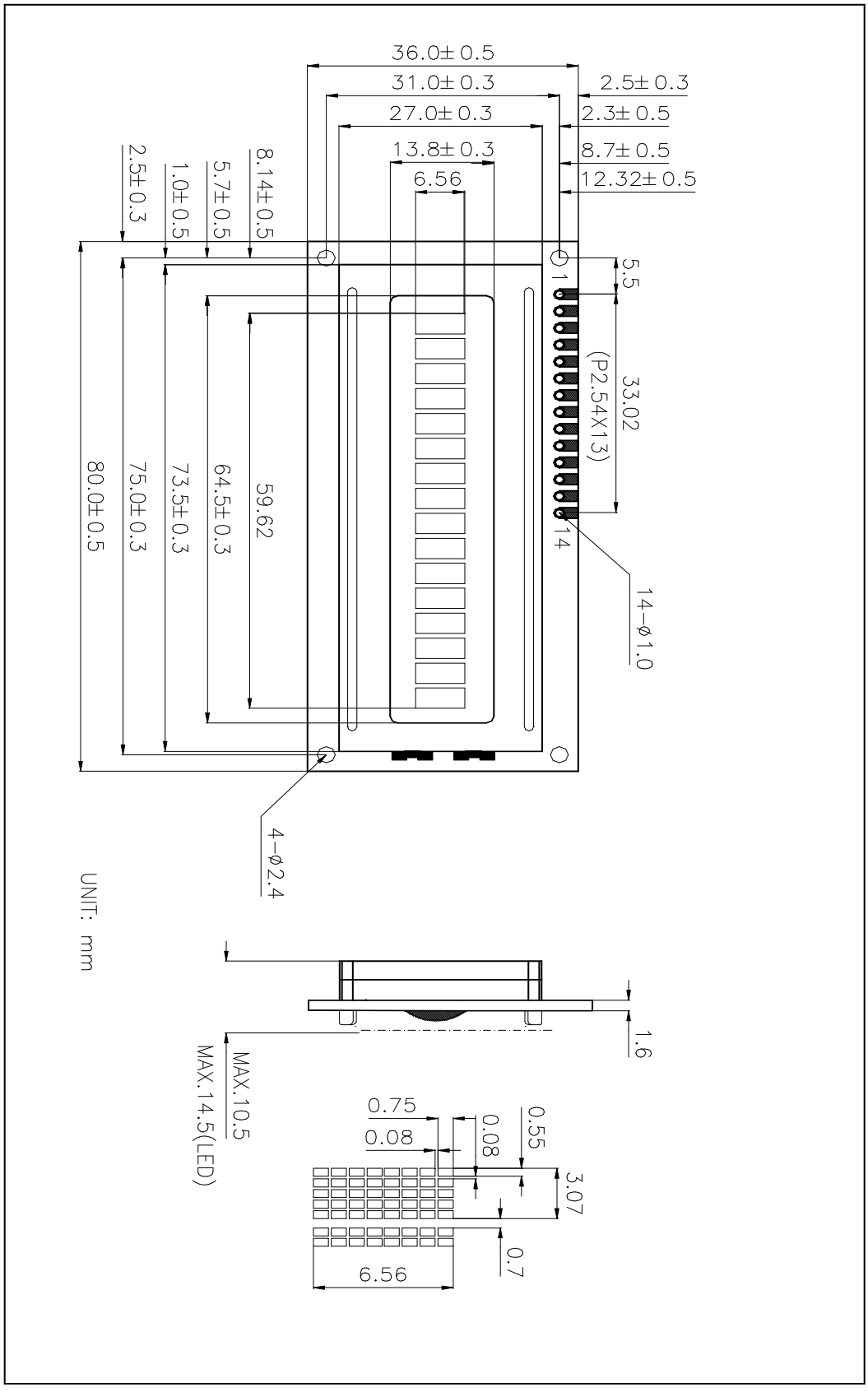
[CORRESPONDENCE BETWEEN CHARACTER CODE AND CHARACTER

PATTERN]

Standard Character Pattern

Thu Jun 05 08:41:48 1997

7. DIMENSIONAL OUTLINE



8. HANDLING PRECAUTION

8-1. MOUNTING METHOD

The panel of the LCD module consists of two thin glass plates with polarizes which easily get damaged since the module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling the LCD modules.

8-2. CAUTION OF LCD HANDLING & CLEANING

When cleaning the display surface. Use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol
-Ethyl alcohol
-Tri chlorotri fluoroethane

Do not wipe the display surface with dry or hard materials that will damage the polarizes surface.

Do not use the following solvent:

-Water
-Ketone
-Aromatics

8-3.CAUTION AGAINST STATIC CHARGE

The LCD modules use COMS LSI drivers. So we recommend that you connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on and ground your body. work/assembly table. And assembly equipment to protect against static electricity.

8-4.PACKAGING

-Modules use LCD elements, and must be treated as such avoid intense shock and falls from a height

-To prevent modules from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

8-5.CAUTION FOR OPERATION

-It is indispensable to drive LCM within the specified voltage limit since the higher voltage than the limit shortens LCM life.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD show dark color in them.

However those phenomena do not mean malfunction or out of order with LCD, which will come back in the specified operating temperature range.

-If the display area is pushed hard during operation. Some font will be abnormally displayed but it resumes normal condition after turning off once.

-A slight dew depositing on terminals is a cause for Electro-chemical reaction resulting in terminal open circuit.

Under the maximum operating temperature, 50%RH or less is required

8-6 STORAGE

In the case of storing for a long period of time (for instance, for years) for the purpose or replacement use. the following ways are recommended

-Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside

in it, and with no desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is, keeping temperature in the specified storage temperature range.

-Storing with no touch on polarizes surface by the anythingelse.

(it is recommended to store them as they have been contained in the inner container at the time of delivery from us.

8-7.SAFETY

-It is recommendable to crash damaged or unnecessary LCD into pieces and wash off liquid crystal by using solvents such as acetone and ethanol, which should be burned up later.

-When any liquid crystal leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

9.PRECAUTION FOR USE

9-1.A limit sample should be provided by the both parties on an occasion when the both parties agree its necessity.

Judgement by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

9-2.On the following occasions, the handling of problem should be decided through discussion and agreement between representative of the both parties

-When a question is arisen in this specification.

-When a new problem is arisen which is not specified in this specifications.

-When an inspection specification change or operating condition change in customer is reported to GEM-TECH, and some problem is arisen in this specification due to the change.

-When a new problem is arisen at the customer’s operating set for sample evaluation in the customer size.