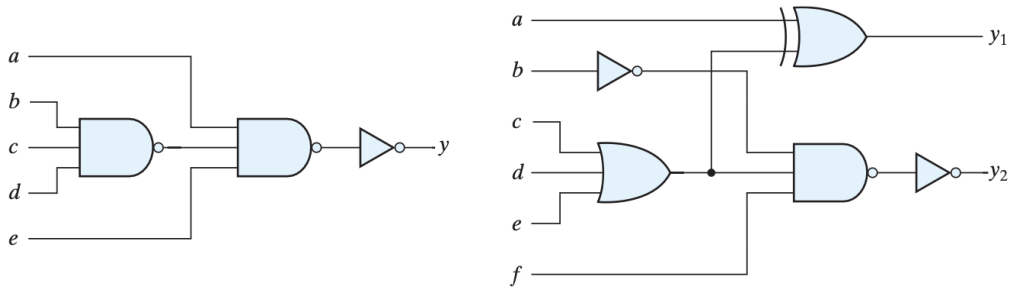
CSCI 160 Spring 2025
Final Exam
Version 1

Name:	
EMPLID:	

◆ Part I ◆



1. Derive the Boolean expressions for y, y_1, and y_2 in terms of the inputs.
2. How many rows and columns are in the truth table for each circuit?

◆ Part II ◆

1. Using three half adders ONLY, design a circuit that adds one to (increments) a 3-bit binary number.

2. Using half adders and external gates, design a circuit that subtracts one from (decrements) a 3-bit binary number.

3. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. Given this verbal description, provide a truth table and K-maps. Derive the minimized sum-of-products expressions for the output variables and draw the corresponding logic diagram(s).

◆ Part III ◆

1. Assume that an exclusive-OR gate has a propagation delay of 20 ns, NAND and OR gates have a propagation delay of 10 ns, and inverters have a propogation delay of 5 ns. **What is the total propagation delay (in nanoseconds) for each circuit from Part I of the exam?**

2. Design a four-input priority encoder with inputs as in Table 4.8, but with input D_0 having the highest priority and input D_3 the lowest priority.

3. The adder–subtractor circuit of Fig. 4.13 has the following values for mode input M and data inputs A and B.

	M	A	B
(a)	0	0111	0110
(b)	0	1000	1001
(c)	1	1100	1000

   In each case, determine the values of the four SUM outputs, the carry C, and overflow V. Show your work to receive full credit.

◆ Part IV ◆

1. Implement the following Boolean function with a 4 x 1 MUX:
   $F_1(A, B, C) = \Sigma(1, 3, 4)$

2. Implement the following Boolean function with a 4 x 1 MUX and external gates:
   $F_1(A, B, C, D) = \Sigma(1, 3, 4, 12, 13, 14, 15)$

3. Using a decoder and external gates, design the combinational circuit defined by the three following Boolean functions:

   $F_1 = x'yz' + xz$

   $F_2 = xy'z' + x'y$

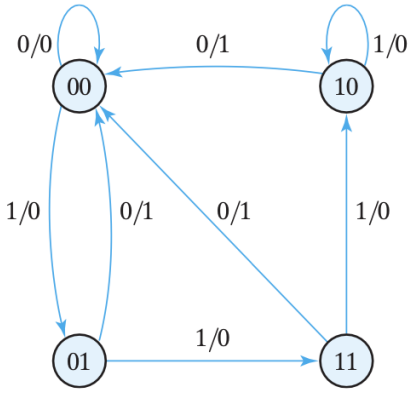
   $F_3 = x'y'z' + xy$

◆ Part V ◆

1. What is the difference between a combinational and sequential circuit?
2. What is a flip-flop? How many flip-flops are needed to store 4 bits of information?
3. What is the difference between a latch and a flip-flop?
4. Draw one clock pulse. Label the positive edge and negative edge transitions on the clock pulse.

♦ Extra Credit ♦

1. Implement a full adder with two 4 x 1 multiplexers.
2. Determine the state transitions and output sequence that will be generated when an input sequence of 010110111011110 is applied to the circuit and it is initially in the state 00.



♦ Reference Sheet ♦

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6

(a)

x \ yz	00	01	11	10
0	m_0 $x'y'z'$	m_1 $x'y'z$	m_3 $x'yz$	m_2 $x'yz'$
1	m_4 $xy'z'$	m_5 $xy'z$	m_7 xyz	m_6 xyz'

(y spans 11 and 10; z spans 01 and 11; x spans row 1)

(b)

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}

(a)

wx \ yz	00	01	11	10
00	m_0 $w'x'y'z'$	m_1 $w'x'y'z$	m_3 $w'x'yz$	m_2 $w'x'yz'$
01	m_4 $w'xy'z'$	m_5 $w'xy'z$	m_7 $w'xyz$	m_6 $w'xyz'$
11	m_{12} $wxy'z'$	m_{13} $wxy'z$	m_{15} $wxyz$	m_{14} $wxyz'$
10	m_8 $wx'y'z'$	m_9 $wx'y'z$	m_{11} $wx'yz$	m_{10} $wx'yz'$

(y spans 11 and 10; x spans 01 and 11; z spans 01 and 11; w spans 11 and 10)

(b)

◆ Reference Sheet ◆

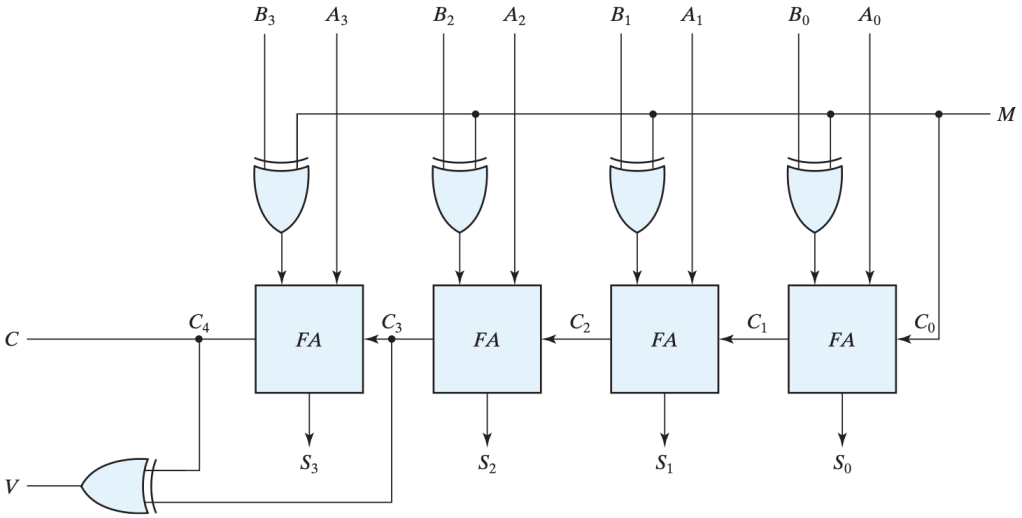


FIGURE 4.13
Four-bit adder–subtractor (with overflow detection)

Table 4.8
Truth Table of a Priority Encoder

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1