![MtM+ Technology logo]

MtM+ Technology

M203

WLAN/BT SiP Module - WLAN 802.11 b/g/n
- Bluetooth 2.1+EDR, 3.0HS, 4.0LE

Preliminary DATASHEET
9th January, 2018

Table of Contents

1 Product Brief

The M203 is a highly integrated wireless SiP module that support 1-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) STA mode with integrated Bluetooth 2.1/4.2 controller, SDIO (SDIO 1.1/2.0/3.0) interface, and HS-UART mixed interface. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and RF in s single chip. M203 provides a complete solution for a high-performance integrated wireless and Bluetooth device.

For the software and driver development, we provide extensive technical document and reference software code for the system integration.

Hardware evaluation kit and development utilities will be released base on listed OS and processors to OEM customers.

KEY FEATURES

- 10.0 x 10.0 mm LGA module
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 1x1, Wave-2 compliant with MU-MIMO STA mode
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 100MHz (SDR50 and DDR50)
- Compatible with Bluetooth v2.1+EDR
- Support Bluetooth 4.2 features
- CHS-UART interface for Bluetooth data transmission compliant with H4 and H5 specification
- PCM interface for audio data transmission via Bluetooth controller
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate

2 Features

Feature List: Wi-Fi

- 10.0x10.0mm LGA module
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 1x1, Wave-2 compliant with MU-MIMO STA mode
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Host Interface: Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 100MHz (SDR50 and DDR50)
- Standards Supported
  - IEEE 802.11a/b/g/n/ac compatible WLAN
  - IEEE 802.11e QoS Enhancement (WMM)
  - IEEE 802.11e QoS Enhancement (WMM)IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
  - IEEE 802.11h DFS, TPC, Spectrum, Measurement
- MAC Features
  - Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
  - Low latency immediate Block Acknowledgement (BA)
  - Long NAV for media reservation with CF-End for NAV release
  - Maximum PHY data rate up to 86.7Mbps using 20MHz bandwidth, 200Mbps using 40MHz bandwidth, and 433.3Mbps using 80MHz bandwidth
  - Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
  - Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.
  - G-SPI interface for configurable endian for WLAN
  - Complies with HS-UART with configurable baud rate for Bluetooth
  - WAPI (Wireless Authentication Privacy Infrastructure) certified.
  - Cisco Compatible Extensions (CCX) for WLAN devices
  - PHY-level spoofing to enhance legacy compatibility
  - MIMO power saving mechanism
  - Channel management and co-existence
  - Multiple BSSID feature allows the RTL8821CS to assume multiple MAC identities when used as a wireless bridge
  - Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
  - Wi-Fi Direct supports wireless peer to peer applications
- Peripheral Interfaces
  - Up to 15 General Purpose Input/output pins
  - Three configurable LED pins (mux with GPIO pins)
- PHY Features
  - IEEE 802.11ac OFDM
  - IEEE 802.11n OFDM
  - 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
  - Support 2.4Ghz and 5Ghz band channels
  - Short Guard Interval (400ns)
  - Sounding packet.
  - DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
  - OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
  - Wi-Fi NAN (Neighbourhood Area Network) support
  - W-F-i FTM (Fine Time Measurement) supported
  - Wi-Fi TDLS (Tunnelled Direct Link Setup) supported
  - CCA on secondary through RTS/CTS

handshake.

- Backward compatible with 802.11a/b/g devices while operating at 802.11n data
- Support TCP/UDP/IP checksum offload
- Generates 40MHz clock for peripheral chip
- Single external power source 3.3V only
- Maximum data rate 54Mbps in 802.11g, 150Mbps in 802.11n and 433Mbps in 802.11ac.
- Switch diversity used for DSSS/CCK
- Support STBC receiving
- Support LDPC transmitting
- Hardware antenna diversity
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Feature List: Bluetooth

- Controller
  - Compatible with Bluetooth v2.1+EDR
  - Support Bluetooth 4.2 features
  - CHS-UART interface for Bluetooth data transmission compliant with H4 and H5 specification
  - PCM interface for audio data transmission via Bluetooth controller
  - Integrated MCU to execute Bluetooth protocol stack
  - Supports all packet types in basic rate and enhanced data rate
- Transceiver
  - Fast AGC control to improve receiving dynamic range
  - Supports AFH to dynamically detect channel quality to improve transmission quality
  - Integrated internal Class 1, Class 2, and Class 3 PA
- Peripheral Interfaces
  - General Purpose Input/output (8 pins)
  - 4-wire EEPROM control interface (93C46)
  - Three configurable LED pins
  - Supports SCO/eSCO link (allows one link for

PCM interface and three links for HS-UART)
- Supports piconets in a scatternet
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff/Sniff Sub-rating)
- Enhanced BT/WLAN Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management
- Flexible CRYSTAL frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support CRYSTAL or external clock input

3 Block Diagram

Single-Band 11n (1x1) Solution and Integrated Bluetooth Controller with dual Antenna
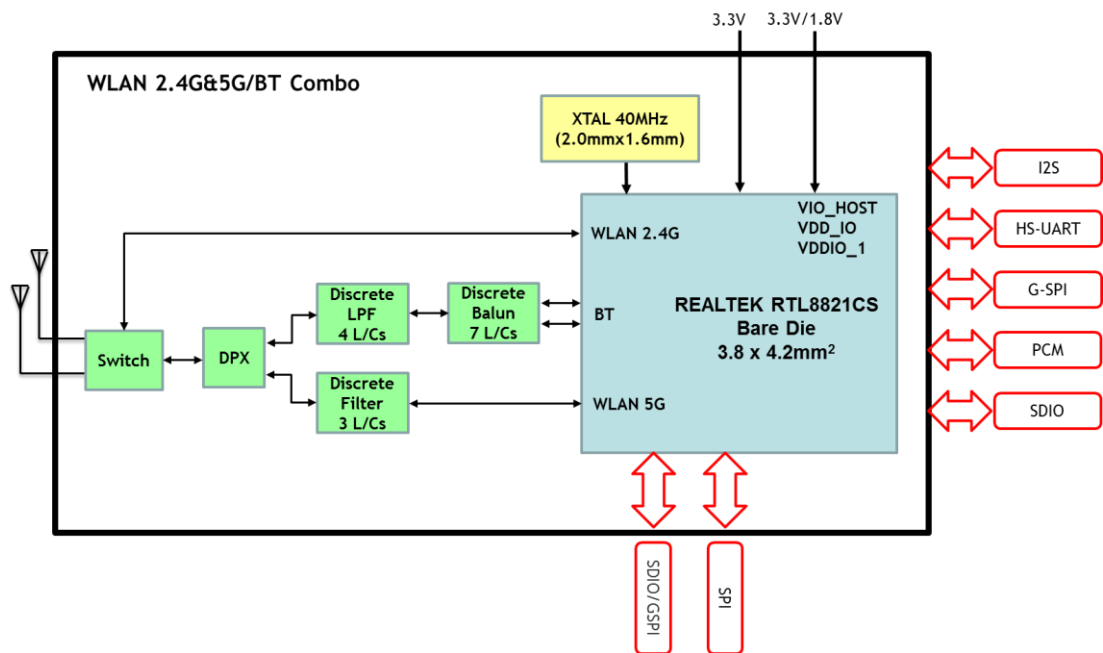
Single-Band 11n (1x1) Solution and Integrated Bluetooth Controller with single Antenna

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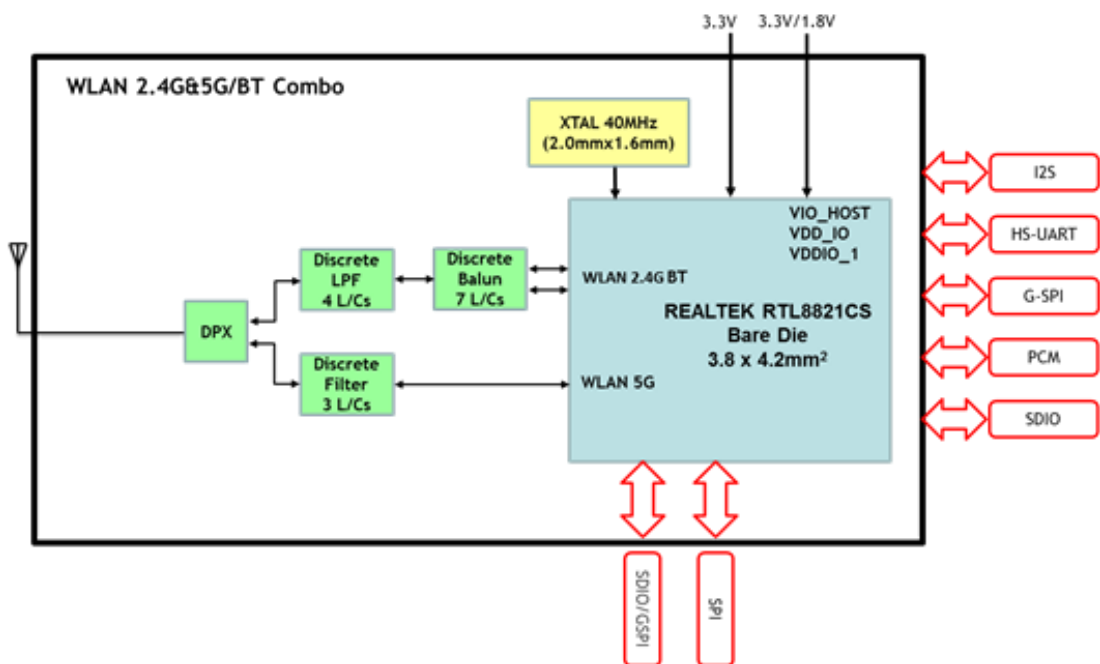
4 Technical Specifications

4.1 Temperature Limit Rating

Item	Min	Max	Unit
Storage Temperature	-55	125	$^{\circ}$C
Ambient Operation Temperature	0	70	$^{\circ}$C
Junction Temperature	0	125	$^{\circ}$C

4.2 Power Supply Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
VD33	3.3V I/O Supply Voltage	3	3.3	3.6	V
VD10	1.5V Supply Voltage	0.945	1.05	1.155	V

4.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

4.4 Power Consumption
4.4.1 Wi-Fi

Power Source 3.3V		Power Consumption	Unit
Radio off (IPS)			
Disable (IPS)			
5G	Transmit@VHT80,11ac		
	Receive@VHT80,11ac		
	Transmit@VHT40,11ac		
	Receive@VHT40,11ac		
	Transmit@VHT20,11ac		
	Receive@VHT20,11ac		
	Transmit@HT40,11n		
	Receive@HT40,11n		
	Transmit@HT20,11n		
	Receive@HT20,11n		
	Transmit@54M,11a		
	Receive@54M,11a		
2G	Transmit@HT40,11n		
	Receive@HT40,11n		
	Transmit@HT20,11n		
	Receive@HT20,11n		
	Transmit@54M,11g		
	Receive@54M,11g		
	Transmit@11M,11b		
	Receive@11M,11b		

4.4.2 Bluetooth

Item	3.3V Current	Unit	Note
Peak Operating(TX): OPP TX			* WLAN Power down mode
Receive: OPP RX			* WLAN Power down mode
BT LPS			* WLAN Power down mode
Page Scan (Interval: 1.28s)			* WLAN Power down mode
Power down			

4.5 Wi-Fi Specification
4.5.1 TX Performance

Band	Mode	Condition	EVM (dB)		Output Power (dBm)	
			Typical	Max	Typical	Min
5G	11ac	MCS9, 80 MHz, CH 155	-35.87	-32	12.24	10
		MCS0, 80 MHz, CH 155	-25.77	-5	16.04	16
	11n	MCS7, 40 MHz, CH 159	-33.04	-27	13.47	12
		MCS0, 40 MHz, CH 159	-23.29	-5	16.24	16
	11a	OFDM, 54 Mbps, CH 165	-29.6	-25	14.39	13
		OFDM, 24 Mbps, CH 165	-25	-16	17.05	17
2G	11n	MCS7, 40 MHz, CH 11	-35.09	-27	14.04	13
		MCS0, 40 MHz, CH 11	-24.96	-5	18.26	18
		MCS7, 20 MHz, CH 13	-33.47	-27	14.2	13
		MCS0, 20 MHz, CH 1	-23.84	-5	18.03	18
	11g	OFDM, 54 Mbps, CH 13	-31.17	-25	15.2	14
		OFDM, 6 Mbps, CH 1	-23.15	-5	18.24	18
	11b	OFDM, 11 Mbps, CH 14	5.26	8	17.41	16
		OFDM, 1 Mbps, CH 6	1.62	8	17.22	16

4.5.2 RX Performance

Band	Mode	Condition	Typical	Max	Unit
5G	11ac	MCS9, BW 80 MHz, CH 155, 10% PER	-59	-51	dBm
		MCS0, BW 80 MHz, CH 155, 10% PER	-83.5	-76	dBm
	11n	MCS7, BW 40 MHz, CH 155, 10% PER	-67.5	-61	dBm
		MCS0, BW 40 MHz, CH 155, 10% PER	-86	-79	dBm
	11a	Rate 54Mbps ,20 MHz, CH 165, 10% PER	-73	-65	dBm
		Rate 6Mbps, BW 20 MHz, CH 165, 10%, PER	-89.5	-82	dBm
2G	11n	MCS7, BW 40 MHz, CH 11, 10% PER	-69.5	-64	dBm
		MCS0, BW 40 MHz, CH 11, 10% PER	-88.5	-82	dBm
		MCS7, BW 20 MHz, CH 13, 10% PER	-72.5	-64	dBm
		MCS0, BW 20 MHz, CH 13 10% PER	-91	-82	dBm
	11g	Rate 54Mbps, BW 20 MHz, CH 13, 10%, PER	-75	-65	dBm
		Rate 6Mbps, BW 20 MHz, CH 13, 10%, PER	-92	-82	dBm
	11b	CCK, Rate 11Mbps, BW 20MHz, CH 13, 10%, PER	-88	-76	dBm
		CCK, Rate 1Mbps, BW 20MHz, CH 13, 10%, PER	-96.5	-97.5	dBm

4.6 Bluetooth Specification

4.6.1 TX Performance

| Mode	Condition	Min	Typical	Max	Unit
BR TX Power	BR Transmitter Output Power	-6	5.8	+20	dBm
EDR2 Max TX Power	EDR2 Transmitter Output Power	-4	-2.5	+1	dBm
EDR3 Max TX Power	at 5% DEVM rms	-4	-2.5	+1	dBm
BLE Max TX Power	EDR3 Transmit Output Power	-10	4.7	+20	dBm
Min TX Power	at 5% DEVM rms	--	-15.2	4	dBm
Power Control Step	BLE Transmit Output Power	--	4.5	8	dB
BR Adj Channel Power	Minimum Transmit Power	--	-48	-20	dBm
EDR Adj Channel Power	Control Setting	--	-30	-20	dBm
EDR Adj Channel Power	From Max to Min Power	26	45	TBD	dB
BR Modulation Characteristics	[M-N] = 2 / [M-N]>3	0.8	0.89	-	
EDR Modulation Accuracy	[M-N] = 2 / [M-N]>3	--	0.053	0.2	
	PTX-26 dB – PTXref [M-N] = 1	--	0.101	0.35	
	$\triangle$f2avg / $\triangle$f1avg	--	0.04	0.3	
BLE Modulation Characteristics	RMS DEVM	0.8	0.88		

4.6.2 RX Performance

Mode	Condition	Min	Typical	Max	Unit
Sensitivity					
BR RX Sensitivity	BER < 0.1%	--	-90	-85	dBm
EDR2 RX Sensitivity	BER < 0.01%	--	-90	-87	dBm
EDR3 RX Sensitivity	BER < 0.01%	--	-87	-80	dBm
BLE RX Sensitivity	PER < 30.8%	--	-90	-87	dBm
Maximum Input Level					
BR Max RX Level	BER < 0.1% – RCV/CA/06/C	-15	-2	--	dBm
EDR2 Max RX Level	BER < 0.1% – RCV/CA/10/C	-15	-2	--	dBm
EDR3 Max RX Level	BER < 0.1% – RCV/CA/10/C	-15	-2	--	dBm
BLE Max RX Level	PER < 30.8% – RCVLE/CA/06/C	-5	-1	--	dBm

5 Dimensions

The size and thickness of the M203 module 10.0mm (W) x 10.0mm (L) x 1.3mm (H):
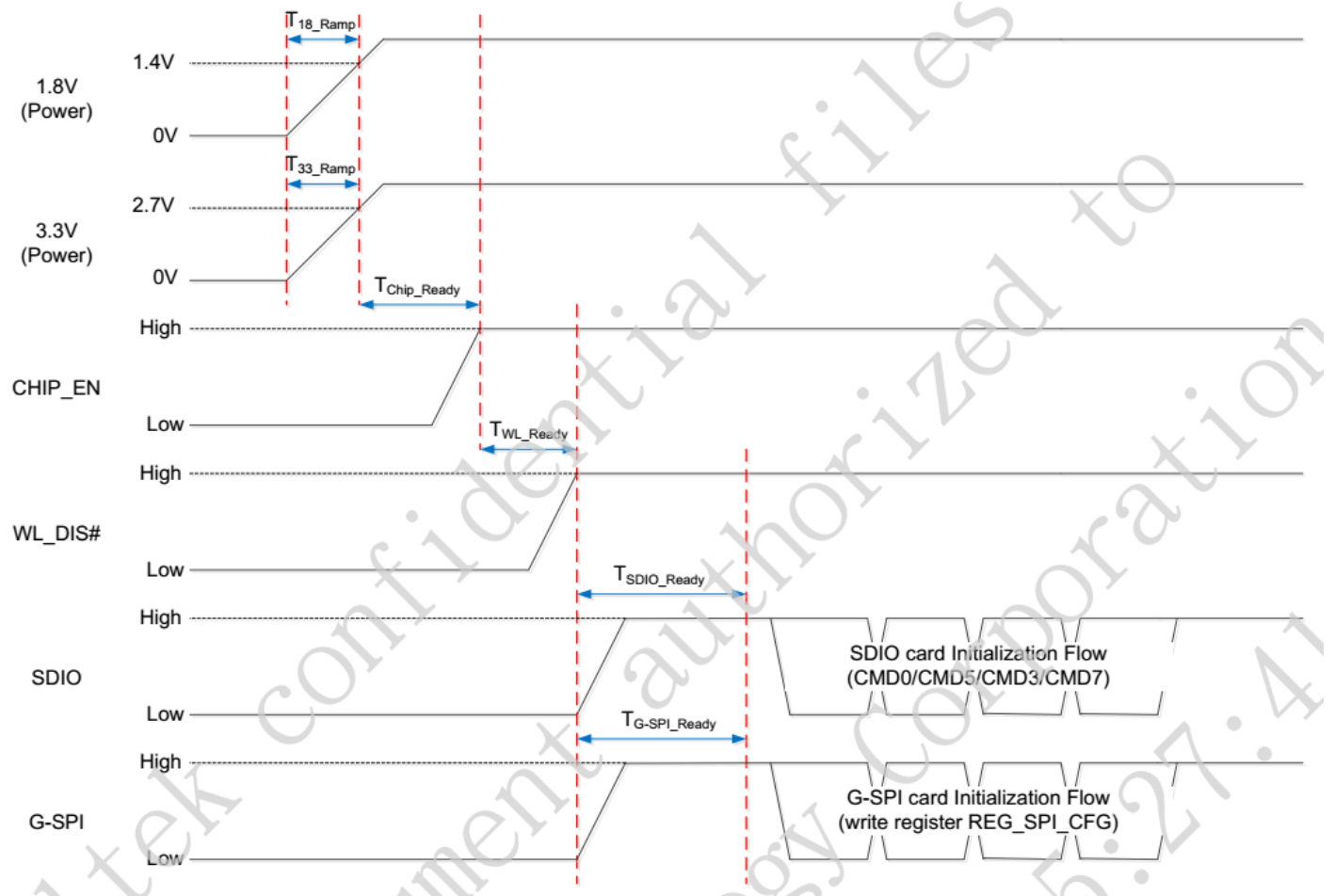
Top-View:

(TOP VIEW)
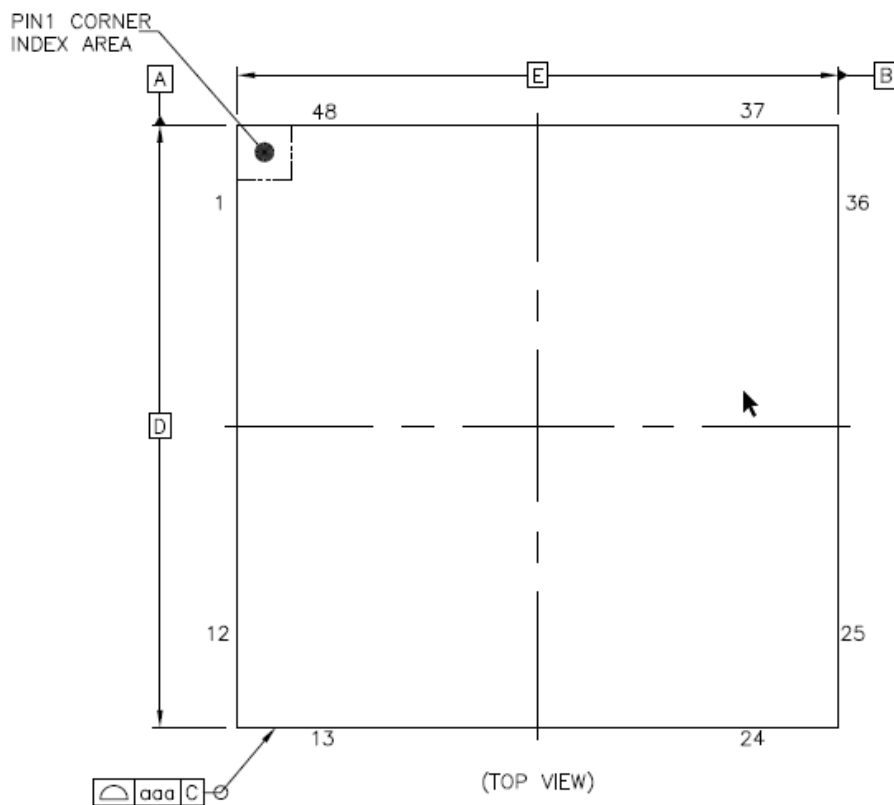
6 Pin Assignment

The foot print dimension and pin definition is defined as below:

No	Pin Name	Pin Type	Description
1	GND	P	Ground (0V)
2	VDD33	P	Power supply
3	GND	P	Ground (0V)
4	WL_5G_BT	I/O	WLAN 5G / BT RF I/O
5	GND	P	Ground (0V)
6	GND	P	Ground (0V)
7	WL_2G_ANT	I/O	WLAN 2G RF I/O
8	GND	P	Ground (0V)
9	TCXO_IN	I	26M/40MHz OSC Input Input of 26M/40MHz Crystal Clock Reference
10	COEX_RXD / GPIO6	I	LTE_RXD
11	COEX3 / GPIO7	I	LTE_COEX3
12	COEX_TXD / GPIO12	O	LTE_TXD
13	GND	P	Ground (0V)
14	SD_RESET / GPIO9	I	This Pin Can Externally Shutdown the RTL8821CS WLAN function when SD_RESET is pulled low. When this pin is pulled low, SDIO/G-SPI interface will be disabled.
15	VDD_IO	P	VDD for GPIO6,GPIO7,GPIO9,GPIO10,GPIO12,GPIO13, GPIO14,GPIO15
16	GND	P	Ground (0V)
17	HST_WAKE_BT / GPIO13	I	GPIO13
18	UART_WAKE / GPIO14	I	GPIO14
19	WL_DIS_N / GPIO15	I	This Pin Can Externally Shutdown the M203 (no requirement for Extra Power Switch) when BT_DIS_N is pulled low This pin can also support the WLAN Radio-off function with host interface remaining connected.
20	VD10	P	1.05V for WLAN and BT digital power
21	GND	P	Ground (0V)
22	LX_SPS	P	Switching Regulator Output
23	GND_SPS	P	Switching Regulator Ground
24	SD_WAKE / GPIO10	I	GPIO10
25	SD_D3	I/O	SDIO Data Line 3
26	SD_D2	I/O	SDIO Data Line 2
27	SD_D1	I/O	SDIO Data Line 1
28	SD_D0	I/O	SDIO Data Line 0
29	SD_CMD	I/O	SDIO Command Input
30	SD_CLK	I	SDIO Clock Input
31	VIO_HOST	P	Supply voltage for SDIO IO
32	GND	P	Ground (0V)
33	UART_CTS	I	High-Speed UART CTS
34	UART_TX	O	High-Speed UART Data Out
35	UART_RX	I	High-Speed UART Data In

36	UART_RTS	O	High-Speed UART RTS
37	GND	P	Ground (0V)
38	VDD_IO_1	P	VDD for GPIO0 to GPIO5 and GPIO11
39	BT_DIS_N / GPIO11	I	This Pin Can Externally Shutdown the M203 (no requirement for Extra Power Switch) when WL_DIS_N is pulled low. This pin can also support the BT Radio-off function with host interface remaining connected.
40	PCM_IN / GPIO0	I	PCM Input
41	PCM_OUT / GPIO1	O	PCM Out
42	PCM_SYNC / GPIO2	O	PCM Clock
43	PCM_CLK / GPIO3	I/O	PCM Synchronization control
44	GND	P	Ground (0V)
45	LED_BT	O	LED Pin (Active Low)
46	LED_WL	O	LED Pin (Active Low)
47	SUSCLK	I	Shared with EECS. External 32K or RTC clock input.
48	GND	P	Ground (0V)
EP	GND	P	Ground (0V)

7 Interface Timing Specification

	Min	Typical	Max	Unit	Description
T_{18_Ramp}	0.1	0.5	2.5	ms	The 1.8V main power ramp up duration.
T_{33_Ramp}	0.1	0.5	2.5	ms	The 3.3V main power ramp up duration.
T_{Chip_Ready}					CHIP_EN pull high timing
T_{WL_Ready}				ms	WL_DIS# pull high timing
T_{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8821CS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
$T_{G\text{-}SPI\_Ready}$	3	4	18	ms	The duration G-SPI device internal initialization. After
					$T_{G\text{-}SPI\_Ready}$, SPI host can then send command to write REG_SPI_CFG register. REG_SPI_CFG register is to control SPI endian and word length.

8 Recommend Footprint

SMD Design:
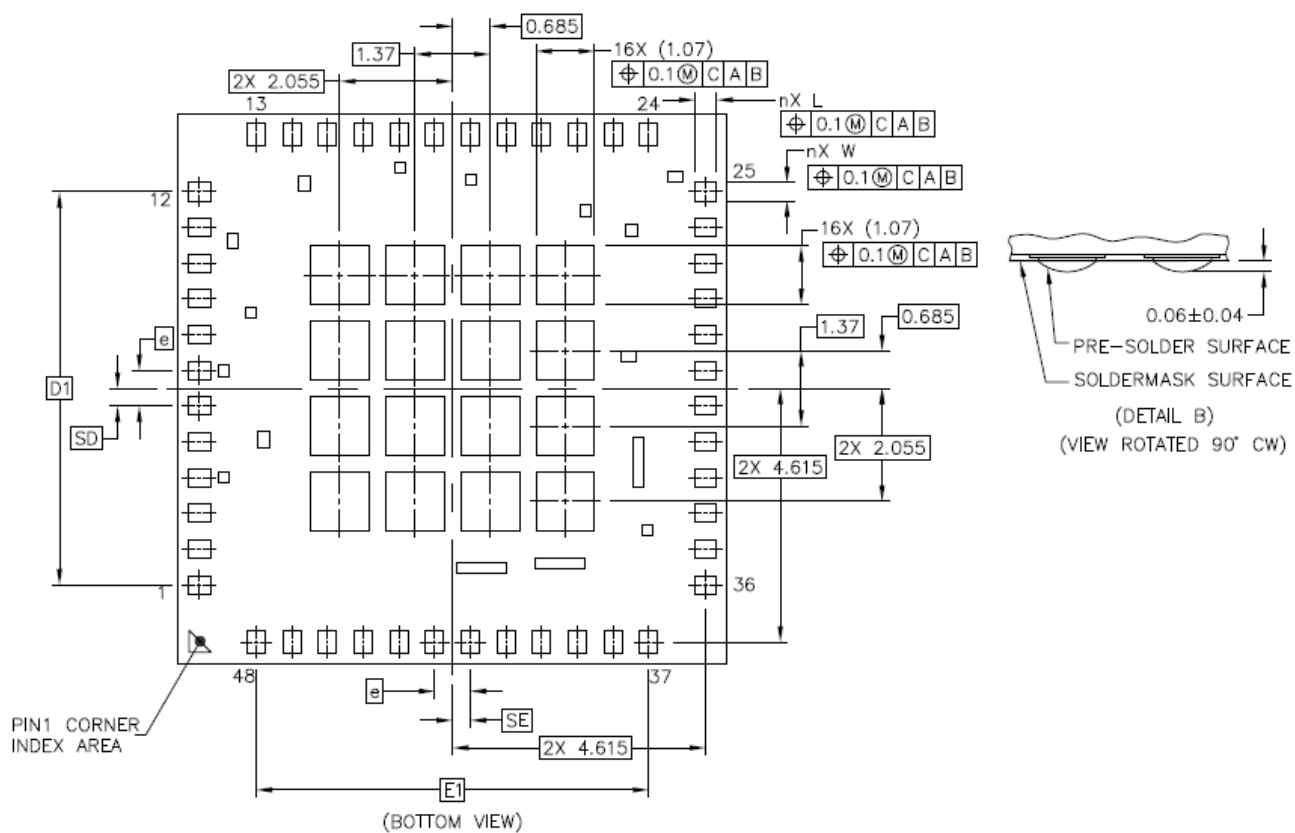
Dimension Detail

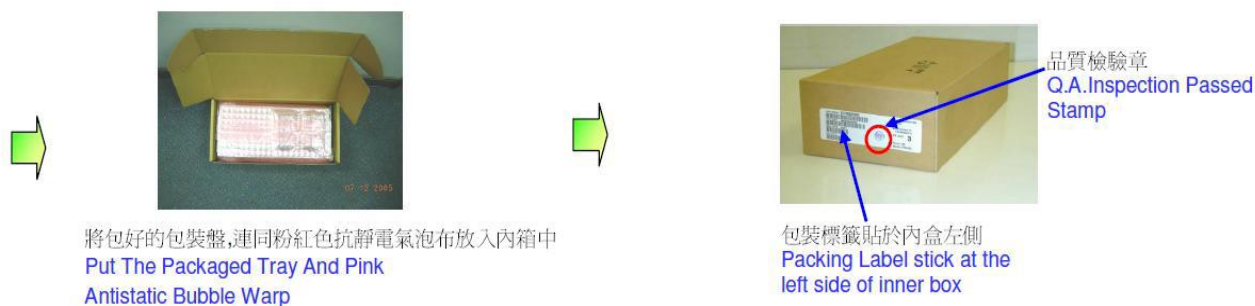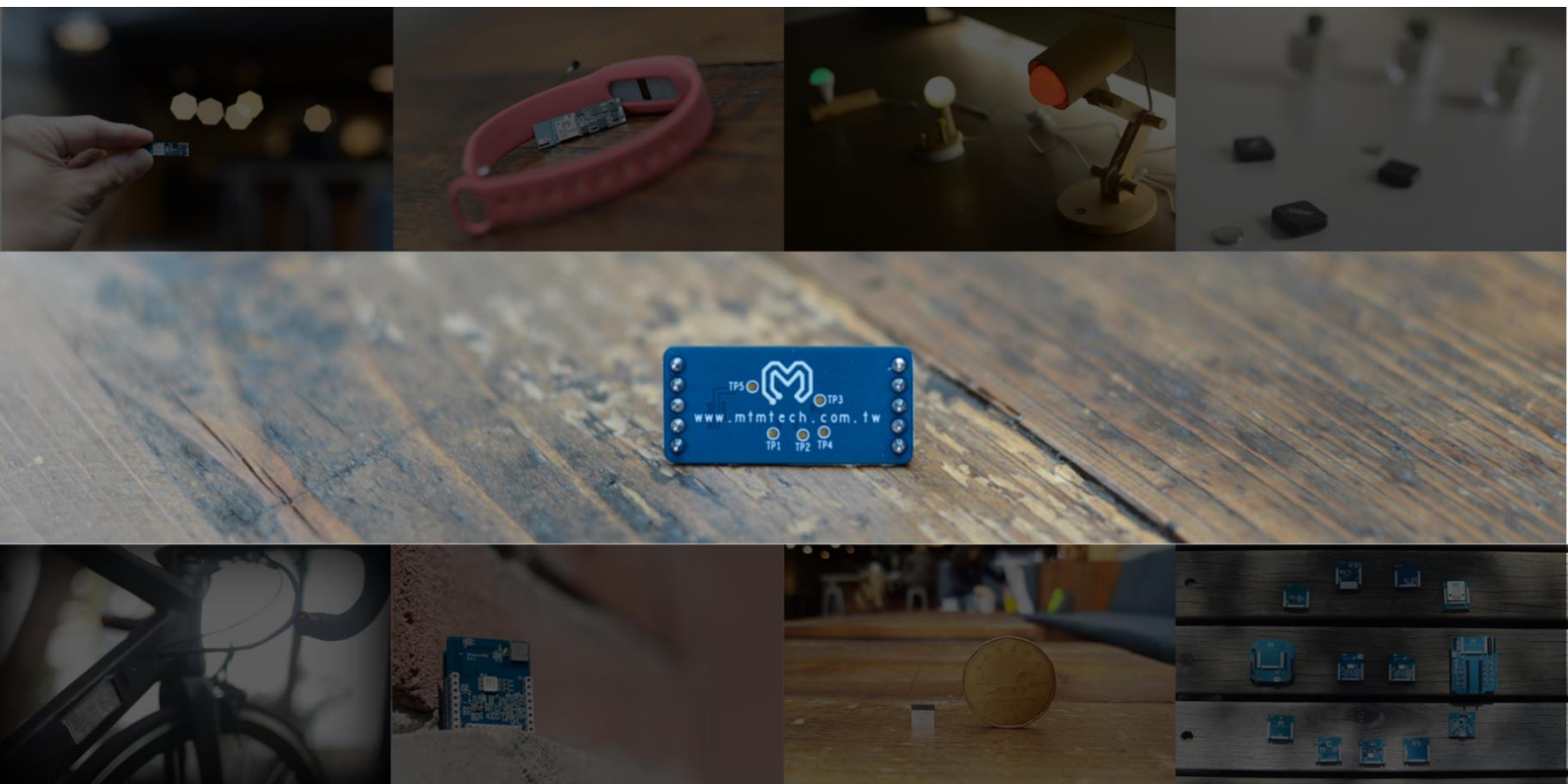|	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.3
SUBSTRATE THICKNESS	A1		0.3	REF
MOLD THICKNESS	A2		0.8	REF
BODY SIZE	D		10	BSC
	E		10	BSC
LEAD WIDTH	W	0.28	0.33	0.38
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.65	BSC
LEAD COUNT	n		48	
EDGE BALL CENTER TO CENTER	D1		7.15	BSC
	E1		7.15	BSC
BODY CENTER TO CONTACT BALL	SD		0.325	BSC
	SE		0.325	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	
PRE-SOLDER THICKNESS			0.06±0.04	

9 Recommend Reflow Profile
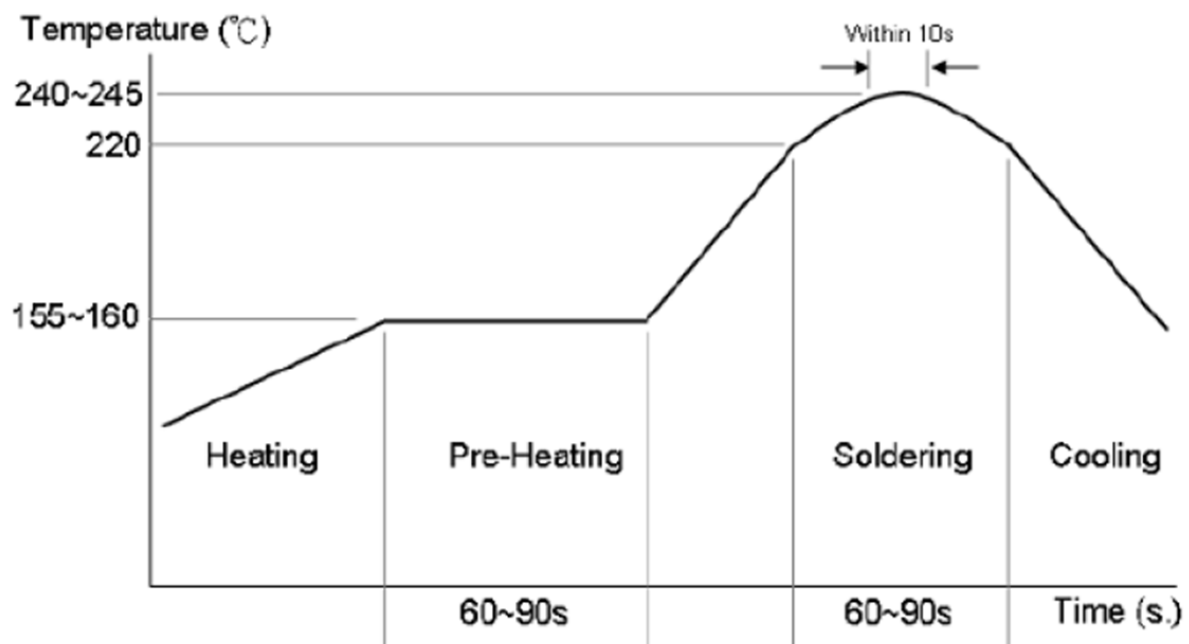
Profile Condition

a. Suitable for Lead-free solder

b. Between 155 ~ 160°C: 60 ~ 90 sec.

c. Above 220°C: 60 ~ 90 sec.

d. Peak Temperature: 240~245°C (<10 sec.)

10 Package Information

空盤 COVER TRAY
缺口 Indentation

乾燥包 Desiccant
打帶方式:三短一長 Strap Method : 3S1L
缺口 Indentation

濕度卡 Humidity Indicator Card

真空袋 Dry-pack Bag(Al-Bag)
缺口 Indentation

品質檢驗章 Q.A.Inspection Passed Stamp

一張粉紅色抗靜電氣泡布 1 piece of Pink Bubble Wrap
包裝標籤 Packing Label

For partial bundle, please place 41PACLBW001 bubble sheet on top of the product until the product can't move inside the box.
針對零絡材料，請加放41PACLBW001氣泡布於材料上方，直到材料於內盒不會晃動為止。

If the item create in barcode label, no need to fill in MSL,sealing date.
如果包裝標籤已定義則不須填上

級數 MSL
溫度(若無資料可空白) Temp (If no data, allow keeping empty)
封合日期 Sealing Date

將包好的包裝盤,連同粉紅色抗靜電氣泡布放入內箱中
Put The Packaged Tray And Pink Antistatic Bubble Warp

品質檢驗章 Q.A.Inspection Passed Stamp

包裝標籤貼於內盒左側 Packing Label stick at the left side of inner box

外箱內未滿6盒時，請以緩衝材填塞，不須另補空盒
Please place the cushion but the empty box to fill the spare space in the outer box, if the inner box q'ty is less than 6.

麥頭 ASECL Shipping Marked
品質檢驗章 Q.A.Inspection Passed Stamp
外箱 Outer Box

11 Document History

Date	Modifications	Version
Jan. 02, 2018	Preliminary Version	1.0

www.mtmtech.com.tw

MtM Technology Corporation

7F, 178 MinQuan East Road Section 3,
Songshan District, Taipei,
Taiwan (R.O.C.)

+886-2-7736-7386

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