Cadence Oscillator Simulation

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CPE 690 - Introduction to VLSI

Introduction:

The purpose of this report is to outline the design approach and simulation results in Cadence Virtuoso associated with the creation of a 5-stage CMOS oscillator. The oscillator would be composed of 5 sequential CMOS inverters, with the output of the final inverter directly wired the the input of the first inverter. The schematic would also be translated into a layout and extracted view that exhibits equivalent functionality as the corresponding schematic without violating any established design rules.

Additionally, the behavior of the oscillator would be simulated across varying temperatures and supply voltages. The simulation temperatures include -25C, 25C, and 100C. The simulation supply voltages include 2.5V, 3.0V, and 3.5V. The frequencies that correspond to each temperature and voltage level would be recorded and analyzed heuristically.

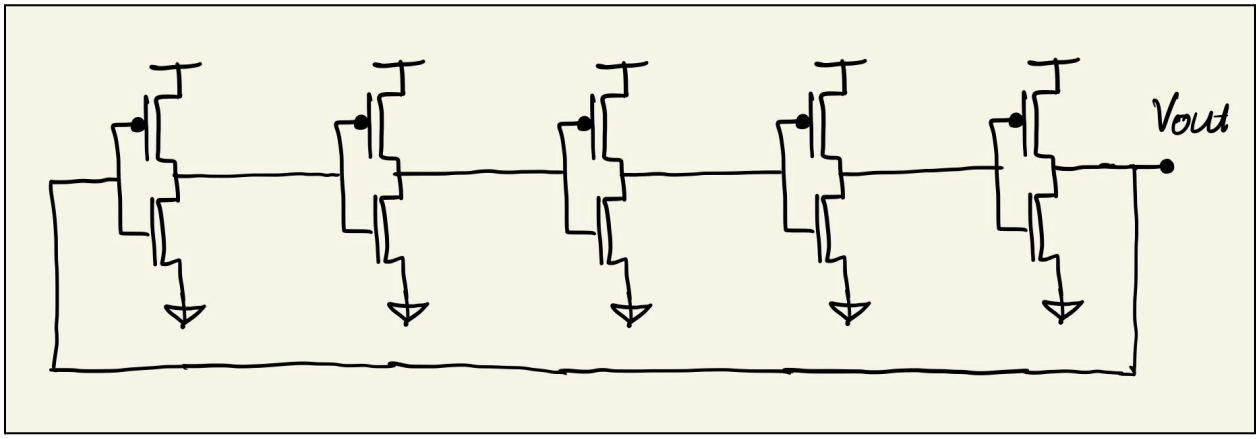

Figure 1

Design Process:

In order to eventually design the complete oscillator, a key step in the design process was to first design a modular inverter that could be instantiated for repeated use. This involved creating a cell view of a CMOS inverter with four input/output pins. This would allow for the inverter to be easily connected to any future inputs, outputs, supply voltages, and ground nodes with ease. The corresponding schematic, layout, and extracted view can be found below.

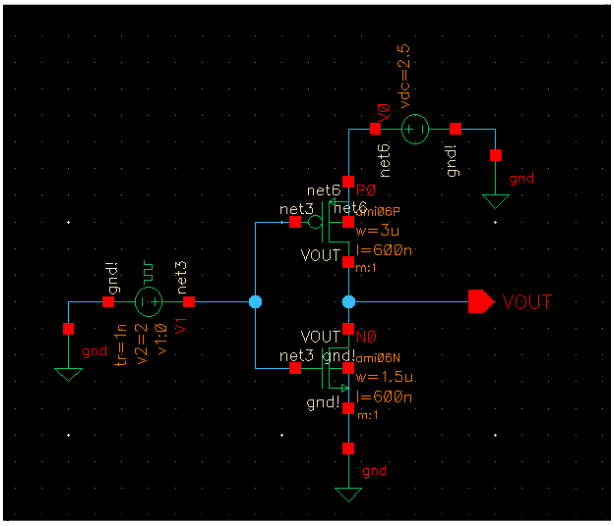

Figure 2

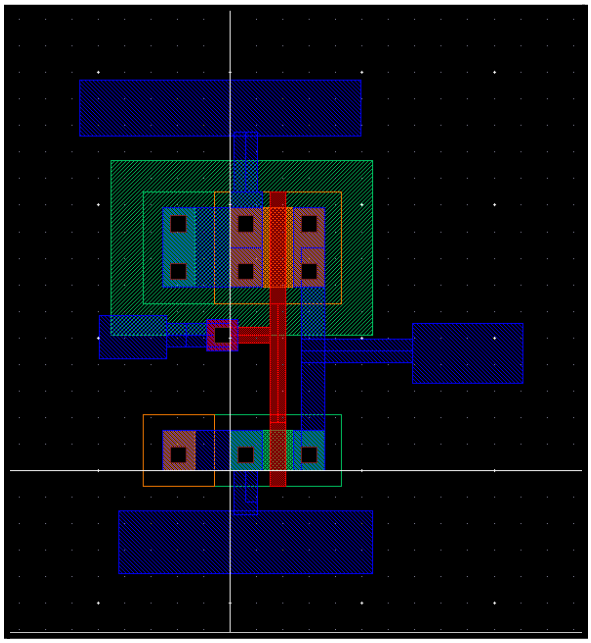

Figure 3

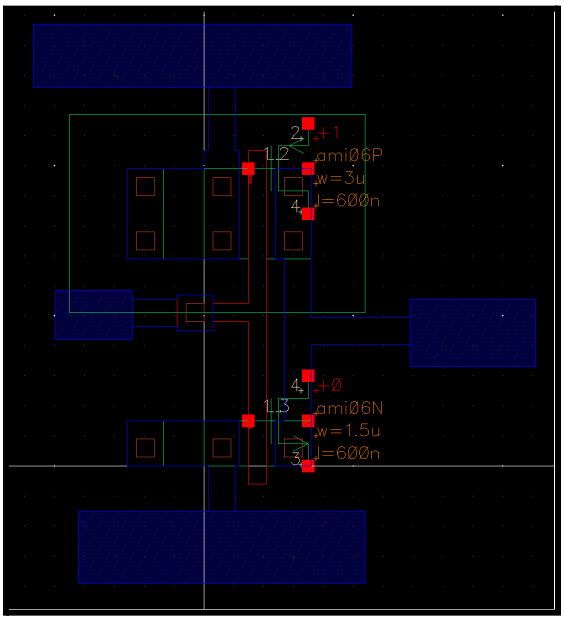

Figure 4

The inverter was tested to ensure proper functionality before moving forward. Next, five instances of the inverter were placed and connected sequentially in a separate schematic in order to replicate the behavior of an oscillator. To achieve this, inverter the output of each inverter was connected to the input of the following inverter. Additionally, the output of the fifth inverter was connected to the input of the first inverter. The schematic, layout, and extracted view can be found below:

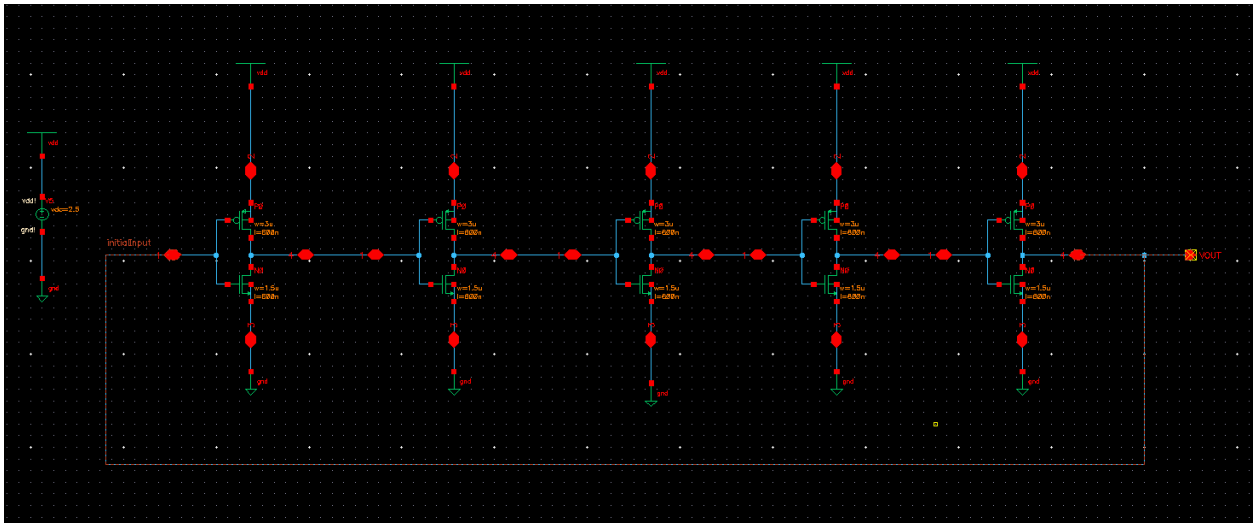

Figure 5

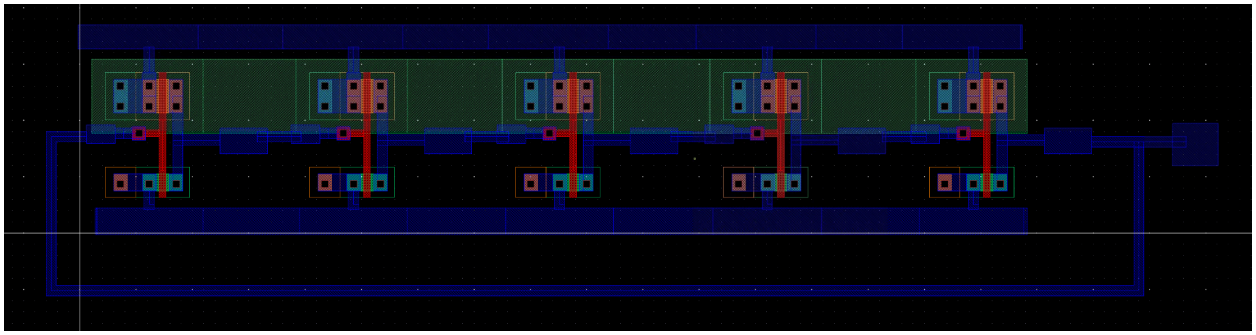

Figure 6

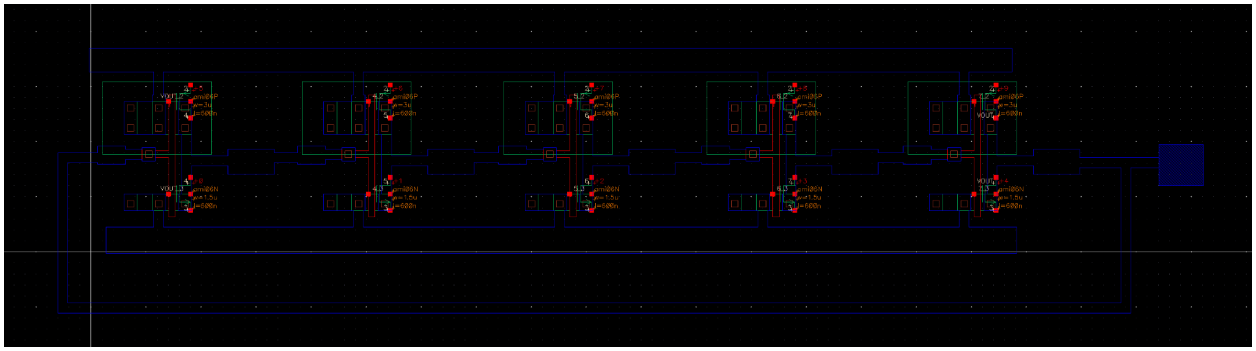

Figure 7

Results/Analysis:

Firstly, it is important to note that the final oscillator layout and extraction were verified via a design rule check (DRC) and layout versus schematic (LVS) verification. The DRC was confirmed after analysis of the layout was complete. The LVS was also successful for the extracted view of the final oscillator. The resulting DVS and LVS verification results are shown below:

```
DRC started.......Sun Nov 24 22:39:32 2024
    completed ....Sun Nov 24 22:39:32 2024
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "clock layout"   *********
   Total errors found: 0
```

Figure 8

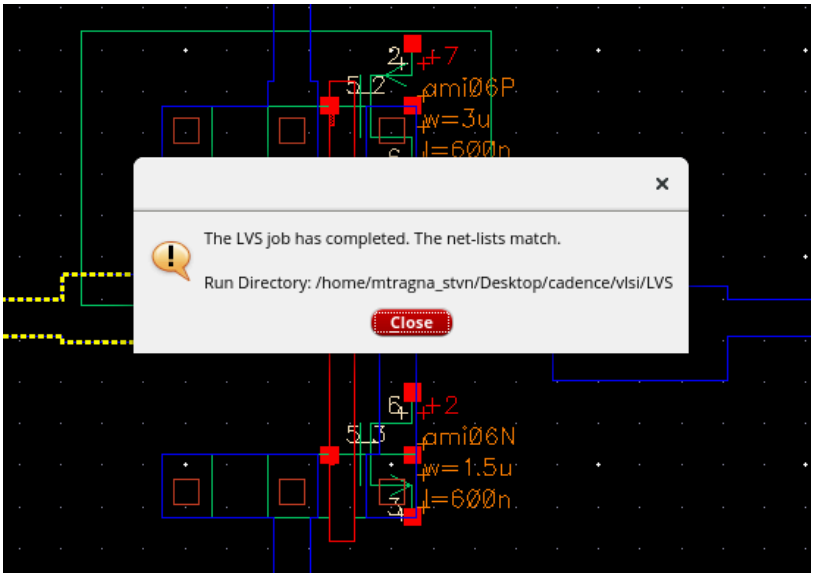

Figure 9

Next, the behavior of the oscillator was simulated using the ADE L launcher from the oscillator schematic. The output of the oscillator was simulated for 10 nanoseconds for various temperatures and supply voltage levels. The resulting data from these simulations can be found below, along with a graph of the oscillator's behavior (100C, 3.5V):

Frequencies	**2.5V**	**3.0V**	**3.5V**
-25C	550 MHz	650 MHz	825 MHz
25C	425 MHz	525 MHz	650 MHz
100C	325 MHz	425 MHz	500 MHz

Figure 10

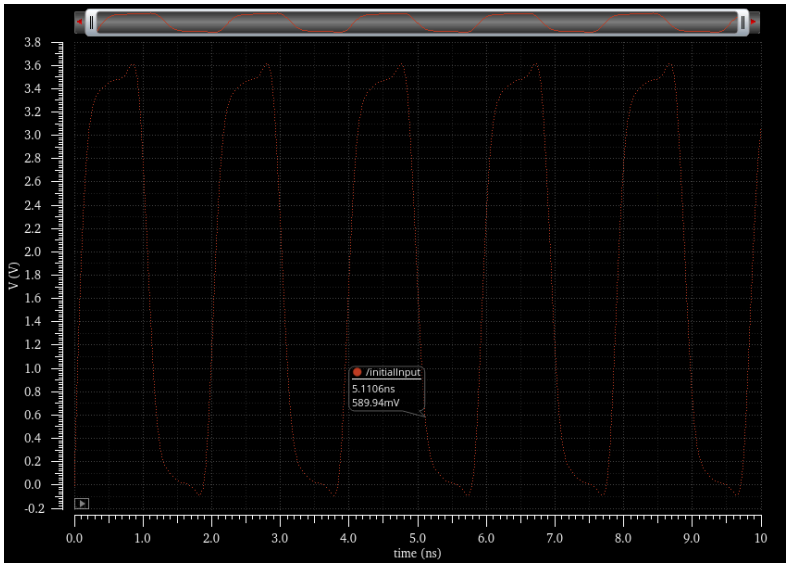

Figure 11

Difficulties:

Over the course of this project, there were many unexpected difficulties. One early difficulty was properly simulating the behavior of the oscillator. Initially, the oscillator would only display ripples around the supply voltage rather than oscillating between 0V and the supply voltage, Vdd. This was remedied by creating an initial condition of zero volts in the simulation testbench, which resulted in a corrected output waveform.

There were continuous server issues with respect to accessing Cadence via Stevens AppSpace. Unfortunately, there were many times where I was unable to access Cadence as a result of being connected to a server that did not include proper Cadence credentials and certifications. Additionally, there were multiple instances of being locked from editing files that were saved while using different servers. As a result, I often had to continuously create copies of original files, as well as sporadically try to access Cadence in hopes of being able to access a functional server.