PROJECT 2 SEQUENTIAL CIRCUITS

PROBLEM DEFINITION

It is requested to design and implement a synchronous sequential circuit which detects two different
4-bit sequences A and B. The constraints are given below.

1. **A** is the 4-bit binary code of your **school number's digit before the last one**.
2. **B** is the 4-bit binary code of your **school number's last digit**. (If **A=B** choose a different digit)
3. The circuit will have 1-bit data input **X**, 1-bit data output **Y**, 1-bit **CLK** (clock) input and 1-bit **RST** (reset) input.
4. **A and B may overlap**. Your circuit will detect both which means your circuit will not ignore detecting another sequences while detecting any sequence. A overlapping A, A overlapping B, B overlapping B and B overlapping A are valid situations.
5. **When an A or a B word is detected**, your circuit **sets its Y** output. Otherwise the output remains at reset.
6. Your circuit will go to a lock state, which is determined by yourself, and get stuck on there **when two A or two B words (same words) are detected**. Only a **reset** signal will move your circuit to the initial or idle state.
7. At the beginning, you should draw your **state diagram** and report it. Your work on **state reduction** and **state coding** should be included by your report.
8. You should report your design details and also you should gather information from ISE reports. Your project report should include **timing and area performances**.
9. You should **write your own test code** and verify your circuit with this code. The test code should have an input pattern with **all possible** overlapping and discrete A and B word positions on the input bit stream.
10. At the end, you should determine your circuit's score after the placement and routing.
    Score = 1/(The number of LUTs * the number of D-flipflops * minimum applicable period to your circuit). Please note your score to the report
11. Your report (max. 3 pages) should include your analysis about the **circuit type** (Mealy/Moore), the complete analysis about the existence of **hazards** (zararlı hatalı çıkışlar).

Good luck.