EXPERIMENT I: SSI COMPONENTS

AND GATE

```
=========================================================================
*                          Low Level Synthesis                          *
=========================================================================

Optimizing unit <Top_Module> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Top_Module, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================
```

Figure 1 Low level synthesis of AND gate

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : Top_Module.ngr
Top Level Output File Name         : Top_Module
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 3

Cell Usage :
# BELS                             : 1
#      LUT2                        : 1
# IO Buffers                       : 3
#      IBUF                        : 2
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s500efg320-4

 Number of Slices:                        1  out of   4656     0%
 Number of 4 input LUTs:                  1  out of   9312     0%
 Number of IOs:                           3
 Number of bonded IOBs:                   3  out of    232     1%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
```

Figure 2 Low level synthesis of AND gate

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 6.209ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 2 / 1
-------------------------------------------------------------------------
Delay:               6.209ns (Levels of Logic = 3)
  Source:            A (PAD)
  Destination:       C (PAD)

  Data Path: A to C
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.218   0.595  A_IBUF (A_IBUF)
     LUT2:I0->O            1   0.704   0.420  GATE/O1 (C_OBUF)
     OBUF:I->O                 3.272          C_OBUF (C)
    ----------------------------------------
    Total                      6.209ns (5.194ns logic, 1.015ns route)
                                       (83.7% logic, 16.3% route)

=========================================================================
```

Figure 3 Timing details of AND gate

As seen in the report, from input 1 to output is 6.209 ns. With 1 fanout from input to gate (the time on wire) 1.813 ns. From gate to output wire is 1.124 ns.

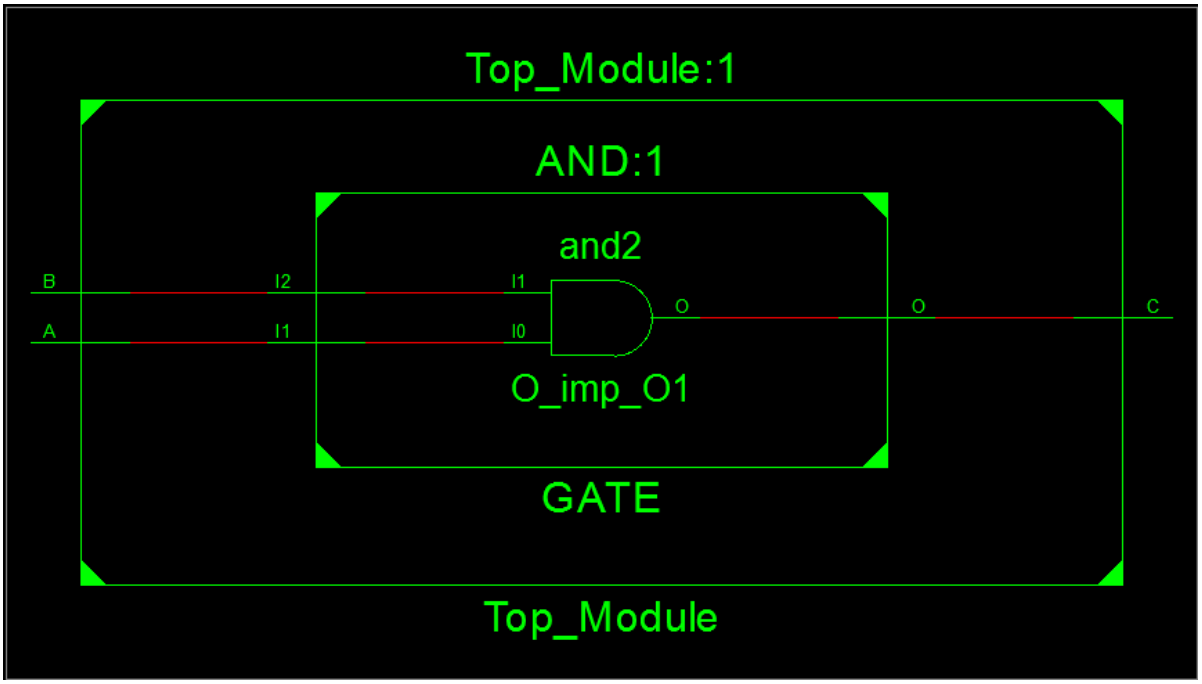

Figure 4 RTL schematics of AND gate

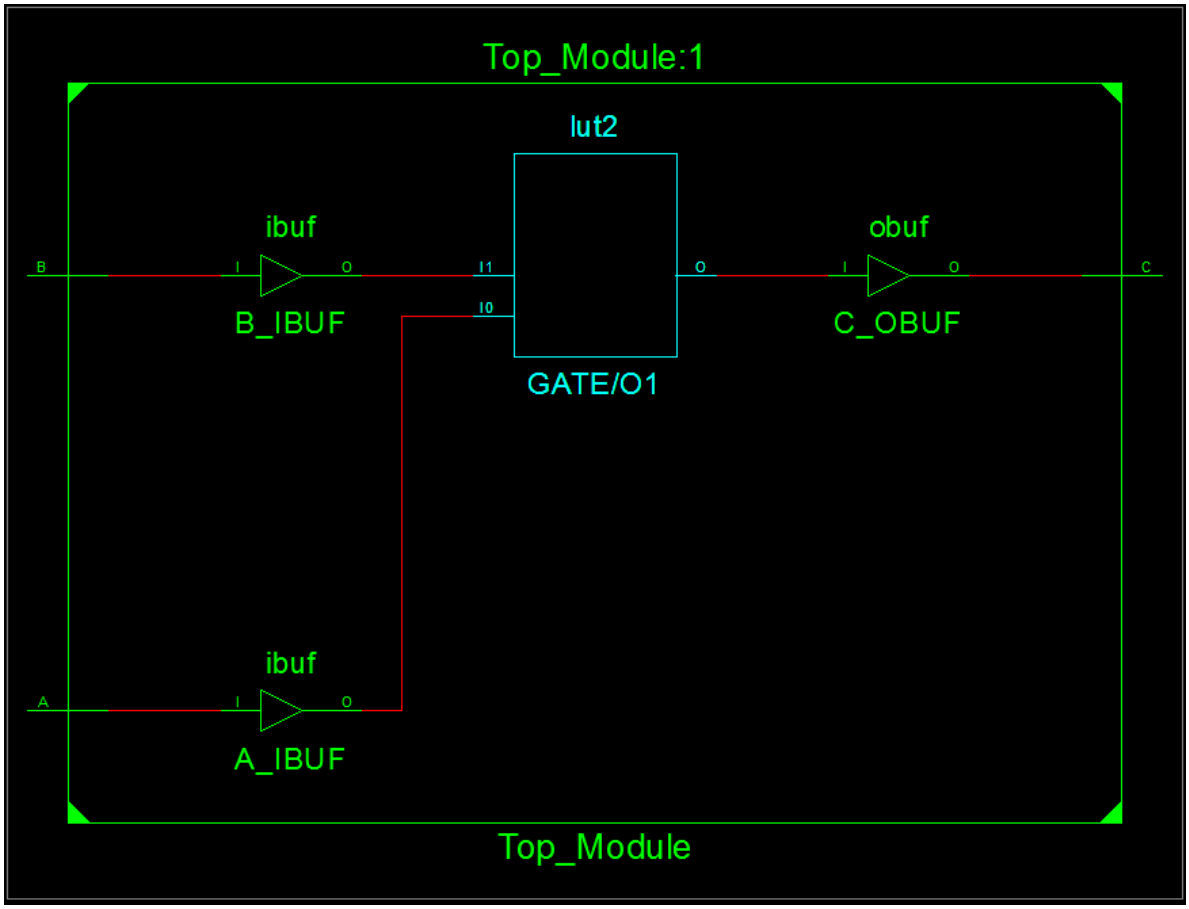

Figure 5 Technology schematics of AND gate

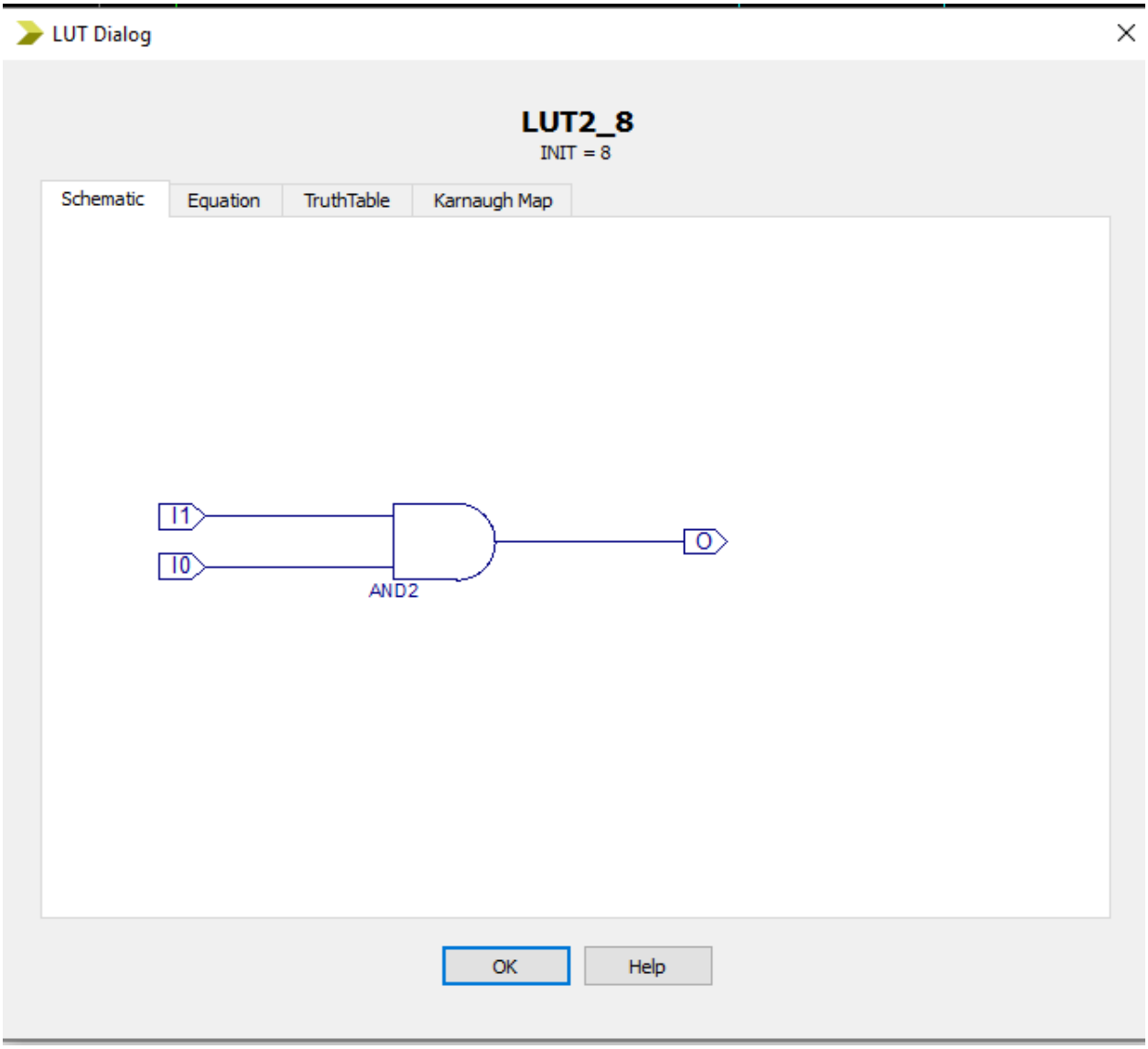

Figure 6 Inside of LUT in Technology schematics of AND gate

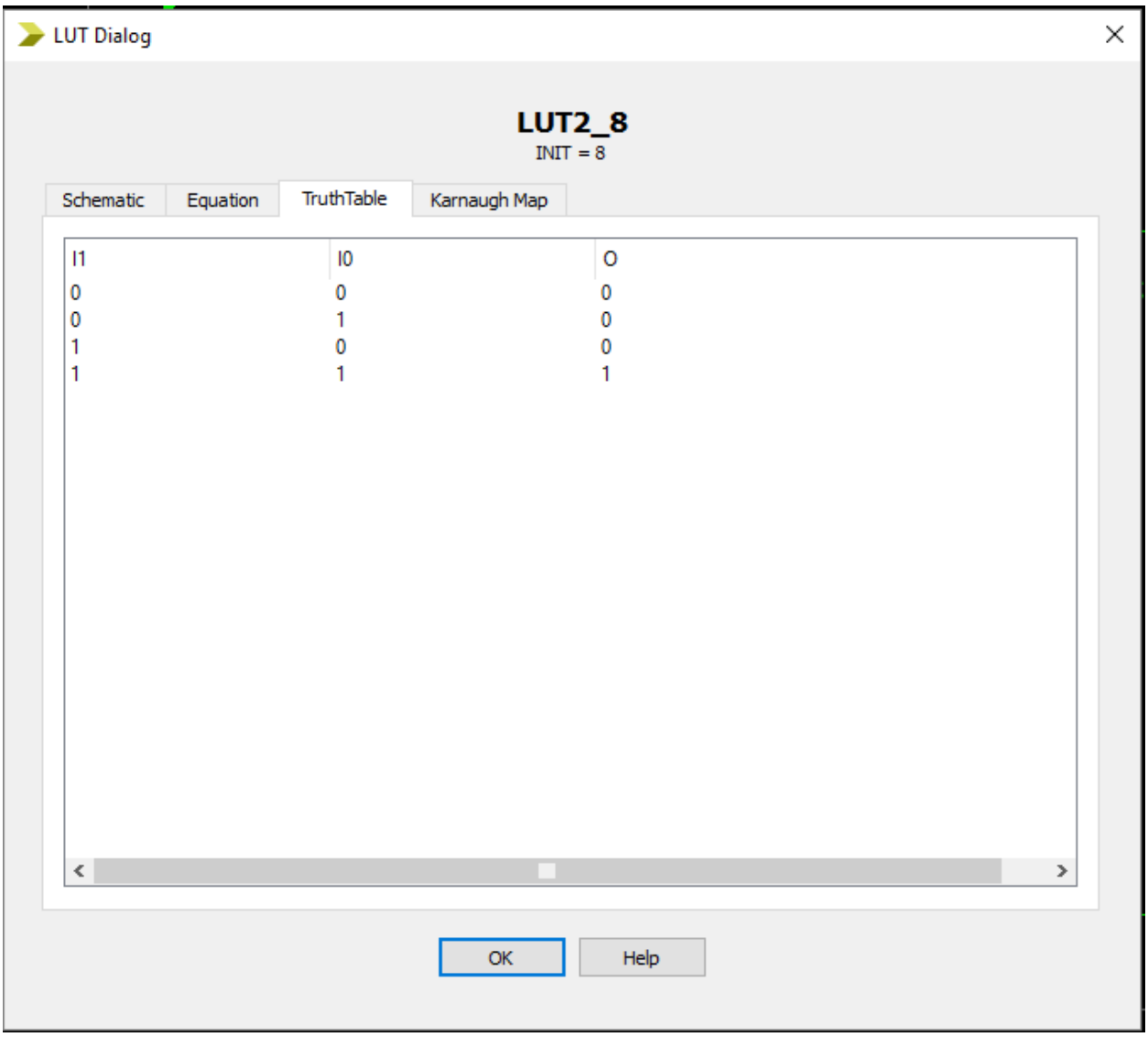

Figure 7 Truth Table of LUT in Technology schematics of AND gate

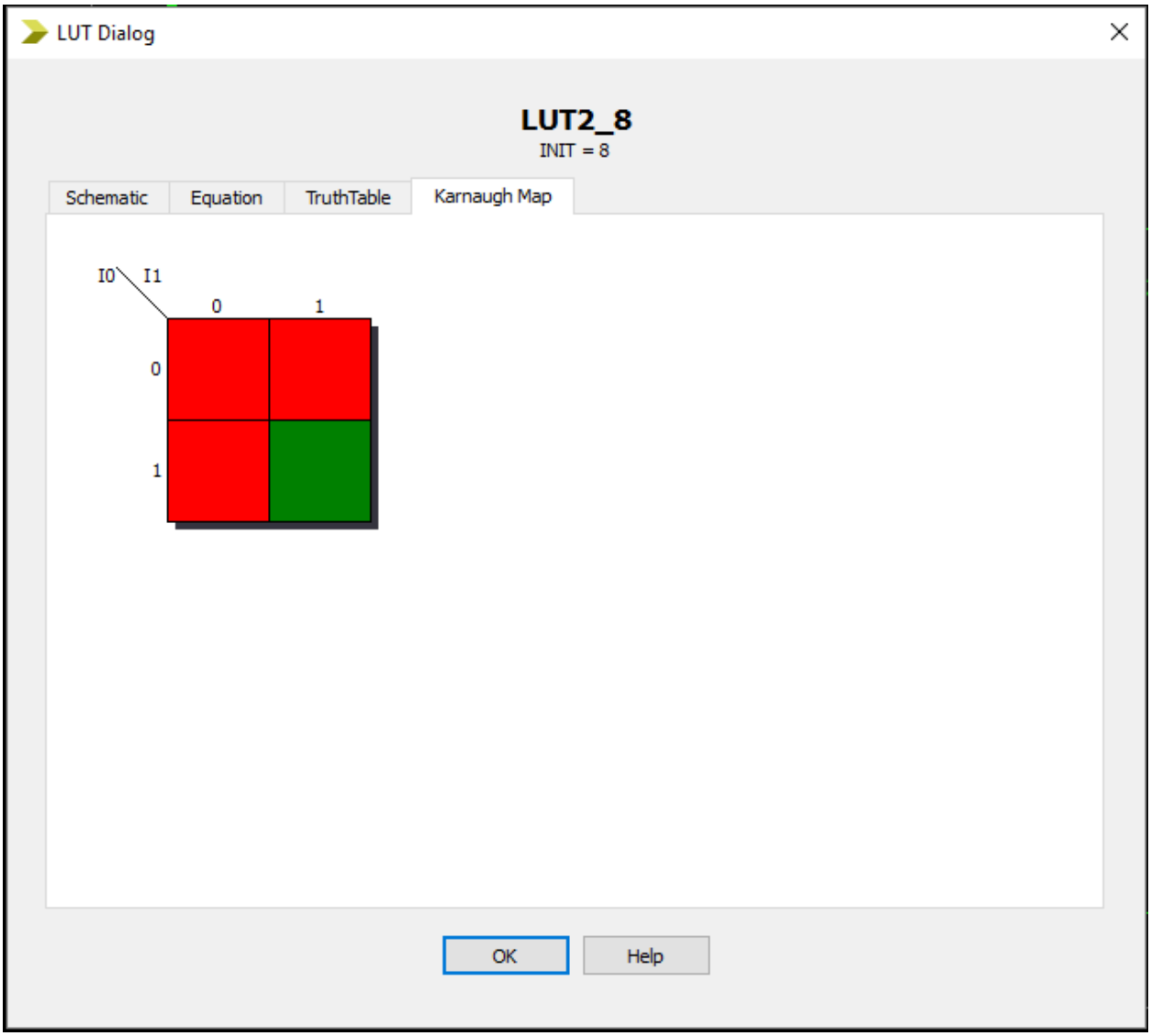

Figure 8 Karnaugh Map of LUT in Technology schematics of AND gate

Original Code:

```
module AND (input I1,I2, output O);
assign O = ( I1 & I2 );
endmodule
```

Code after Post-Synthesis Simulation Model:

```
`timescale 1 ns/1 ps

module Top_Module (
  A, B, C
);
  input A;
  input B;
  output C;
  wire A_IBUF_1;
  wire B_IBUF_3;
  wire C_OBUF_5;
  LUT2 #(
    .INIT ( 4'h8 ))
  \GATE/O1  (
    .I0(A_IBUF_1),
    .I1(B_IBUF_3),
    .O(C_OBUF_5)
  );
  IBUF   A_IBUF (
    .I(A),
    .O(A_IBUF_1)
  );
  IBUF   B_IBUF (
    .I(B),
    .O(B_IBUF_3)
  );
  OBUF   C_OBUF (
    .I(C_OBUF_5),
    .O(C)
  );
endmodule
```

LUT Primitives are the functions that tell FPGA how the LUTS will work. Normally initial value of LUT primitive is 0, because it works as ground. However, in our design it is 8, because we used AND gate, as seen above. For our inputs the program used buffers on the wires.

Code After Post-Translate Simulation Model:

```
`timescale 1 ns/1 ps

module Top_Module (
  A, B, C
);
  input A;
  input B;
  output C;
  wire A_IBUF_1;
  wire B_IBUF_3;
  wire C_OBUF_5;
  X_LUT2 #(
    .INIT ( 4'h8 ))
  \GATE/O1  (
    .ADR0(A_IBUF_1),
    .ADR1(B_IBUF_3),
    .O(C_OBUF_5)
  );
  X_BUF   A_IBUF (
    .I(A),
    .O(A_IBUF_1)
  );
  X_BUF   B_IBUF (
    .I(B),
    .O(B_IBUF_3)
  );
  X_IPAD   A_5 (
    .PAD(A)
  );
  X_IPAD   B_6 (
    .PAD(B)
  );
  X_OPAD   C_7 (
    .PAD(C)
  );
  X_OBUF   C_OBUF (
    .I(C_OBUF_5),
    .O(C)
  );
endmodule
```

With translation, the code is more likely to understood by FPGA. Now instead of just showing the places of wires, and where their output is going in AND gate.

```
Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of 4 input LUTs:                  1 out of   9,312    1%
Logic Distribution:
  Number of occupied Slices:               1 out of   4,656    1%
    Number of Slices containing only related logic:       1 out of       1 100%
    Number of Slices containing unrelated logic:          0 out of       1   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:            1 out of   9,312    1%
  Number of bonded IOBs:                   3 out of     232    1%

Average Fanout of Non-Clock Nets:                1.00

Peak Memory Usage:  297 MB
Total REAL time to MAP completion:  1 secs
Total CPU time to MAP completion:   1 secs
```

Figure 9 Map Report of AND gate

```
Section 5 - Removed Logic
-------------------------

Section 6 - IOB Properties
--------------------------

+------------------------------------------------------------------------------------------------------------------------+
| IOB Name                         | Type            | Direction | IO Standard          | Diff  | Drive    | Slew | Reg (s)      | Resistor | IOB      |
|                                  |                 |           |                      | Term  | Strength | Rate |              |          | Delay    |
+------------------------------------------------------------------------------------------------------------------------+
| A                                | IBUF            | INPUT     | LVCMOS25             |       |          |      |              |          | 0 / 0    |
| B                                | IBUF            | INPUT     | LVCMOS25             |       |          |      |              |          | 0 / 0    |
| C                                | IOB             | OUTPUT    | LVCMOS25             |       | 12       | SLOW |              |          | 0 / 0    |
+------------------------------------------------------------------------------------------------------------------------+
```

Figure 10 IOB properties of AND gate

```
Data Sheet report:
------------------
All values displayed in nanoseconds (ns)

Pad to Pad
---------------+---------------+---------+
Source Pad     |Destination Pad|  Delay  |
---------------+---------------+---------+
A              |C              |    5.452|
B              |C              |    5.452|
---------------+---------------+---------+
```

Figure 11 Delays from source to destination pad of AND gate

Code after Post-Map Simulation Model:

```
`timescale 1 ns/1 ps

module Top_Module (
  A, B, C
);
  input A;
  input B;
  output C;
  wire A_IBUF_12;
  wire B_IBUF_13;
  wire \C/O ;
  wire \B/INBUF ;
  wire \A/INBUF ;
  wire C_OBUF_44;
  wire VCC;
  initial $sdf_annotate("netgen/map/top_module_map.sdf");
  X_OPAD   \C/PAD  (
    .PAD(C)
  );
  X_OBUF   C_OBUF (
    .I(\C/O ),
    .O(C)
  );
  X_IPAD   \B/PAD  (
    .PAD(B)
  );
  X_BUF   B_IBUF (
    .I(B),
    .O(\B/INBUF )
  );
  X_IPAD   \A/PAD  (
    .PAD(A)
  );
  X_BUF   A_IBUF (
    .I(A),
    .O(\A/INBUF )
  );
  X_BUF   \B/IFF/IMUX  (
    .I(\B/INBUF ),
    .O(B_IBUF_13)
  );
  X_LUT4 #(
    .INIT ( 16'h8888 ))
  \GATE/O1  (
```

```
    .ADR0(A_IBUF_12),
    .ADR1(B_IBUF_13),
    .ADR2(VCC),
    .ADR3(VCC),
    .O(C_OBUF_44)
  );
  X_BUF   \A/IFF/IMUX  (
    .I(\A/INBUF ),
    .O(A_IBUF_12)
  );
  X_BUF   \C/OUTPUT/OFF/OMUX  (
    .I(C_OBUF_44),
    .O(\C/O )
  );
  X_ONE   NlwBlock_Top_Module_VCC (
    .O(VCC)
  );
endmodule
```

Inputs of LUTs:
    Post-Translate Simulation Model: 2
    Post-Map Simulation Model: 4
Input signals of LUTs:
    Post-Translate Simulation Model: 2
    Post-Map Simulation Model: 2
Initial value of LUTs:
    Post-Translate Simulation Model: h8
    Post-Map Simulation Model: h8888

```
Design Summary Report:

 Number of External IOBs                           3 out of 232     1%

   Number of External Input IOBs                   2

      Number of External Input IBUFs               2

   Number of External Output IOBs                  1

      Number of External Output IOBs               1

   Number of External Bidir IOBs                   0


   Number of Slices                          1 out of 4656    1%
      Number of SLICEMs                      0 out of 2328    0%
```

Figure 12 Place and Route Report of AND gate

```
Data Sheet report:
------------------
All values displayed in nanoseconds (ns)

Pad to Pad
---------------+---------------+---------+
Source Pad     |Destination Pad|  Delay  |
---------------+---------------+---------+
A              |C              |    5.914|
B              |C              |    6.052|
---------------+---------------+---------+
```

Figure 13 Post-PAR Static Timing Report of AND gate

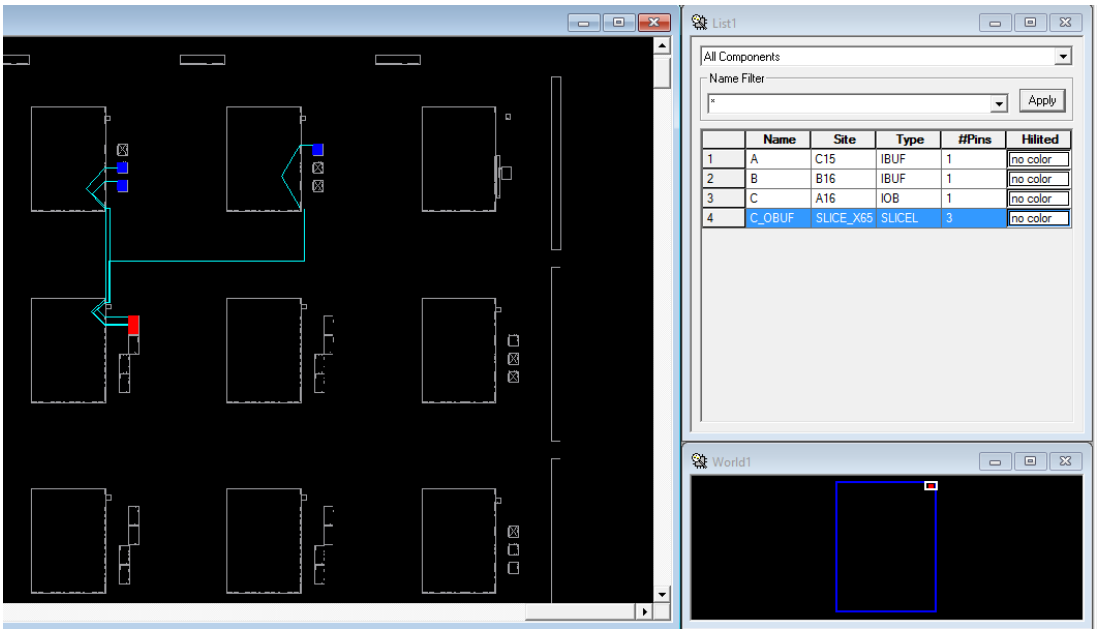

Figure 14 SLICE of AND gate in FPGA editor

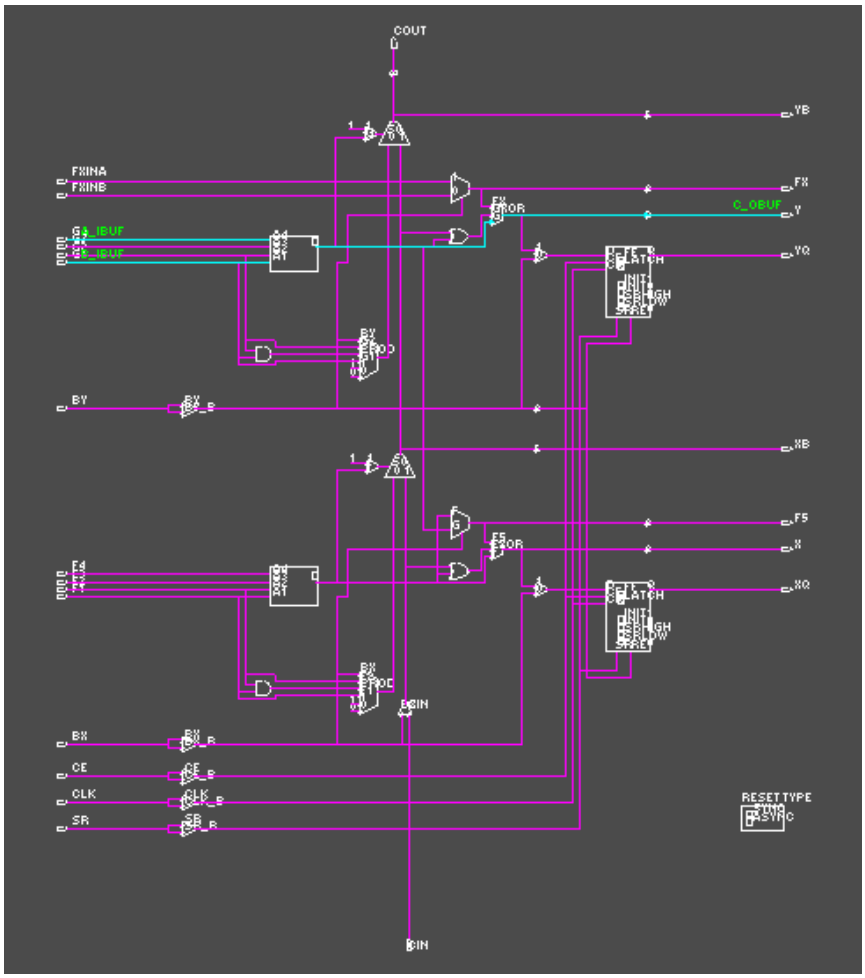

Figure 15 Internal view of output SLICE of AND gate in FPGA editor

Figure 13 Logical Function of AND gate in FPGA editor

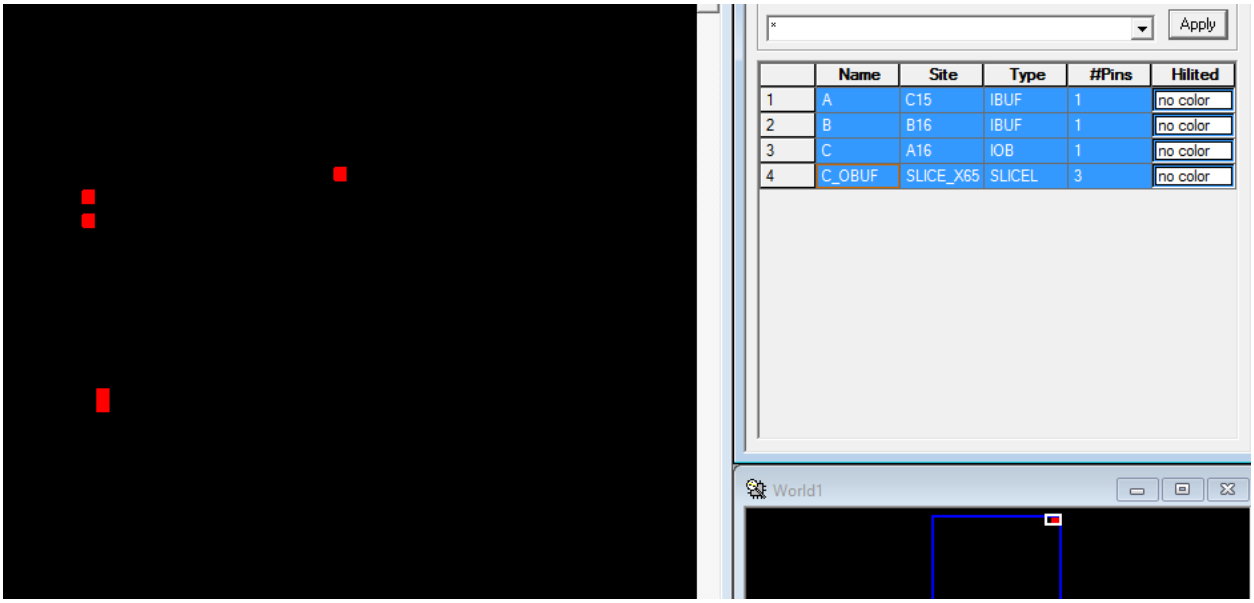

Figure 16 RPM grids of input and output of AND gate in FPGA editor

Code after Post-Place and Route Simulation:

```
`timescale 1 ns/1 ps

module Top_Module (
  A, B, C
);
  input A;
  input B;
  output C;
  wire A_IBUF_12;
  wire B_IBUF_13;
  wire \C/O ;
  wire \B/INBUF ;
  wire \A/INBUF ;
```

```
wire C_OBUF_44;
wire VCC;
initial $sdf_annotate("netgen/par/top_module_timesim.sdf");
X_OPAD #(
  .LOC ( "PAD56" ))
\C/PAD  (
  .PAD(C)
);
X_OBUF #(
  .LOC ( "PAD56" ))
C_OBUF (
  .I(\C/O ),
  .O(C)
);
X_IPAD #(
  .LOC ( "PAD57" ))
\B/PAD  (
  .PAD(B)
);
X_BUF #(
  .LOC ( "PAD57" ))
B_IBUF (
  .I(B),
  .O(\B/INBUF )
);
X_IPAD #(
  .LOC ( "IPAD58" ))
\A/PAD  (
  .PAD(A)
);
X_BUF #(
  .LOC ( "IPAD58" ))
A_IBUF (
  .I(A),
  .O(\A/INBUF )
);
X_BUF #(
  .LOC ( "PAD57" ))
\B/IFF/IMUX  (
  .I(\B/INBUF ),
  .O(B_IBUF_13)
);
X_BUF #(
  .LOC ( "IPAD58" ))
\A/IFF/IMUX  (
  .I(\A/INBUF ),
```

```
    .O(A_IBUF_12)
  );
  X_LUT4 #(
    .INIT ( 16'hAA00 ),
    .LOC ( "SLICE_X65Y91" ))
  \GATE/O1  (
    .ADR0(B_IBUF_13),
    .ADR1(VCC),
    .ADR2(VCC),
    .ADR3(A_IBUF_12),
    .O(C_OBUF_44)
  );
  X_BUF #(
    .LOC ( "PAD56" ))
  \C/OUTPUT/OFF/OMUX  (
    .I(C_OBUF_44),
    .O(\C/O )
  );
  X_ONE   NlwBlock_Top_Module_VCC (
    .O(VCC)
  );
endmodule
```

Input Signals of LUT: 2
Initial values of LUT: hAA00
Loc information of Primitives: SLICE_X65Y91

OR GATE

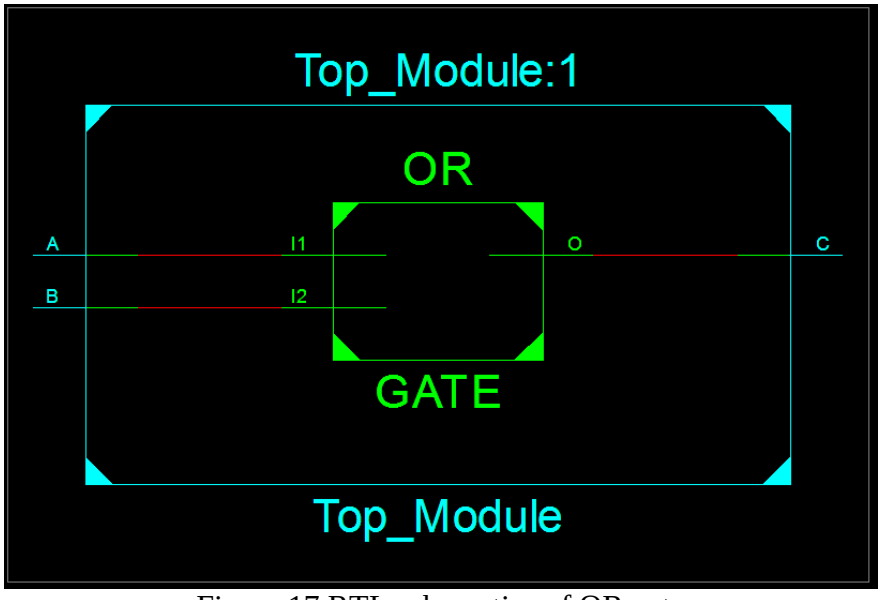

Figure 17 RTL schematics of OR gate

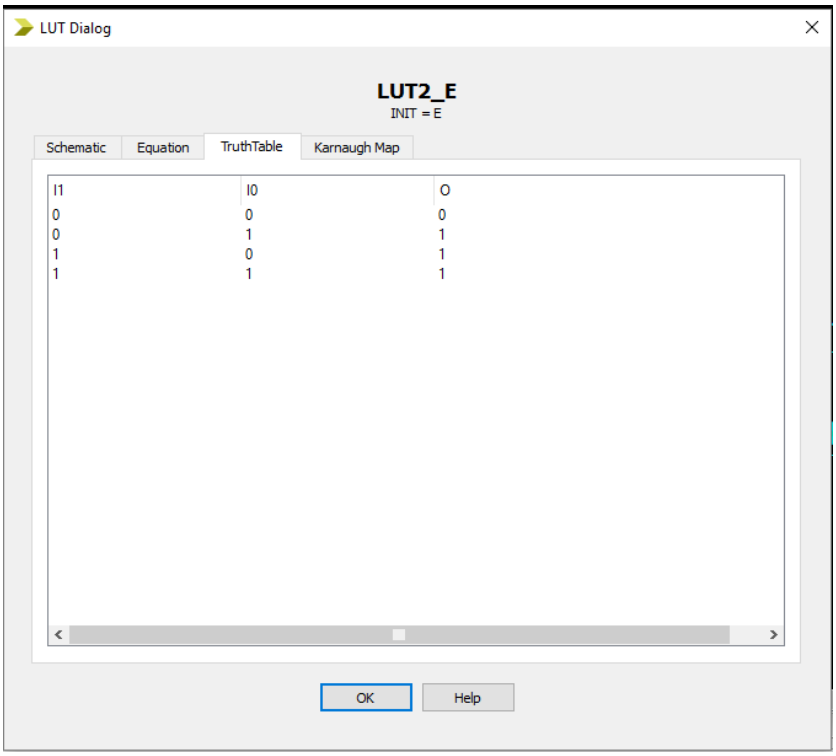

Figure 18 Truth table of LUT in Technology schematics of OR gate

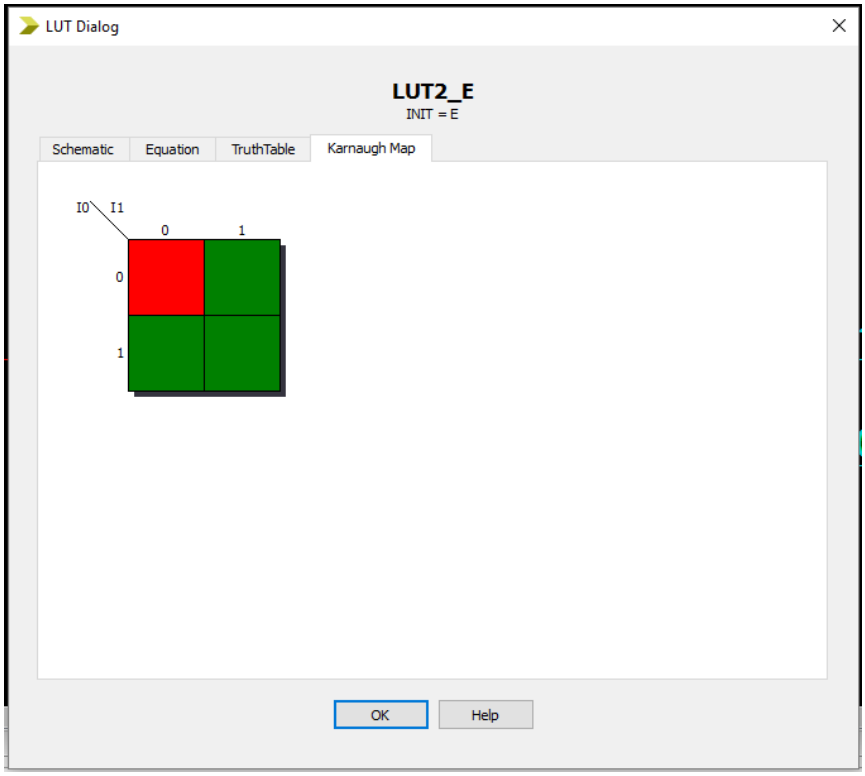

Figure 19 Karnaugh Map of LUT in Technology schematics of OR gate

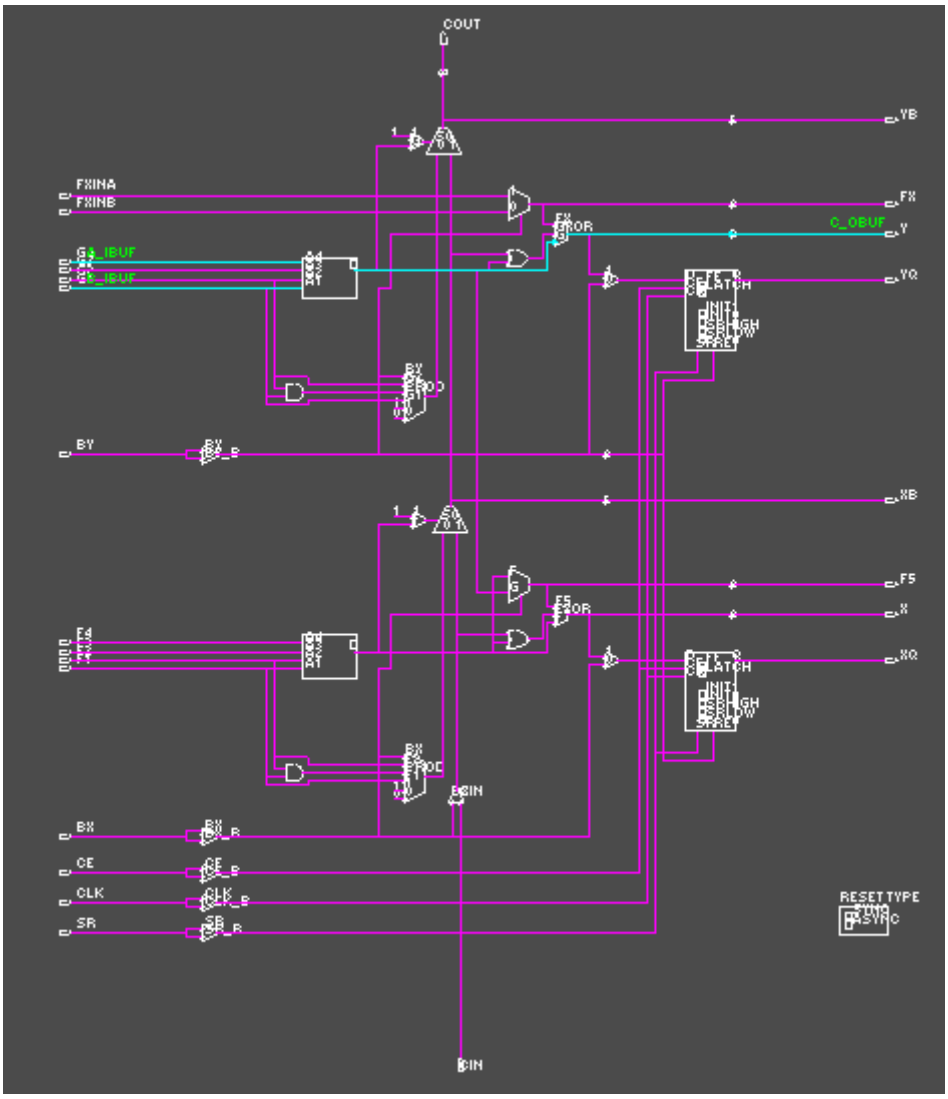

Figure 20 Design of OR gate in FPGA editor

NOT GATE

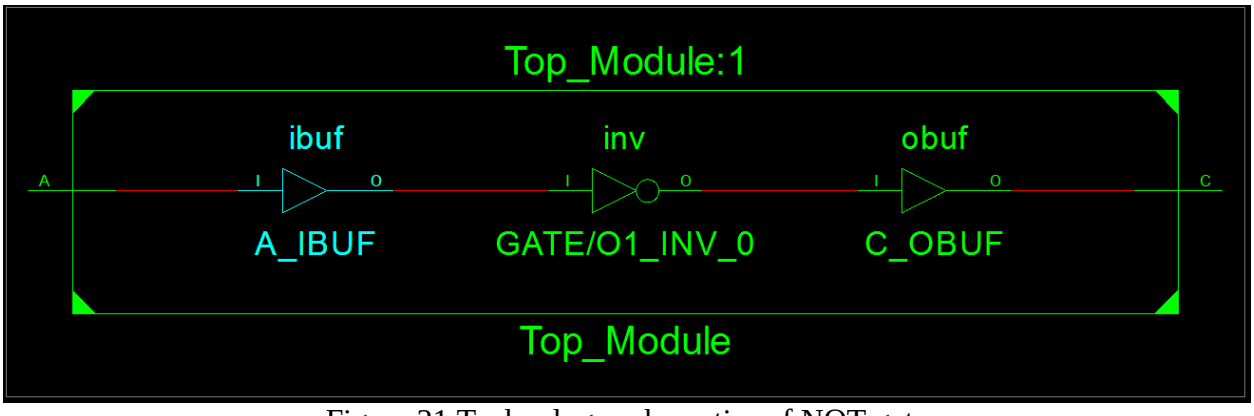

Figure 21 Technology schematics of NOT gate

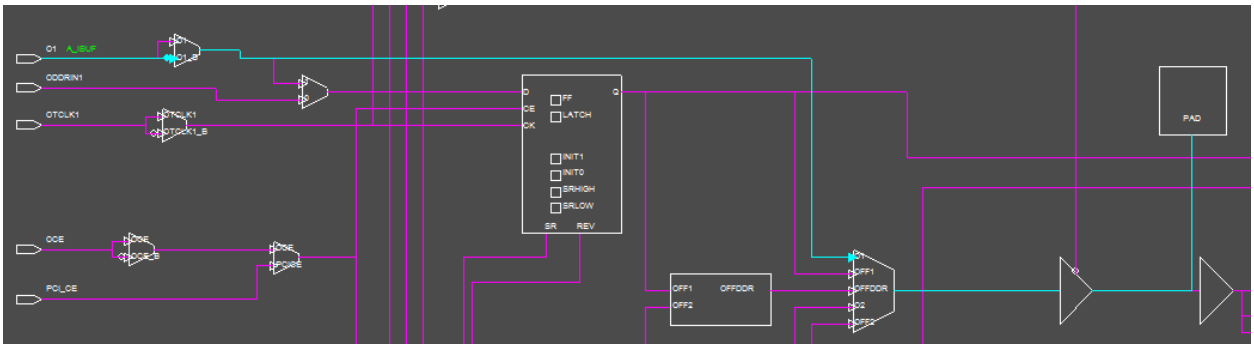

Figure 22 Design of NOT gate in FPGA editor

NAND GATE

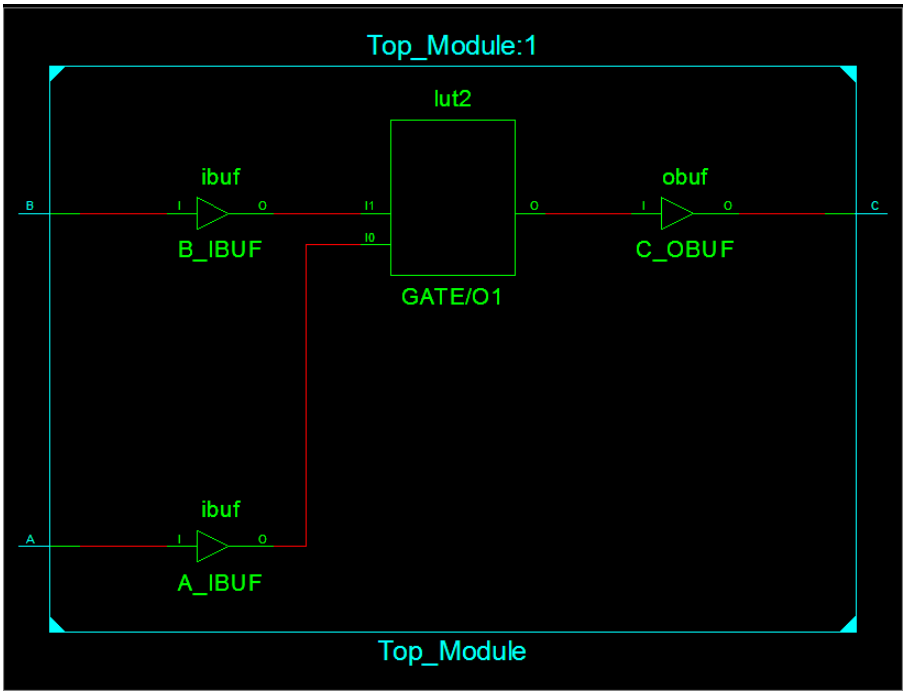

Figure 23 Technology schematics of NAND gate

I1	I0	O
0	0	1
0	1	1
1	0	1
1	1	0

Figure 24 Truth Table of NAND gate

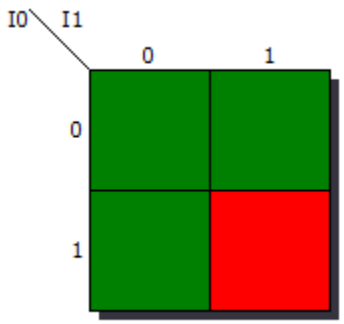

Figure 25 Karnaugh Map of NOT gate

RING OSCILLATOR

Without KEEP function program is reduced to 2 LUTs, which is minimum for this design. It made 1 TRI gate and 1 NOT gate. With KEEP function we use 200 LUTs, which are used for 1 TRI gate and 199 NOT gate for design we wanted.

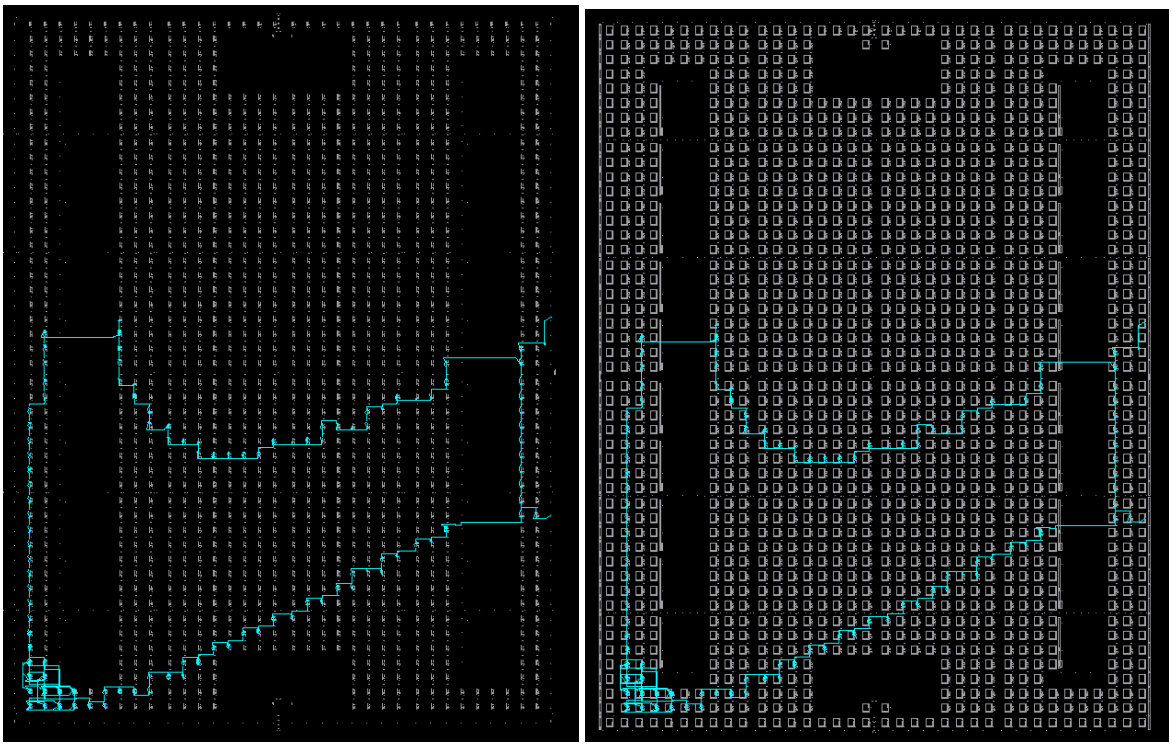

Figure 26 Design of ring oscillator in FPGA editor

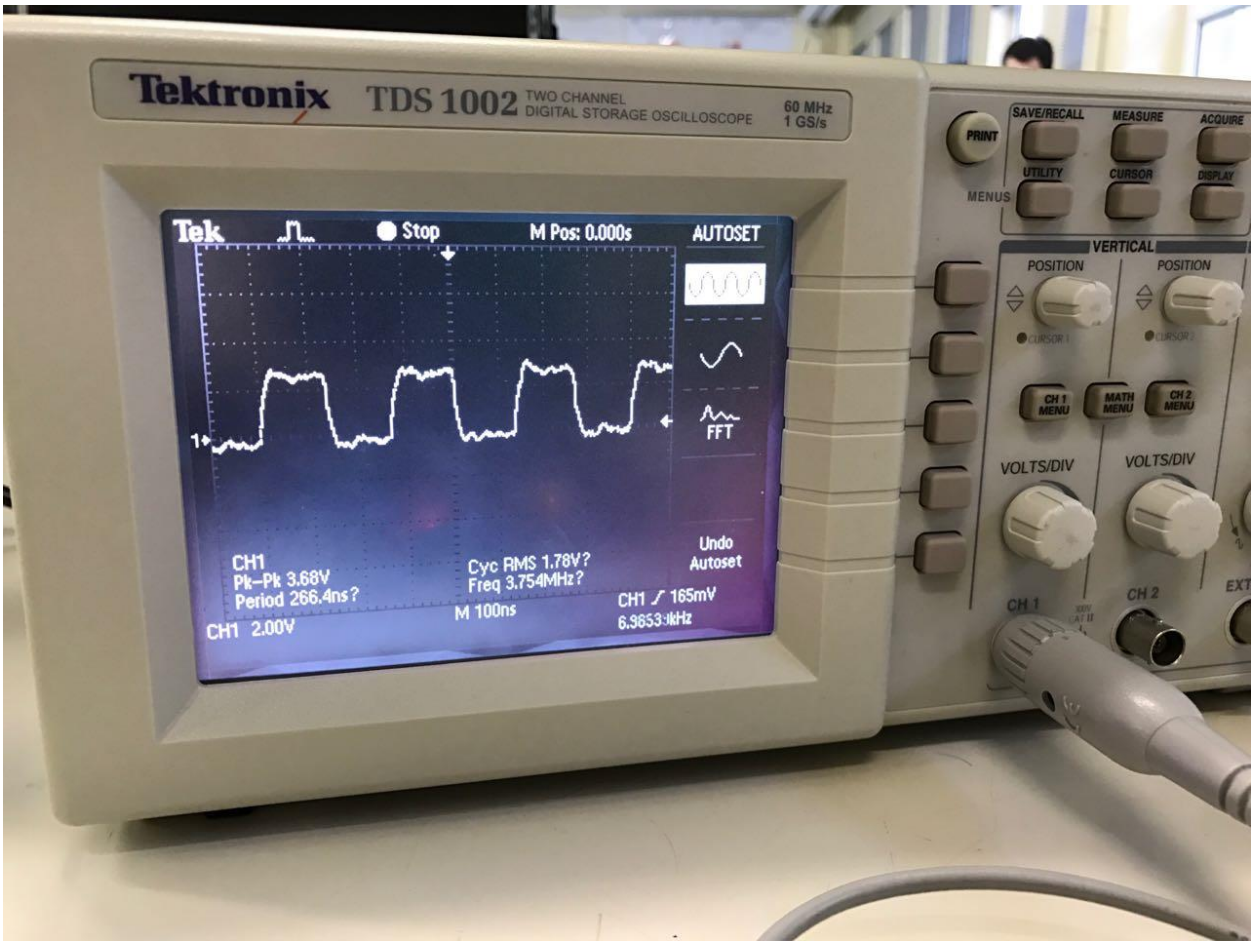

Figure 27 Frequency and wave type of ring oscillator

We see from figure 25 that output frequency is 3.754MHz.