

Assignment B-3 Exercise 3.0 Part 1 and Part 2

3. Combinational Logic Circuits

Lab. Exercise 3.0 Part 1

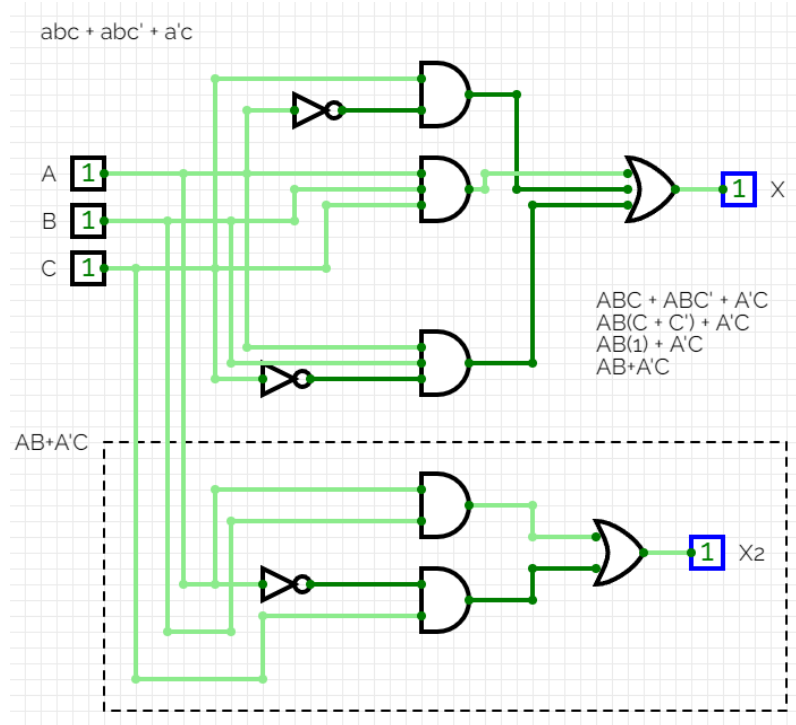
- **Exercise 3-0:** Practice the Simulator
 - Design the Digital Circuit for
 - $abc + abc' + a'c$
 - 1) STEP 1: Use the **original** algebra expression
 - 2) STEP 2: Design the Logic Circuit
 - 3) STEP 3: Draw the Logic Circuit in the Simulator
 - 4) STEP 4: Prove the circuit output is correct.
 - Show the output status based on the Truth Table
 - Create a **testbench**
 - Fill out the truth table for this algebra expression
 - Validate your truth table
 - Run all

3. Combinational Logic Circuits

Lab. Exercise 3.0 Part 2

- **Exercise 3-0:** Practice the Simulator
 - Design the Digital Circuit for
 - $abc + abc' + a'c$
 - 1) STEP 1: **Simplify** the algebra expression
 - 2) STEP 2: Design the Logic Circuit
 - 3) STEP 3: Draw the Logic Circuit in the Simulator
 - 4) STEP 4: Prove the circuit output is correct.
 - Show the output status based on the Truth Table
 - Create a **testbench**
 - Fill out the truth table for this algebra expression
 - Validate your truth table
 - Run all

1.) Design Screenshot



2.) Testbench

Title:

Sequential Test Combinational Test

	INPUTS <input type="checkbox"/>			OUTPUTS <input type="checkbox"/>	
Label	A	B	C	X	X2
Bitwidth	1	1	1	1	1

Group 1

Click + to add tests to the group

0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	1

+ New Group

Import from CSV Export as CSV Attach

3.) Test Result

TESTBENCH

Test: Test

Type: Combinational

Edit

Remove

Group: < Group 1 >

Case: < 1 >

LABELS	A	B	C	X	X2
Bitwidth	1	1	1	1	1
Current Case	0	0	0	0	0
Result					

Validate

Run All

8 out of 8 Tests Passed [View Detailed](#)