

Assignment B-8 Exercise 3.5 Project 1 and 2. RS Latch with Clock and JK Latch

3. Combinational Logic Circuits

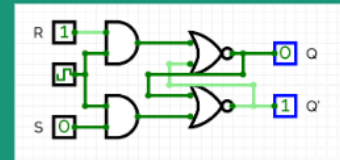
R-S Latch and D-Latch

- **Exercise 3-5:** draw the circuits by using the logic simulator

- Project 1

- Draw the clocked RS Latch with (AND, OR , and NOT gate)

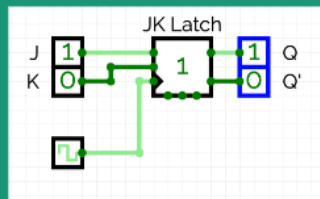
- 1) Draw the full circuits RS Latch without any sub-circuit
- 2) Add the clock on the RS Latch so as to draw the RS Flip-Flop
- 3) Show the test results



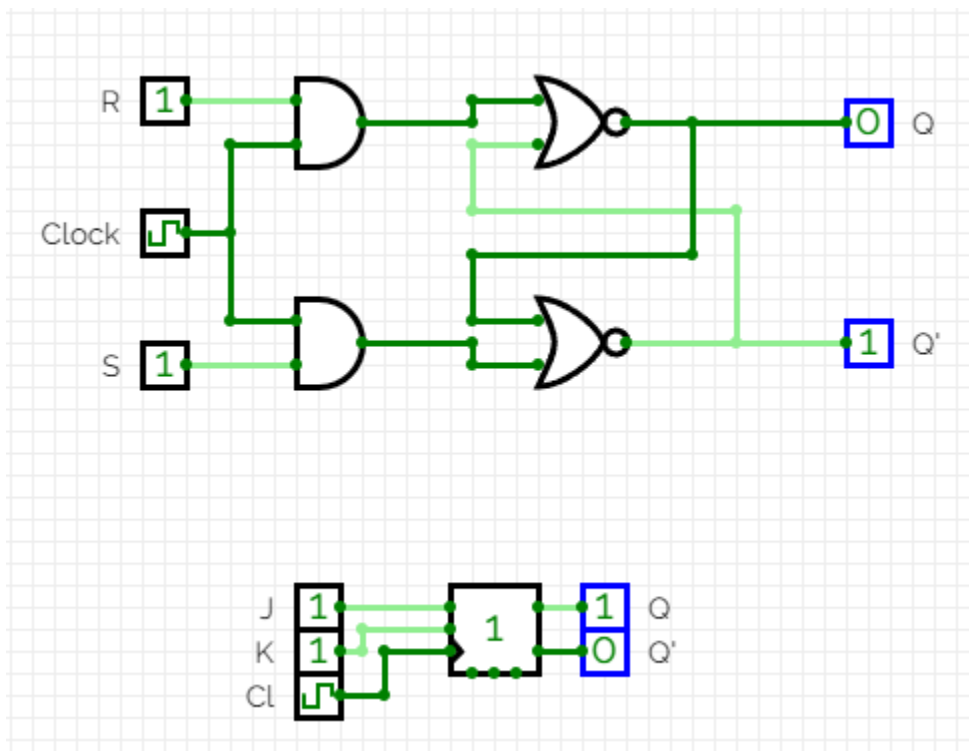
- Project 2

- Draw the clocked JK Latch

- 1) Draw the JK Latch with the built-in JK FFs Sequential Element
- 2) Show the test results



1) Design Screenshot



2) Testbench

Title:

Sequential Test

Combinational Test

	INPUTS +			OUTPUTS +	
Label	S	R	Clock	Q	Q'
Bitwidth	1	1	1	1	1

Group 1

Click + to add tests to the group

0	0	1	no change	hold <u>prev</u> state
1	0	1	1	0
0	1	1	0	1
1	1	1	invalid	invalid

Title:

Sequential Test

Combinational Test

	INPUTS +			OUTPUTS +	
Label	J	K	Clock	Q2	Q'2
Bitwidth	1	1	1	1	1

Group 1

Click + to add tests to the group

0	0	1	no change	hold <u>prev</u> state
1	0	1	1	0
0	1	1	0	1
1	1	1	change	to opposite state

3) Test Result

Kept getting “duplicate input” errors. None of the inputs are labeled the same. Could be caused by the loop itself but I have no idea how to fix/test it correctly. 😞 I wrote notes in the test bench.