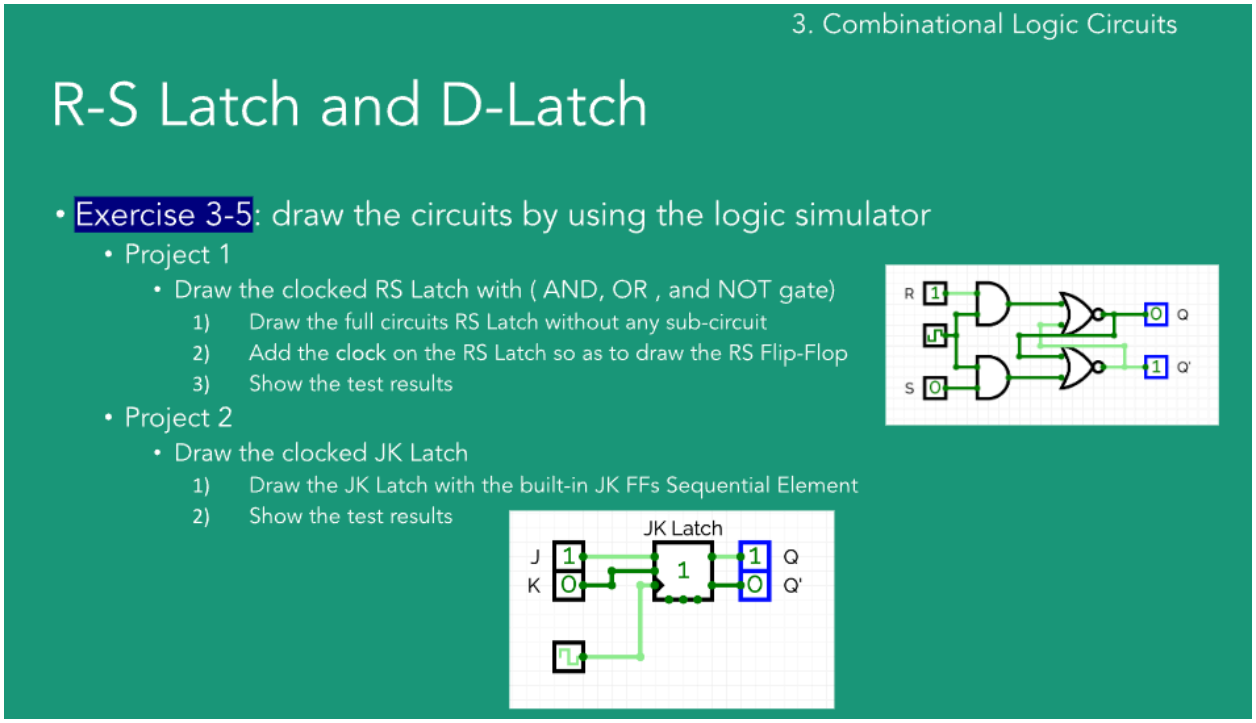
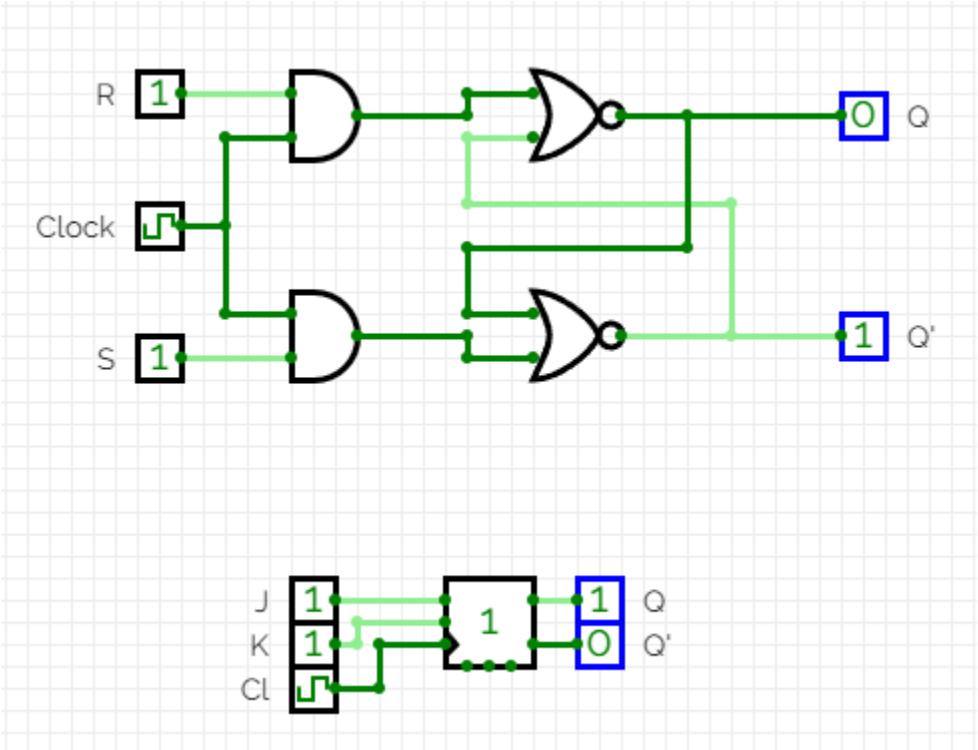
Assignment B-8 Exercise 3.5 Project 1 and 2. RS Latch with Clock and JK Latch



1) Design Screenshot



2) Testbench

Title: Test1

Sequential Test | Combinational Test

	INPUTS ⊕			OUTPUTS ⊕	
Label	**S**	**R**	**Clock**	**Q**	**Q'**
Bitwidth	1	1	1	1	1

Group 1

Click + to add tests to the group

0	0	1	no change	hold prev state
1	0	1	1	0
0	1	1	0	1
1	1	1	invalid	invalid

Title: Test2

Sequential Test | Combinational Test

	INPUTS ⊕			OUTPUTS ⊕	
Label	**J**	**K**	**Clock**	**Q2**	**Q'2**
Bitwidth	1	1	1	1	1

Group 1

Click + to add tests to the group

0	0	1	no change	hold prev state
1	0	1	1	0
0	1	1	0	1
1	1	1	change	to opposite state

3) Test Result

Kept getting “duplicate input” errors. None of the inputs are labeled the same. Could be caused by the loop itself but I have no idea how to fix/test it correctly. 😕 I wrote notes in the test bench.