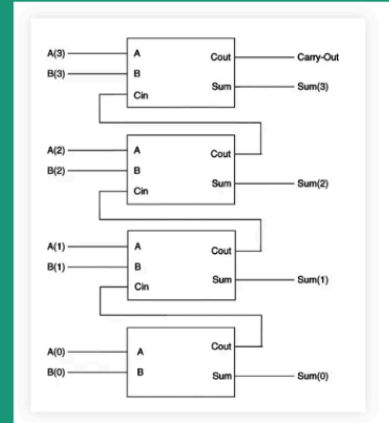


## Assignment B-7 Exercise 3.4 Full Adder

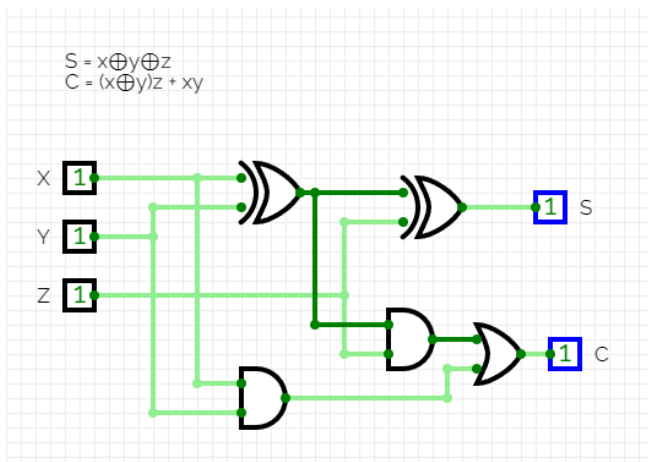
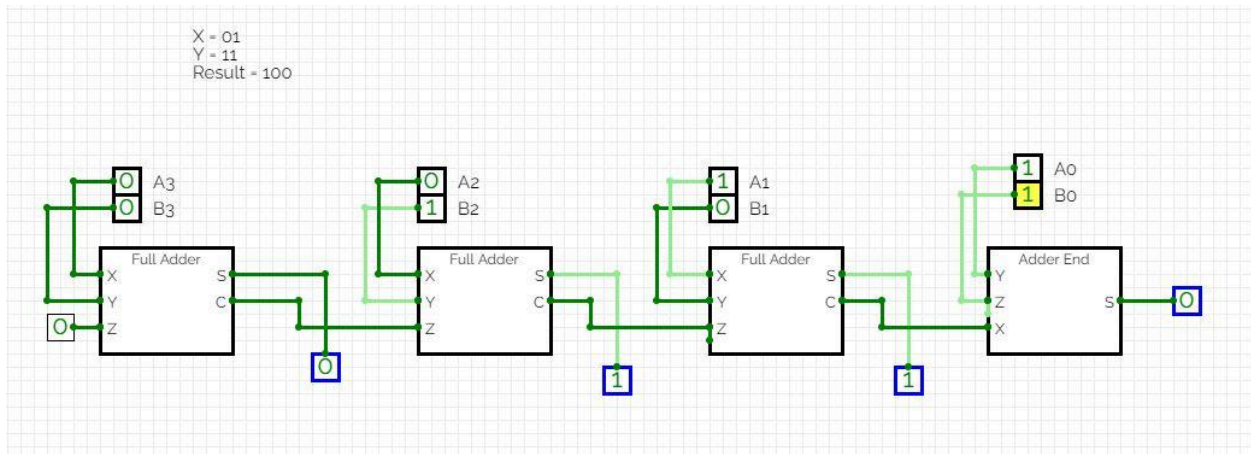
### 3.3.3 Exercise 3-4 : Draw the circuit of Full adder

#### • Exercise 3-4:

- 1) Draw the circuit for 1-bit full adder
- 2) Draw the 4-bits full adder with the entire logic gates
- 3) Draw the circuit for 4-bits full adder using the sub-circuit that was made in step (1)
- 4) Test your circuits with the arithmetic addition of two numbers
  - 1) 0111 + 0101 (Overflow?)
    - show this result by using "testbench"
  - 2) 0011 + 1011 (What is the result as the 2's complement representation)
    - Show your result
    - Elaborate the result with the decimal and binary value



#### 1) Design Screenshot



## 2) Testbench

| Label    | X | Y | Z | C | S |
|----------|---|---|---|---|---|
| Bitwidth | 1 | 1 | 1 | 1 | 1 |

### Group 1

Click + to add tests to the group

|   |   |   |   |   |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

## 3) Test Result

Gates

Decoders & Plexers

Sequential Elements

Annotation

Misc

TESTBENCH

Test: Test 1

Edit Remove

Type: Combinational

Group: < Group 1 >

Case: < 1 >

| LABELS       | X | Y | Z | C | S |
|--------------|---|---|---|---|---|
| Bitwidth     | 1 | 1 | 1 | 1 | 1 |
| Current Case | 0 | 0 | 0 | 0 | 0 |
| Result       |   |   |   |   |   |

Validate Run All 8 out of 8 Tests Passed View Detailed

$$S = x \oplus y \oplus z$$
$$C = (x \oplus y)z + xy$$

X 1

Y 1

Z 1

S 1

C 1