CSM 61C Spring 2020

Boolean Algebra

Exam Question Compilation

This document is a PDF version of old exam questions by topic, ordered from least difficulty to greatest difficulty.

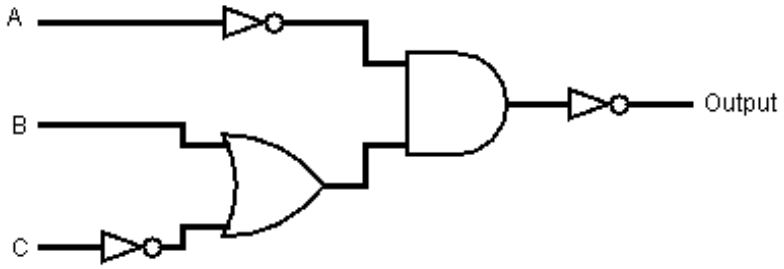
Questions:

- Fall 2015 Final QMT2-1a
- Fall 2018 Final QF2a
- Spring 2018 Midterm 2 Q2a
- Fall 2019 Midterm Q5b
- Fall 2019 Final Q5d
- Summer 2019 Midterm 2 Q3
- Summer 2018 Midterm 2 Q2

SID: _____

MT2-1: Synchronous Finite State Digital Machine Systems (9 points)

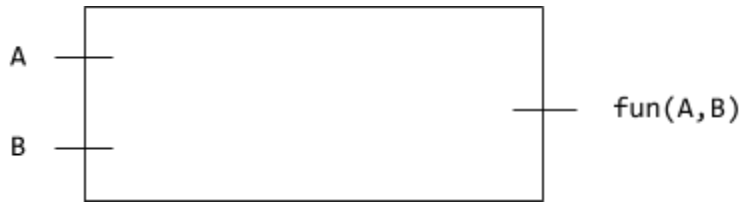
a. The circuit shown below can be simplified. Write a Boolean expression that represents the function of the simplified circuit using the minimum number of AND, OR, and NOT gates.



F2) *SDS* (20 points = 8+5+7, 30 minutes) SID_____

a) Transform the **fun** function below into the *fewest Boolean gates* that implement the same logic. You may use AND, OR, XOR and NOT gates. *Hint: start with the truth table.*

```
bool fun(bool A, bool B) { return (A == B) ? true : B; }
```



Problem 2 ***Tell Us The Truth*** **(17 points)**

X	Y	Z	Out
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(a) Select all of the following expressions that are equivalent to the truth table above.

- O $(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + Z)$
- O $\bar{Z} + Y$
- O $\bar{Y} + Z$
- O $X\bar{Y}Z + \bar{X}\bar{Y}Z$
- O $X\bar{Y} + \bar{X}\bar{Y} + Z\bar{X} + ZX$
- O $\bar{Y} + \bar{Y}Z + Z$

(b) Suppose you wanted to implement $\bar{A} + B$, but the only available gates are NAND gates. What is the minimum number of NAND gates you need to implement the above truth table correctly?

_____

Fall 2019 Midterm
Question 5b

b) Draw the **FULLY SIMPLIFIED** (*fewest* number of primitive gates) circuit for the equation below.
You may use the following primitive gates: AND, NAND, OR, NOR, XOR, XNOR, and NOT.

SHOW YOUR WORK FOR PART (b) BELOW

$$out = \overline{(A + \overline{B}B)} + \overline{(B + \overline{A})(A + BC)}$$

Q5) Watch the clock and don't delay! **(30 pts = 2*5 + 10 + 10)**

d) Draw the **FULLY SIMPLIFIED** (*fewest* primitive gates) circuit for the equation below into the diagram on the lower right. You may use the following primitive gates: AND, NAND, OR, NOR, XOR, XNOR, and NOT**.**

$$out = \overline{(C + AB\overline{C} + \overline{B}\,\overline{C}D)} + \overline{(C + \overline{B + D})}$$

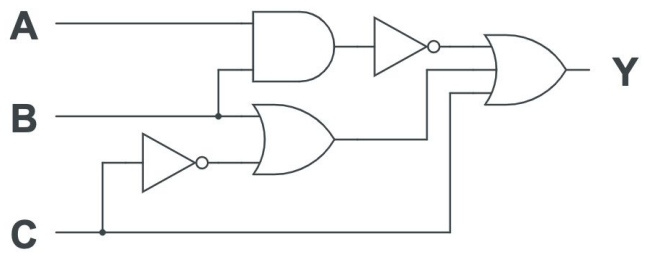
SHOW YOUR WORK IN THIS BOX

Question 3: Are Vulcans good at digital logic? - 14 pts

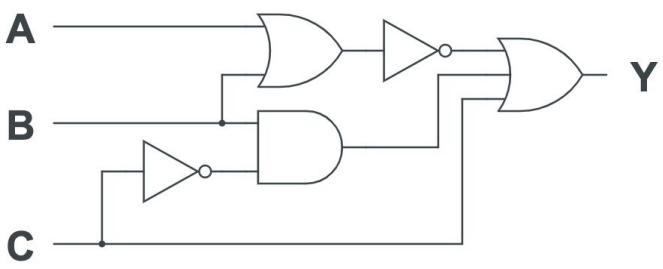
Which circuit diagram exactly matches the following boolean algebra expression?

$$Y = C(\overline{A+B})(B\overline{C})$$

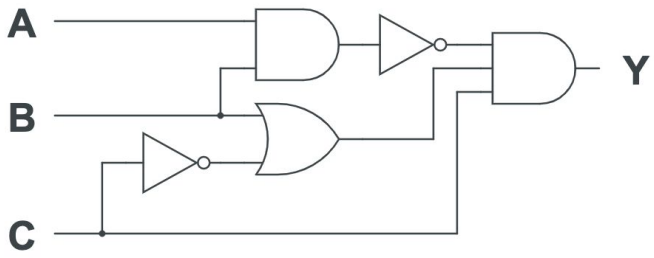
1)



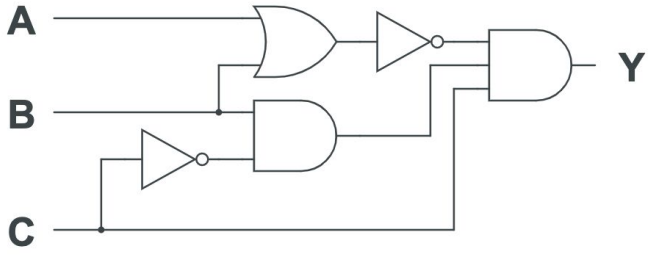
2)



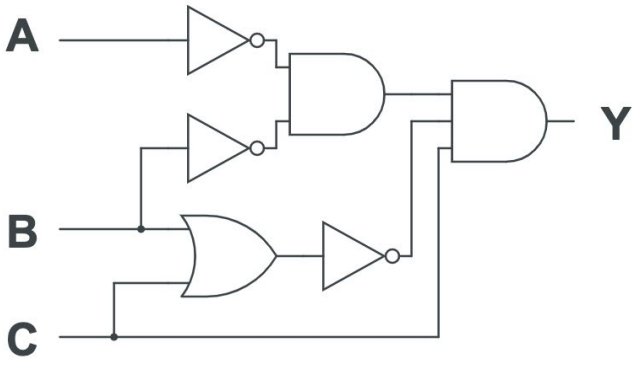
3)



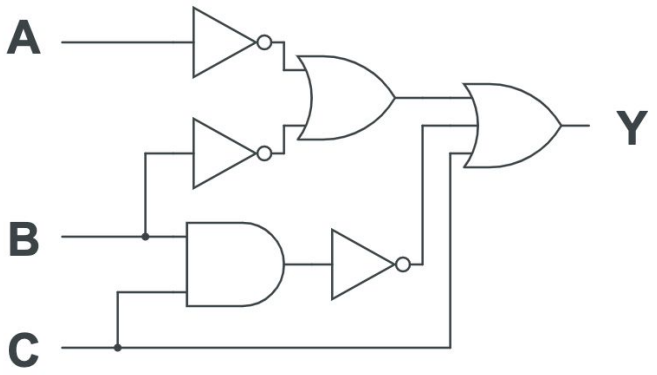
4)



5)



6)



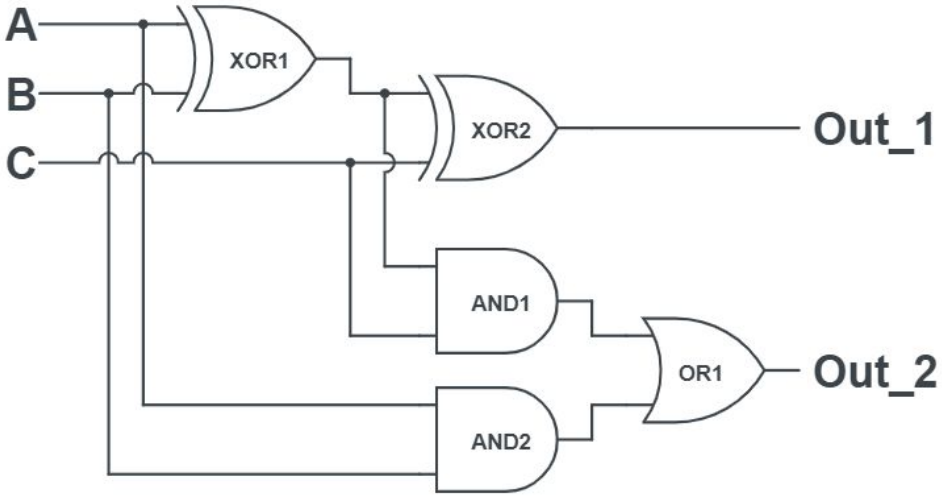
The correct circuit is number: _____

Simplify the following boolean algebra expression. Show your work for partial credit, and you may use any method to simplify.

$$Y = B(AB + A\overline{B})(\overline{AC} + C)$$

Simplified Solution: _____

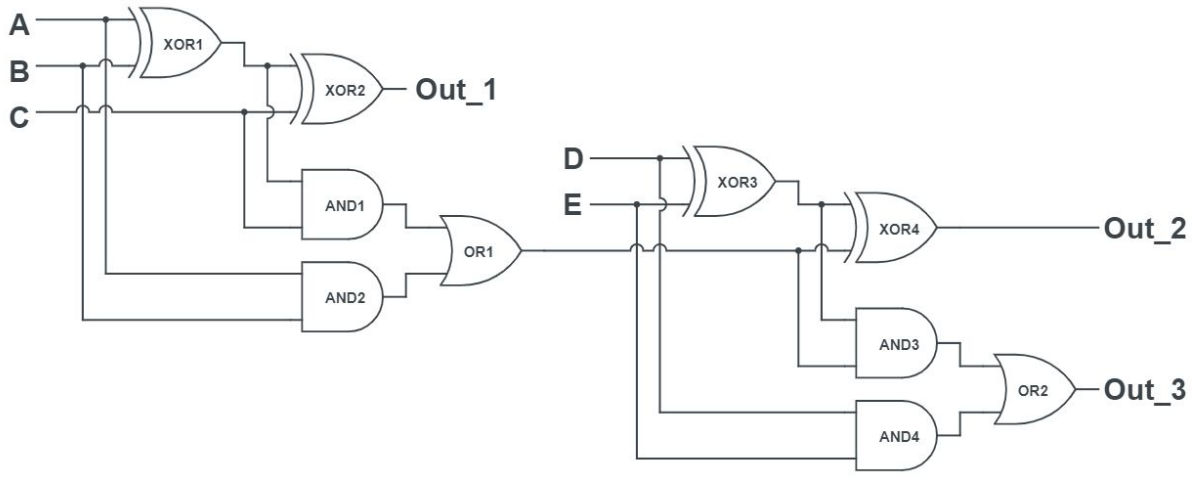
Fill out the following truth table that corresponds to the following circuit.



C	B	A	Out_1	Out_2
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Find the combination logic delays for each output or each circuit given the following parameters. There is no setup or hold time from the inputs or outputs.

- XOR gate delay: 80 ps
- AND gate delay: 60 ps
- OR gate delay: 40 ps



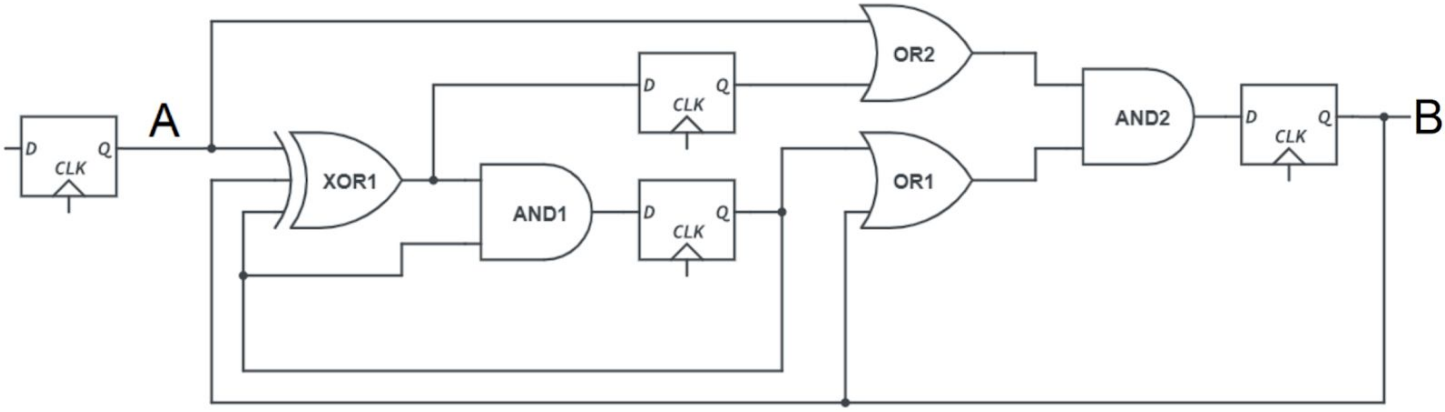
Out_1 Delay: _____

Out_2 Delay: _____

Out_3 Delay: _____

For the next problems, consider the following pipelined circuit. Assume all registers have their clock inputs correctly connected to a global clock signal and that logic gates have the following parameters:

- XOR gate delay: 80 ps
- AND gate delay: 60 ps
- OR gate delay: 40 ps



When shopping for registers, we find two different models and want to determine which would be best for our circuit.

Register Type λ

- Setup Time: 40 ps
- Hold Time: 20 ps
- Clock-to-Q Delay: 30 ps

Register Type τ

- Setup Time: 10 ps
- Hold Time: 10 ps
- Clock-to-Q Delay: 80 ps

What is the minimum latency for the circuit from A to B if we use register type **λ**? _____

What is the minimum latency for the circuit from A to B if we use register type **τ**? _____

SID: _____

Question 2: Simple Democratic Selection (12 pts)

As the semester is reaching a close, Steven, Nick, and Damon are busy determining the difficulty of the final exam. All three will vote on whether the final should be easy or hard, but the final decision will always be made based on the following rules:

Rule 1. If the vote is unanimously hard or unanimously easy, then it will be hard or easy, respectively.
Rule 2. If Damon disagrees with Steven and Nick, then Damon's vote will be chosen.
Rule 3. If Steven and Nick differ, then the minority vote will be chosen.
Else In all other situations, the outcome can be either easy or hard (i.e. they can be anything)

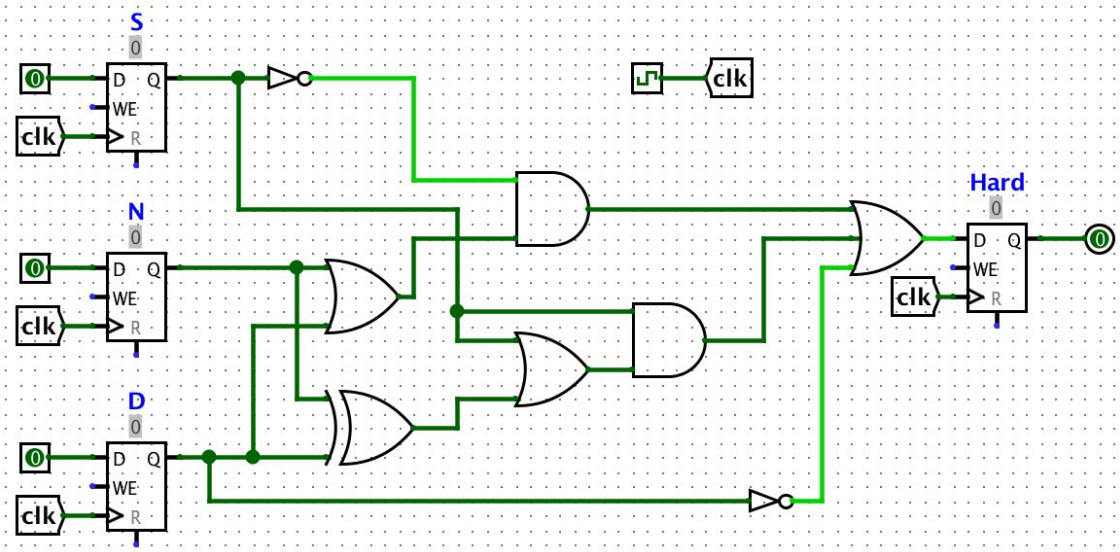
We will represent Steven's vote with the variable **S** which takes on values of 0 (easy) and 1 (hard). Similarly, Nick's vote is represented as **N** and Damon's vote is represented as **D**. For each rule, write out the **simplest** boolean logic expression using these three binary inputs that outputs whether or not the final exam will be easy or hard. Note: the symbol for XOR is $\oplus$.

Rule 1: _____ **Rule2:** _____ **Rule3:** _____

Below is a boolean algebra expression that models this problem. Simplify it into as few gates as possible:

$\overline{S}\,(N+D) \;+\; S(S \;+\; (N \oplus D)) \;+\; \overline{D}$ Simplified: _____

For the next 2 questions, refer to the circuit diagram below which models the unsimplified boolean expression:



You are given that all logic gates have a propagation delay of 5ps, the register clk-to-q delay is 3ps, the register hold time is 11ps, and the setup time is 8ps. What is the critical path delay of this circuit?

Critical path delay: _____ ps

Using the assumptions above, what is the smallest value that the clk-to-q can be and **not** cause a hold-time violation?

clk-to-q: _____ ps