

Each of the 16 inputs has the function applied to them (w/ 2 possibilities per output)

Lecture 16: Combinational Logic

Logic Gates

AND $A \cdot B = D$

OR $A + B = C$

NOT $A \rightarrow \neg A$

XOR $A \oplus B = C$

NAND $A \cdot B = D$

NOR $A + B = D$

XOR rule: 1 if # 1's in the input is odd

FSM Circuit



PS	INP	NS	OUT
00	0	00	0
00	1	01	0
01	0	00	0
01	1	10	0
10	0	00	0
10	1	00	1

$$INP \cdot \overline{PSo} = PS_1$$

Laws of Boolean Algebra

Complementarity: $x \cdot \overline{x} = 0, x + \overline{x} = 1$

0's and 1's: $x \cdot 0 = 0, x + 1 = 1$

Identity: $x \cdot 1 = x, x + 0 = x$

Idempotency: $x \cdot x = x, x + x = x$

Associativity: $x(y+z) = (x+y)z = x$

Distributivity: $x(y \cdot z) = (x \cdot y)(x \cdot z)$

DeMorgan's: $\overline{xy} = \overline{x} + \overline{y}, \overline{x+y} = \overline{x} \cdot \overline{y}$

Canonical Form

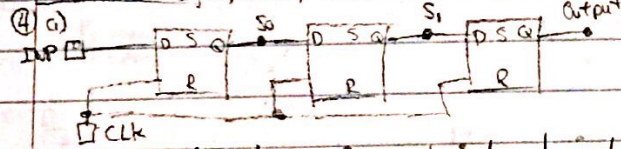
- Sum of products: $y = \overline{A} \cdot \overline{B} + \overline{A} \cdot B + A \cdot \overline{B} + A \cdot B$
- From canonical form, use boolean algebra to simplify the expression
- Can build circuit from simplified form
- Boolean expression as intermediate b/w truth table & Gate Diagram to work w/ simplest possible expression

Example: $y = \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot C$

$$y = \overline{A} \cdot B \cdot (C + \overline{C}) + A \cdot \overline{B} \cdot (C + \overline{C})$$

$$y = \overline{A} \cdot B + A \cdot \overline{B}$$

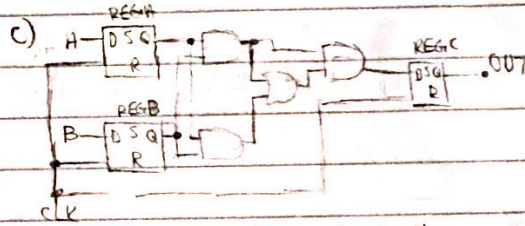
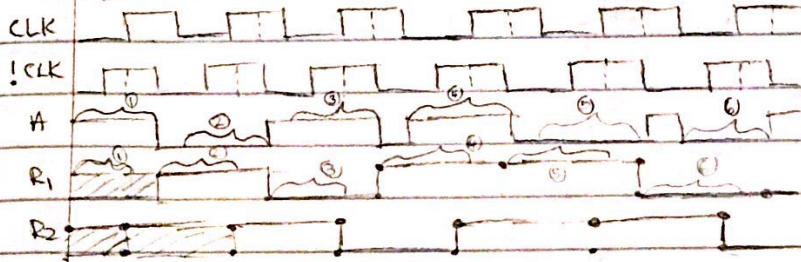
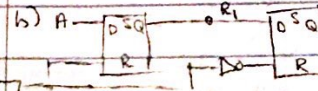
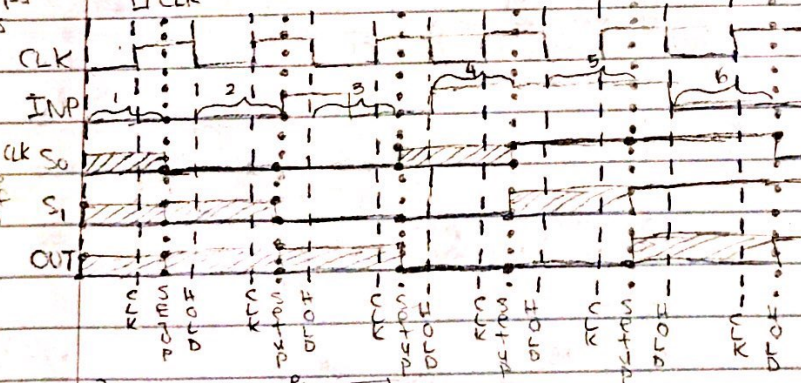
Disc 6 - Logic, FSM, SDS



CLK Period: 8ps
clk to Q: 2ps
Setup: 4ps
Hold: 2ps

- Samples INP on rising edge of clk
- Initial state S0
- Samples INP if steady from setup across hold

NOT Delay: 2ps



REG A/B: Setup=Hold=clk-to-Q=4ns
Logic Gate Delay=5ns
REG C: Setup=6ns
Max hold time for Reg C = earliest possible time for input to change = CTQ of prev register + Shortest CL = 4+2.5=6.5ns
Minimum acceptable clock cycle time = Longest possible time of completion b/w any 2 registers = CTQ (starting Reg) + Longest CL + Setup (Ending Reg) = 4+5+3+6=25ns