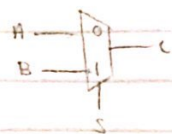
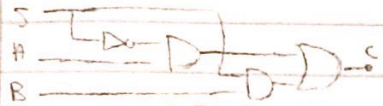


Lecture 17: Combinational Logic Blocks

Data Multiplexer (2-to-1)

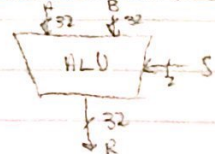


- $C = \bar{S}A + SB$
- Not $S \Rightarrow$ Choose A
- $S \Rightarrow$ Choose B

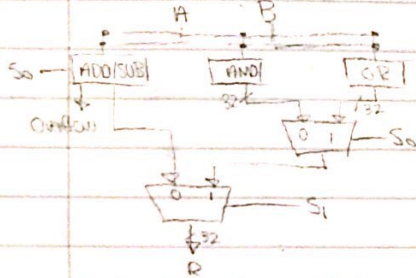


$$E = \bar{S}_1 \cdot \bar{S}_0 \cdot A + \bar{S}_1 \cdot S_0 \cdot B + S_1 \cdot \bar{S}_0 \cdot C + S_1 \cdot S_0 \cdot D$$

Arithmetic Logic Unit

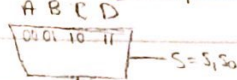


- $S=00 \Rightarrow R = A+B$
- $S=01 \Rightarrow R = A-B$
- $S=10 \Rightarrow R = A \& B$
- $S=11 \Rightarrow R = A | B$



- S_1 simultaneously used to select subblock along w/ add/sub
- Need to deal w/ overflow for add/sub
- subblock just constituted by 32 series of bitwise operations

4-to-1 Multiplexer

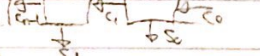
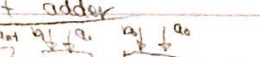
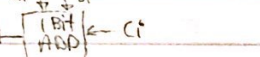
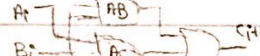


$$E = \bar{S}_1 \cdot \bar{S}_0 \cdot A + \bar{S}_1 \cdot S_0 \cdot B + S_1 \cdot \bar{S}_0 \cdot C + S_1 \cdot S_0 \cdot D$$

- Use 2-to-1 multiplexers to select initial A/B & C/D
- choose b/w those w/ S_1

1-bit Adder

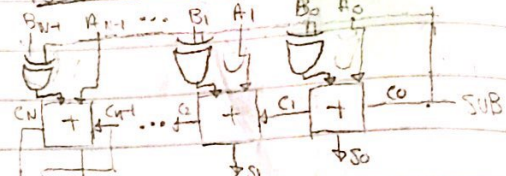
$$\begin{aligned} A: A_0 & S_0 = a_0 \text{ XOR } b_0 \\ + B: B_0 & C_1 = a_0 \text{ AND } b_0 \\ \dots S_i & S_i = \text{XOR}(a_i, b_i, c_i) \\ & C_{i+1} = \text{MAJ}(a_i, b_i, c_i) \\ & = a_i b_i + a_i c_i + b_i c_i \end{aligned}$$



Overflow

- Unsigned: if $C_{n+1} = 1 \Rightarrow$ OVERFLOW
- bit not enough to represent
- 2's C: $00=0, 01=1, 10=-2, 11=-1$
- $00 + \text{Anything} = \text{Anything} \Rightarrow$ Fine
- $* 01 + 01 (1+1) = 10 (-2) \Rightarrow$ Overflow [$C_{in}=1$]
- $C_{out}=0$
- $01(1) + 10(-2) = 11(-1)$
- $01(1) + 11(-1) = 100(0) \Rightarrow$ Fine
- ($C_{in}=1, C_{out}=1$)
- $* 10(-2) + 10(-2) = 100(-4) \Rightarrow$ Overflow
- ($C_{in}=0, C_{out}=1$)
- $* 10(-2) + 11(-1) = 101(-3) \Rightarrow$ Overflow
- ($C_{in}=0, C_{out}=1$)
- $11(-1) + 11(-1) = 110(-2) \Rightarrow$ Fine
- KEY FORMULA: Overflow = $C_n \text{ XOR } C_{n+1}$

SUBTRACTOR: $A-B = A+(-B)$



X	Y	XOR(X,Y)
0	0	0
0	1	1
1	0	1
1	1	0

- XOR acts as a conditional inverter
- IF SUB=1 \Rightarrow Invert B's bits & add 1 to perform 2's C unit

represented by carry-in & carry-out of final adder