Lecture 14: Synchronous Digital Systems

- Synchronous: operations record. by a central clock
- Digital: all values are discrete (can be treated as 1's & 0's)
- Hardware design: useful to understand capabilities/limitations (esp. processors)

Circuits

- key idea: open/close a switch to repr. 0 or 1
  - can combine switches to perform Boolean logic
- Shannon saw how circuits from switches resembled Boole's math findings
  - Boolean logic

OR / AND

- Transistor: device that amplifies/switches signals
  - Prev: vacuum tubes, curr: integrated circuit

MOS Transistor

MOS Transistor: Drain, Gate, Source

N-Channel

- Open when G is low
- Close when V(G) > V(S) + ε

P-Channel

- Closed when G is low
- Open when V(G) < V(S) + ε

RULES: Node should never be connected directly to source & ground (short-circuit)
& Node must be connected to either source or ground (can't be neither)

NOT

High X ⇒ G1 open, G2 closed
Low X ⇒ G1 closed, G2 open
Hence, this acts as a NOT Gate

NAND

Intuition: when A or B is low, then either G1 or G2 is closed, so source ⇒ C
when both are high, C is connected to ground

SIGNALS

- Signals: treated as 0/1 in digital domain (treat time transmission as negligible & can only carry 1 value)
  - REALITY: there is delay

Signal Grouping: can treat N signals as an N-bit # (easier to repr)

Adder Circuit Delay

4 bit, 4 bit (input)
4 bit (output)

Propagation Delay

Insert circuit name here

Interval is adder propagation delay: diff btw output for prev inputs and arrival of next set of inputs

Types of Circuits

- Combinational Logic (CL) circuits: output only looks at inputs (no side effects)
  - Example: adder circuit
- State elements: store info in a circuit (more than just y = f(x))

LOAD — Register — IN / OUT

- Store input in LOAD & only re-store when signal (3V) received to refetch from IN

CLOCK — Register — IN / OUT

- Frequently used in content of a clock
  - periodically store inputs w/ regularity of clock signal