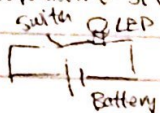


Lecture 14: Synchronous Digital Systems

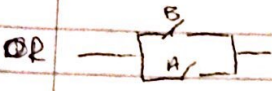
- Synchronous: operations coord. by a central clock
- Digital: all values are discrete (can be treated as 0's & 1's)
- Hardware design: useful to understand capabilities/limitations (esp. processors)

Circuits



key idea: open/close a switch to repr. 0 or 1
• can combine switches to perform Boolean logic

- Shannon saw how circuits from switches resembled Boole's math findings
• Boolean logic



AND

Transistor: device that amplifies/switches signals
• Prev: vacuum tubes, curr: integrated circuit

MOS Transistor

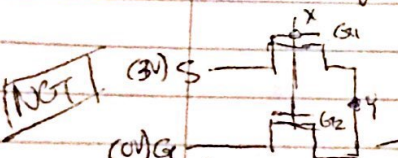
MOS Transistor: Drain, Gate, Source

N-Channel

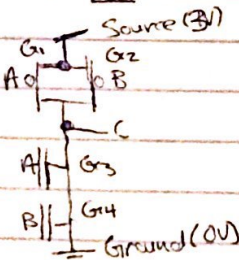
P-Channel

- Open when G is low
- Close when $V(G) > V(S) + E$
- Close when G is low
- Open when $V(G) > V(S) + E$

RULES: Node should never be connected directly to source & ground (short-circuit)
• Node must be connected to either source or ground (can't be neither)

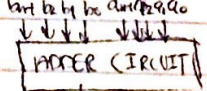


High X \Rightarrow G₁ open, G₂ closed
Low X \Rightarrow G₁ closed, G₂ open
Hence, this acts as a NOT Gate

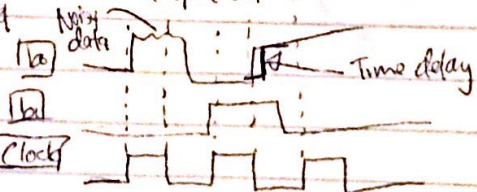


A	B	C
0	1	1
0	0	1
1	1	0
1	0	1

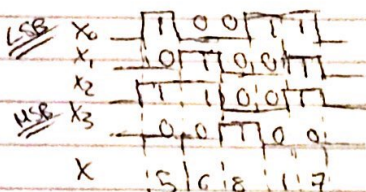
Intuition: when A or B is low, then either G₁ or G₂ is closed, so source \Rightarrow C when C is connected to ground



Take n n-bit inputs and spit out a #



Signal Grouping: can treat N signals as an n-bit # (easier to repr)



Adder Circuit Delay

4 bit, 4 bit (input)
4 bit (output)



A	B	C
2	3	5
3	4	7
4	5	9
5	6	11

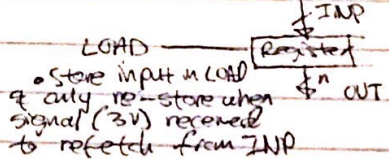
Blank Propagation Delay

Insert circuit name here

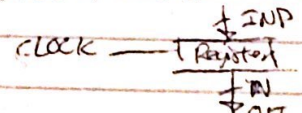
Interval is adder propagation delay: diff b/w output for per inputs and arrival of novel set of inputs

Types of Circuits

- Combinational Logic (CL) circuits: output only, nodes at inputs (no state effects)
• Example: adder circuit
- State elements: store info in a circuit (more than just $y = f(x)$)



store input in LOAD & only re-store when signal (3V) received to refresh from I/O



- Frequently used in context of a clock
- periodically store inputs w/ regularity of clock signal

NOT

AND

SIGNALS

- Signals: treated as 0/1 in digital domain (treat time transmission as negligible & can only carry 1 value)
- REALITY: there is delay