Each of the (6) inputs has the function applied to them (w/ 2 possibilities per outputs)

AND – find inputs, then apply not
OR – OR inputs, then apply not

Lecture 16: Combinatorial Logic

Logic Gates

- 16 possible inputs (a,b,c,d)
- 2^{16} possible bit patterns

AND, OR, NOT, XOR, NAND, NOR

XOR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

⇒

A	Y
0	B
1	$\overline{B}$

• XOR rule: 1 iff # 1's in the input is odd

Laws of Boolean Algebra

Complementarity: $x \cdot \overline{x} = 0$, $x + \overline{x} = 1$
0's and 1's: $x \cdot 0 = 0$, $x + 1 = 1$
Identity: $x \cdot 1 = x$, $x + 0 = x$
Idempotent: $x \cdot x = x$, $x + x = x$
Limiting: $xy + x = x$, $(x+y) \cdot x = x$
Demorgan's: $\overline{xy} = \overline{x} + \overline{y}$, $\overline{x+y} = \overline{x} \cdot \overline{y}$

Commutative: $x \cdot y = y \cdot x$, $x + y = y + x$
Associative: $(xy)z = x(yz)$, $(x+y)+z = x+(y+z)$
Distributive: $x(y+z) = xy+xz$, $x+yz = (x+y)(x+z)$

Canonical Form

- Sum of products: $y = \overline{A} \cdot \overline{B} + A\overline{B} + \overline{A}C$..
- From canonical form, use boolean algebra to simplify the expression
- Can build circuit from simplified form
- Boolean expression as intermediary b/w truth table & Gate Diagram to work w/ simplest possible expression

Example: $y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,C + AB\overline{C} + ABC$
$y = \overline{A}\,\overline{B}(\overline{C}+C) + A\overline{C}(\overline{B}+B)$
$y = \overline{A}\,\overline{B} + A\overline{C}$

2 Bit Adder

A	B	H	B	C
00	00	00	00	000
00	01	00	01	001

Carry out / 3rd bit

Majority Circuit

AB + BC + AC — If 2/3 or more of inputs are 1's, output true

FSM Circuit

PS	INP	NS	OUT
00	0	00	0
00	1	01	0
01	0	00	0
01	1	10	0
10	0	00	0
10	1	00	1

$INP \cdot \overline{PS_0} \cdot DS_1$

Disc 6 – Logic, FSM, SDS

④ a)

CLK Period: 8ps
Clk to Q: 2ps
Setup: 4ps
Hold: 2ps

S_0
- Samples INP during rising edge of CLK
- Initially garbage
- Samples INP if steady from setup across hold

S_1

OUT

---- CLK
---- SETUP
•••• HOLD

NOT Delay: 2ps

b)

c)

REG A/B: Setup = Hold = Clk-to-Q = 4ns
Logic Gate Delay = 5ns
REG C: Setup = 6ns

• Max hold time for Reg C = earliest possible time for input to change = CTQ of prev register + Shortest CL = 4+2.5 = 14ns
• Minimum acceptable clock cycle time = Longest possible time of completion b/w any 2 registers = CTQ(Starting Reg) + Longest CL + Setup(Ending Reg) = 4+5·3+6 = 25ns

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