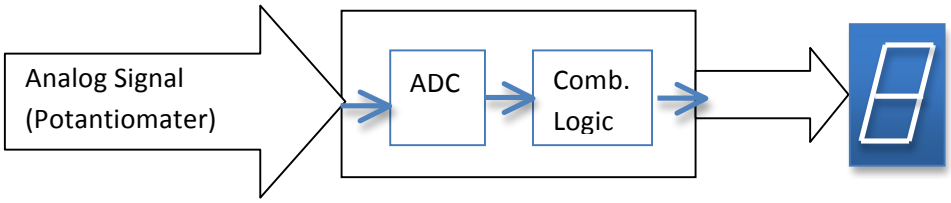
Marmara University Electrical-Electronics Eng. Dept.

CSE315.02 Digital Design Laboratory Assignment #3

The studies will be presented after 2 weeks (Lab sections). **Each group must present their own study. The group members have to work together and each member must know each step of the study.**

For this laboratory assignment, you will use Altera Quartus II software and DE-115 FPGA kit and design an analog signal comparator that has the Input/output definitions below.



- The analog signal, which comes from potantiometer's output is changing from 0 to 3V. The pot. circuit can be seen on the figure below. Here Vcc=3V will be supplied from FPGA kit.
- The ADC IC: 0804 should be used in ADC block, which has 8-bit digital output. These outputs should be connected to the FPGA pins. The supply voltage for ADC block is provided by FPGA kit.
- Combinational logic will be designed by using three 8-bit comparators that include 4x1 multiplexers.
- The circuit should measure the analog input and the voltage value should be displayed on seven segment according to following rules:

$0 \leq Vin < 0.5$ → '0' should be displayed

$0.5 \leq Vin < 1.5$ → '1' should be displayed

$1.5 \leq Vin < 2.5$ → '2' should be displayed

$2.5 \leq Vin < 3.0$ → '3' should be displayed

1. Design a 4x1 multiplexer module,

2. Design the 8-bit comparator module (Use the multiplexer modules),

3. Use the comparator modules and generate the proper LCD outputs and derive the FPGA code.

4. Synthesize the circuit, program the FPGA, and verify its operation.