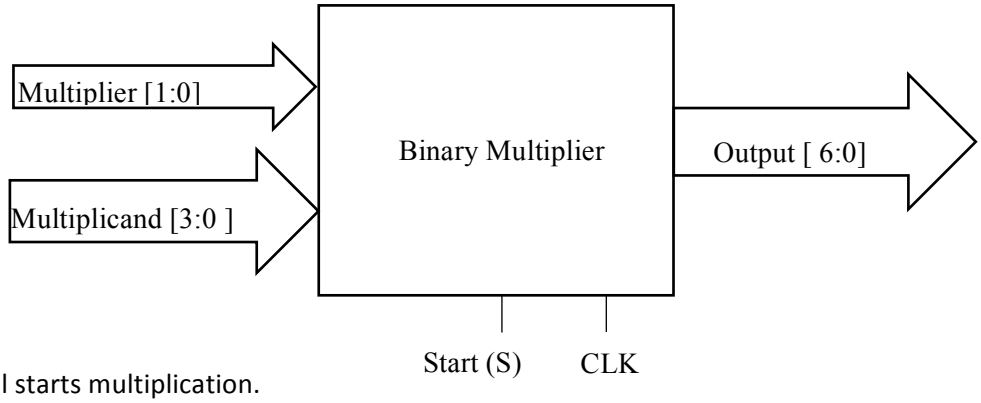
Marmara University Electrical-Electronics Eng. Dept.
CSE315.02 Digital Design Laboratory Assignment #5

The studies will be presented after 2 weeks (First Sunday after the end of Final exams).

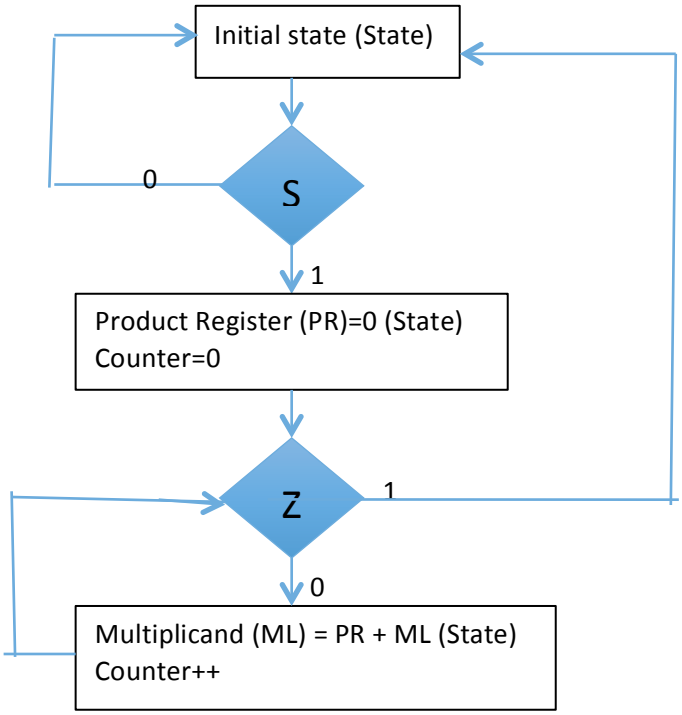
Each group must present their own study. The group members have to work together and each member must know each step of the study.

For this laboratory assignment, you will use Altera Quartus II software and DE-115 FPGA kit and design a binary multiplier that has the Input/output definitions below.



- S signal starts multiplication.
- CLK is the pulse signal which controls the flow in sequential circuit.
- Multiplicand is a 4-bit binary number input.
- Multiplier is 2-bit binary number input.
- Output has 6 bits.

Multiplication will be performed by adding the 'multiplicand' number. 'Multiplier' times addition will give the result. The following chart may help you to understand the required states and signals:



The Z signal is produced by comparing the Multiplier (ML) and the counter. This signal is logic1 if Counter = ML. otherwise Z=0. Adder circuit should add the ML to the PR until Z=1 is obtained.

1. Determine the sub-blocks and their inputs/outputs to built the binary multiplier.
2. Design these sub-blocks (i.e.: Adder block)
3. Develop the state diagram
4. Design the logic circuit.
5. Implement the circuit using FPGA.