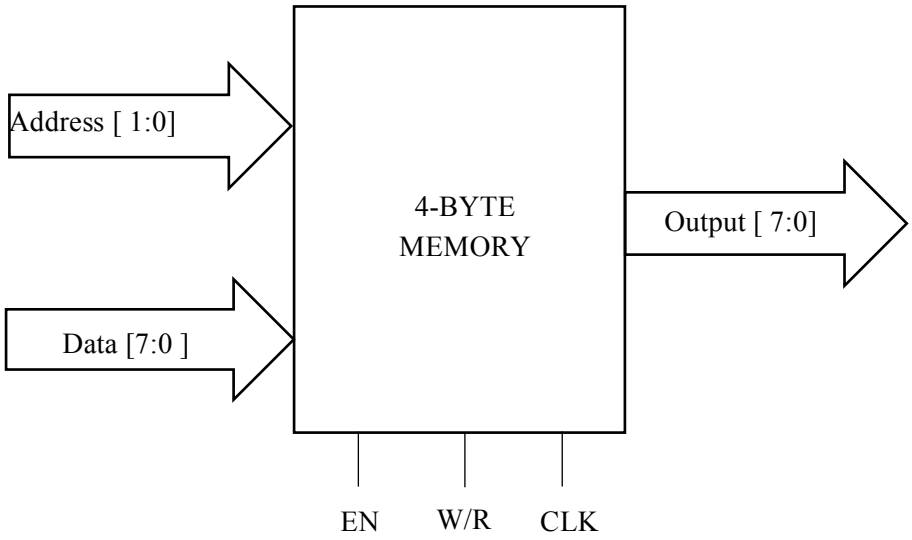
Marmara University Electrical-Electronics Eng. Dept.

CSE315.02 Digital Design Laboratory Assignment #4

The studies will be presented after 2 weeks (Lab sections). **Each group must present their own study. The group members have to work together and each member must know each step of the study.**

For this laboratory assignment, you will use Altera Quartus II software and DE-115 FPGA kit and design an 4-byte write/read Memory that has the Input/output definitions below.



- EN signal enables the module, The output is always zero if EN=0.
- W/R signal defines the operation mode. Output shows the data in the given adrress when W/R =1 (Read mode). The Data will be stored to the Address location if W/R = 0.
- CLK is the pulse signal which should be connected to Flip Flops.
- 4 Byte will be addressed using 2-bit Address input.
- Each Adress stores 8-bit data.

Hint: Each address should be built using Flip-Flops. Each Flip-flop stores 1-bit data. Use a DeMUX to select the required address.

1. Design a Flip Flop module (i.e: D-FF.).

2. Connect the Flip-Flops in order to built 8-bit data memory.

2. Design a DEMUX module,

3. Design the 4-byte memory module as a top-level module (Use the Flip-Flop modules and DEMUX modules)

4. Use the 4-byte memory module and derive the FPGA code.

5. Synthesize the circuit, program the FPGA, and verify its operation.