Project 2

Due Date April 25, 2019

Design a timing game on Cyclone 3 board with Verilog.

- There will be different levels. At least 5 levels.
- Levels and points can be seen through 7-seg displays on DE0 board.
- The LED(s) will slide to left and right.
- The number of LEDs, the speed and direction will change during levels.
- If the user selects the right switch corresponding to the turned on LED the user wins the corresponding level.
- Next level must be harder.
- At any level, the longer the user waits the less points he gets.
- Wrong switches can speed up the LEDs.
- You can ask arithmetic questions when he wins to continue on the next level.
- All improvements based on your imaginations will get extra credit if they deserve and how much they deserve.
- You must perform tesbench simulation with Modelsim.
- You must program Cyclone III FPGA board.
- **Your FSM must use three always blocks as shown.**
- **You must have a distinct datapath block.**
- **No FSM no points.**

Please do NOT be harsh on the DE0 board.