Model Based Testing

Michael Foster Based on material from Professor Rob Hierons

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- Formal models of systems (FSMs)

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- Testing from Finite State Machines

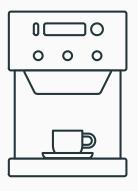
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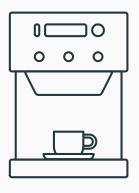
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 - Unique I/O sequences (UIOs)
 - · The W method

Motivating Example - Simple Drinks Machine



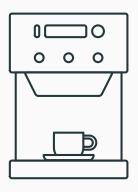
Select a drink

Motivating Example - Simple Drinks Machine



- · Select a drink
- Insert coins

Motivating Example - Simple Drinks Machine



- · Select a drink
- · Insert coins
- Press "vend" to dispense drink

Unit testing

 \cdot Generate tests according to code components

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- · Aim to achieve some level of code coverage

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- Model is a specification or description of a property of interest, often an abstraction and relatively understandable

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- Generate tests according to a formal model
- Model is a specification or description of a property of interest, often an abstraction and relatively understandable
- · Aim to achieve some level of model coverage
- Usually black-box and complements white-box testing
- Major benefits if the model has a formal semantics potential for automation!

There are lots of different modelling notations (Z, B, state machines) We will introduce MBT with state machines

An FSM (Mealy machine) is a sextuple $(S, s_0, X, Y, \delta, \lambda)$ where

· S is a finite set of states

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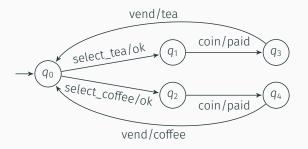
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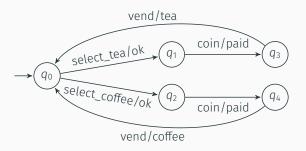
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We can extend δ and λ to take sequences giving δ^* and λ^*

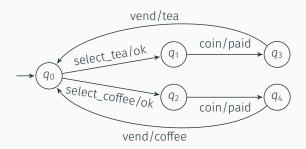
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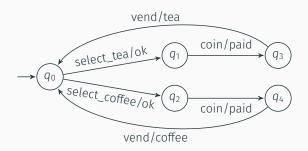
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- Transition x/y represents giving input x and getting output y, e.g.
 - · inputs select_tea, coin, vend, gives us outputs ok, paid, tea
 - Machine follows path $q_0 \rightarrow q_1 \rightarrow q_3 \rightarrow q_0$

5

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- There are extra states; can only happen if there are also state transfer faults

Properties of FSMs

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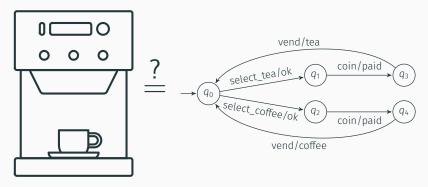
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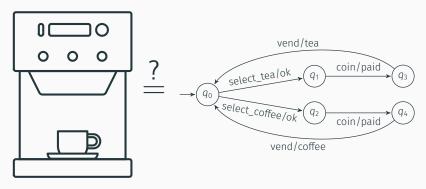
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- An FSM is **strongly connected** if for each pair of states (s_i, s_j) there exists an input sequence that takes the FSM from s_i to s_j

Testing from an FSM



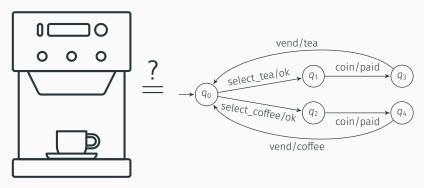
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Testing from an FSM



- · Assume the software behaves like an FSM model
- · Submit inputs to the FSM and software in parallel

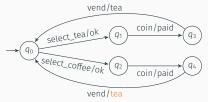
Testing from an FSM



- · Assume the software behaves like an FSM model
- · Submit inputs to the FSM and software in parallel
- Observe and compare the outputs

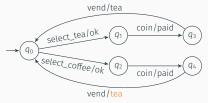
Example Faults for Drinks Machine

Output faults: A transition produces the wrong output (tea)



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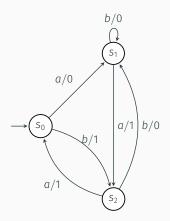
State transfer faults: A transition goes to the wrong state (q_1)



The Transition Tour Method

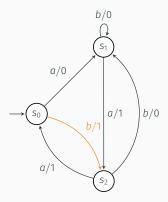
- Given an FSM M, the transition tour method involves:
 - Finding a path (sequence of transitions) ρ from the initial state of M that includes all transitions of M.
 - The test sequence is the label of ρ : the corresponding input/output sequence.
- The transition tour method is guaranteed to find output faults as long as there are no state transfer faults.

Consider a simple example

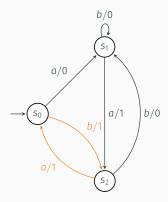


There is more than one possible transition tour

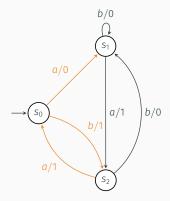
We could start with transition $(s_0, s_2, b/1)$.



Then follow $(s_0, s_2, b/1)$ with $(s_2, s_0, a/1)$.

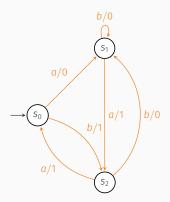


Now maybe follow $(s_0, s_1, a/0)$, giving path $(s_0, s_2, b/1)(s_2, s_0, a/1)(s_0, s_1, a/0)$.



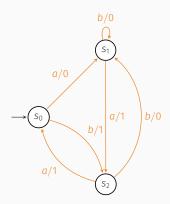
Completing this, we could choose:

- $\cdot (s_0, s_2, b/1)(s_2, s_0, a/1)(s_0, s_1, a/0)$ followed by
- $(s_1, s_1, b/0)(s_1, s_2, a/1)(s_2, s_1, b/0)$



This gives us the following test sequence: b/1, a/1, a/0, b/0, a/1, b/0.

- In testing we apply input sequence baabab and expect to observe output sequence 110010
- The test sequence can also be represented by baabab/110010.

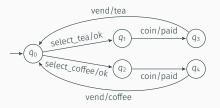


Transition Tours: Generating a Transition Tour

- · We can apply a simple heuristic such as:
 - In the current state *s*, if there is a transition *t* from *s* that has not yet been included then add *t* to the current path and update the current state.
 - Otherwise, follow the shortest path from s that moves M to a state with at least one uncovered transition.
- Alternatively, we can use graph algorithms (we are looking for a path that includes all edges).
 - These can return an optimal (shortest) transition tour in polynomial time.

Transition Tour for Drinks Machine

Assume no state transfer faults, then we can test by just executing every transition



The input sequence select_tea, coin, vend, select_coffee, coin, vend will do that for us.

We validate that the output sequence is ok, paid, tea, ok, paid, coffee.

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- · To find state transfer faults we need to be able to check states
- In black-box testing, this requires finding appropriate input sequences
- We might follow each transition by sequences that distinguish between possible states

To test from an FSM, we want to check every transition $(q_i, q_j, x/y)$

• Get the FSM to state q_i

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- Do we get output *y*?

To test from an FSM, we want to check every transition $(q_i, q_j, x/y)$

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- Do we end up in state q_i ?

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Challenges

To test from an FSM, we want to check every transition $(q_i, q_j, x/y)$

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Controllability: How do we get the FSM to q_i ?

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Challenges

Controllability: How do we get the FSM to q_i ?

Observability: How do we know the FSM is in q_j ?

Controllability

Find a sequence that gets the *specification* to the desired state.

Observability

Characterise states in terms of the I/O actions they can perform:

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Distinguishing sequences

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Observability

Characterise states in terms of the I/O actions they can perform:

- · Distinguishing sequences
- Unique I/O sequences (UIOs)
- · Characterising set

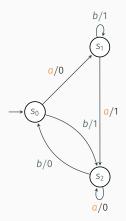
Distinguishing States

Separating two states:

- Two states s and s' of FSM M are separated by input sequence x if: the response of M to x is different in states s and s' $(\lambda^*(s,x) \neq \lambda^*(s',x))$
- If there is such an input sequence x then s and s' are said to be separable.
- States s and s' are said to be equivalent if they are not separable.

Distinguishing States: Example 1

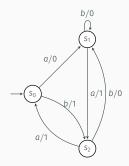
In the following FSM, input a separates states s_0 and s_1 , but does not separate states s_0 and s_2 .



Distinguishing States: Example 2

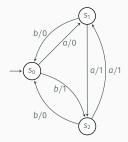
Inputs sequences of length greater than 1 are sometimes needed.

In the following FSM, no input of length 1 can separate states s_1 and s_2 , but aa does $(\lambda^*(s_1, aa) = 11, \lambda^*(s_2, aa) = 10)$



Distinguishing States: Example of Equivalence

In the following FSM, no input can separate states s_1 and s_2 , therefore they are *equivalent*.



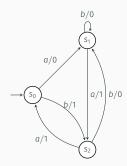
Distinguishing Sequences

A distinguishing sequence *D* is an input sequence that produces a different output **for each state**.

- For every pair of states s and s' of FSM M such that $s \neq s'$, we have that $\lambda^*(s,D) \neq \lambda^*(s',D)$)
- This means that the output produced in response to *D* identifies the state of *M*.

Distinguishing Sequences: Example

- For the example FSM below, aa forms a Distinguishing Sequence since:
 - From state s_0 the output sequence is 01
 - From state s_1 the output sequence is 11
 - From state s_2 the output sequence is 10



Distinguishing Sequences for Drinks Machine

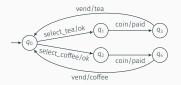
It is possible for an FSM to have multiple distinguishing sequences, but not every FSM has one! Does the drinks machine have one?

Distinguishing Sequences for Drinks Machine

It is possible for an FSM to have multiple distinguishing sequences, but not every FSM has one! Does the drinks machine have one?

Yes! (assuming we know when an input has been refused)

[select_tea, coin, vend]



- From q_0 we get ok, paid, tea
- From q_1 we get refuse, paid, tea
- From q_2 we get refuse, paid, coffee
- From q_3 we get refuse, refuse, tea
- From q₄ we get refuse, refuse, coffee

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- Note: Distinguishing Sequences identify all of the states but a UIO might only identify *one* state.
- · Not all FSMs have these either!

"Brute-force" Approach: Systematically try all possible input sequences of increasing length until a unique input output sequence is found for each state.

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 - Observe output sequences for each state: is the output sequence for any state **unique** wrt *all* other states?

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"Brute-force" Approach: Systematically try all possible input sequences of increasing length until a unique input output sequence is found for each state.

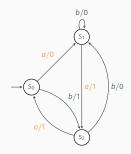
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Easy to understand and implement, but...

- · Computationally expensive for large FSMs
- Finding Unique I/O Sequences is not guaranteed

Unique I/O Sequences (UIOs): Example

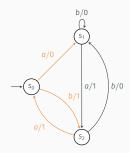
- In the example, a/0 forms a UIO for state s_0 :
 - From state s_0 the output sequence is 0
 - From state s_1 the output sequence is 1
 - From state s_2 the output sequence is 1
- Note that a is **not** a Distinguishing Sequence, as it cannot separate s₁ and s₂.



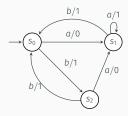
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Using UIOs to test transitions...

- In order to test the transition $t = (s_2, s_0, a/1)$ we can build a test sequence as follows:
 - A preamble b/1 that reaches the initial state of t (s_2);
 - The input/output pair a/1 of the transition t.
 - Finally, the chosen UIO for the **end state** of the transition (a/0).
- This gives the test sequence b/1, a/1, a/0.



Unique I/O Sequences (UIOs): Another Example



Following the brute-force algorithm (building table from left to right):

State	a	b	aa	ab	ba	bb	aaa	
S_0	0	1	01	01	10	11	011 111 011	
S ₁	1	1	11	11	10	11	111	
S_2	0	1	01	01	10	11	011	

- In the first iteration, we already identify 'a' as a UIOs for state s₁, because 'a' distinguishes it from all other states
- \cdot Up to length 2, we cannot find UIOs for states s_0 and s_2

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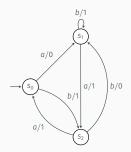
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- There are polynomial time algorithms to generate W sets
- We can minimise every FSM

Characterising Sets: Usage

- If we know the output triggered by each input sequence from *W*, then we can identify the state.
- To check transition $t = (s_i, s_j, x/y)$ we can separately follow t by each element of W.
- Thus, using a characterising set leads to multiple tests for a transition.

Characterising Sets: Example



For the above FSM, $\{a, b\}$ is a characterising set since for every pair of states, there is an element in the set that distinguishes them:

State	Response to a	Response to b
S ₀	0	1
S ₁	1	1
S_2	1	0

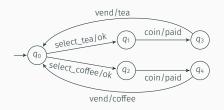
Characterising Sets: Implications

- For this example, if we are checking the final state of a transition *t* we separately follow it by *a* and *b*.
- · So, we use two tests for a transition.
- If the response to a after t is 1 and the response to b after t is 0 the transition must have taken the implementation to a state corresponding to s_2 .

Characterising Set for Drinks Machine

Again, assuming we know when an input has been refused (e.g., a loop in each state that outputs "refused"):

 $W = \{[select_tea, coin, vend]\}$



State	Response to [select_tea, coin, vend]
90	ok, paid, tea
91	refused, paid, tea
q_2	refused, paid, coffee
q ₃	refused, refused, tea
Q ₄	refused, refused, coffee

The *W* method produces a set of input sequences to test correctness, assuming:

• Implementation behaves like some unknown FSM with no more than *n* states.

¹Note: Many real systems have a reset and sometimes this simply means switching the system off and then on again, but it may be a more complex operation.

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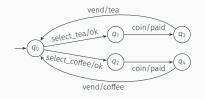
More generally, for n+m states, we get $VW \cup VXW \cup ... \cup VX^mW$

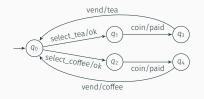
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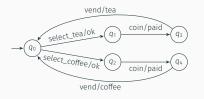
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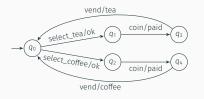
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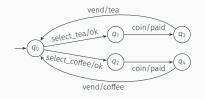
Make sure you reset before each sequence!

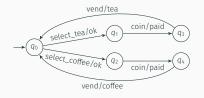


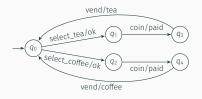


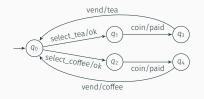


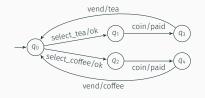


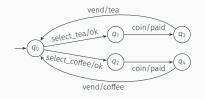


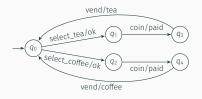


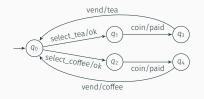


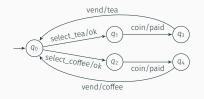


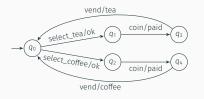


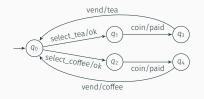


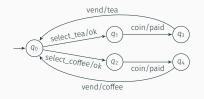


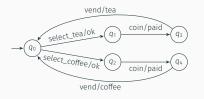


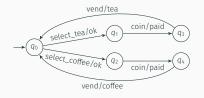


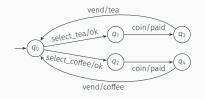


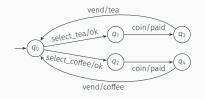


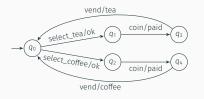


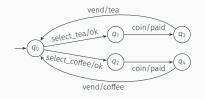


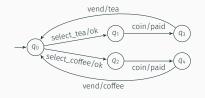


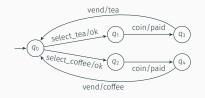


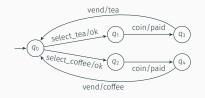




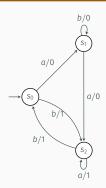








A Smaller Example



$$V = \{\epsilon, a, b\}, X = \{a, b\}, \text{ and } W = \{a, b\}$$

$$VW = \{\epsilon, a, b\}\{a, b\} = \{a, b, aa, ab, ba, bb\}$$

$$VXW = \{\epsilon, a, b\}\{a, b\}\{a, b\}$$

$$= \{aa, ab, ba, bb, aaa, aab, aba, abb, baa, bab, bba, bbb\}$$

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 - · Model inference!
- · What if we can't reliably reset?
 - · Use transfer

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- In these cases, we need to apply black-box testing techniques
- · Model-based testing is one such technique
- We can test that the system matches an FSM specification using the *W* method.
 - The W method is guaranteed to find a fault if the implementation is faulty and satisfies the assumption (at most one extra state).