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Digital Piano

Introduction

The project is about building a digital piano having different octaves via VHDL and implementing it on BASYS3 FPGA board.

Methodology

By changing the clock timers, the different octaves will be generated. Then, by using different clock timers and signal wave formations such as sinusoidal, triangular waves different sound options may be added.

External Components

BASYS3 FPGA board

Amplifier (since sound generated by BASYS3 will be low) (TRC-11 amplifier from the EEE-211 project would be candidate for that mission.)

Speaker

Project Presentation

Progress Demo: The main part of the project which is building the digital piano will be completed and presented. Additionally, the performed note will be displayed through 7-segment display or leds.

Final Demo: The different octaves will be added. Optionally, I may add different sound options and the project will be finalised. If the adding different sound options is succeeded the used different sound option will be displayed through leds or 7-segment display.