

Check for right locations first

(mark as seen) delete letters that match from guess & answer

{ Check wrong locations next

delete letter that exists in both

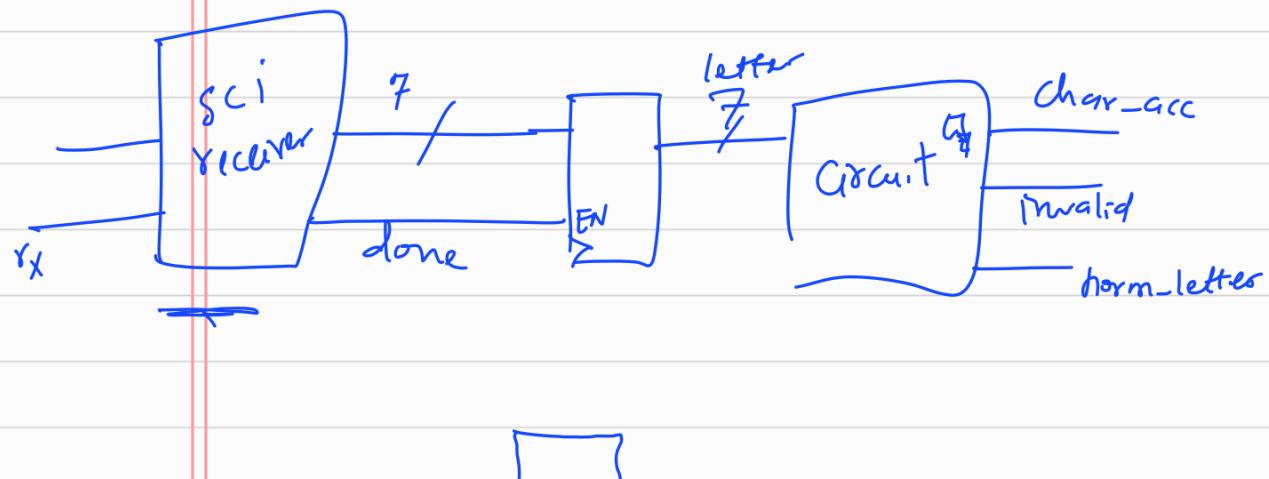
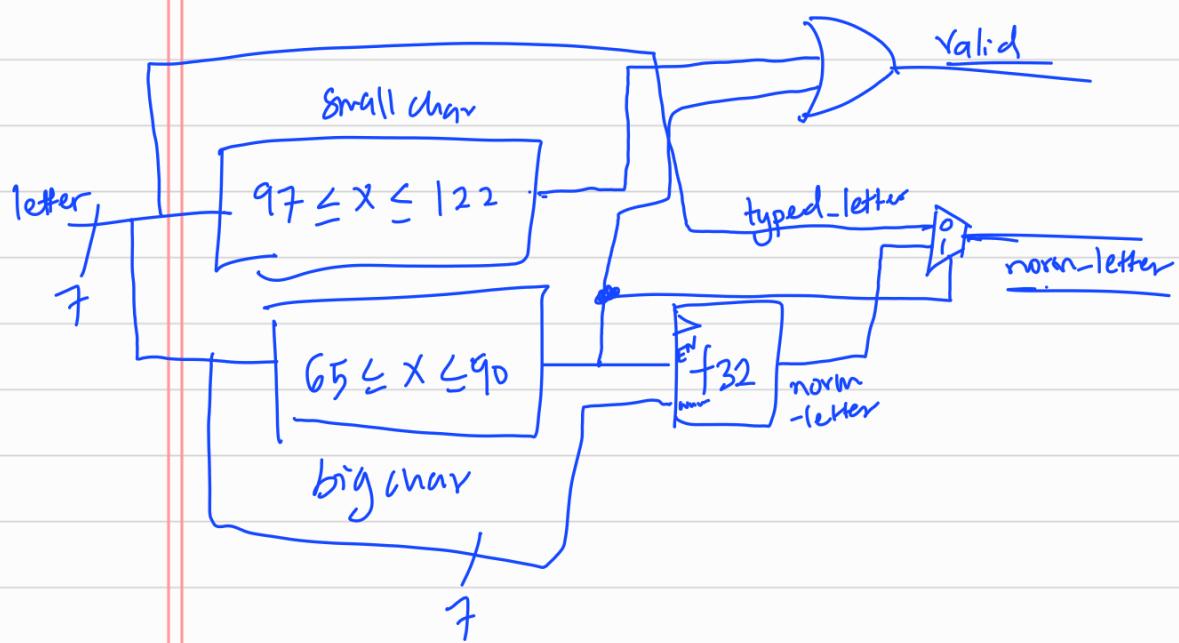
loop till end of either word.

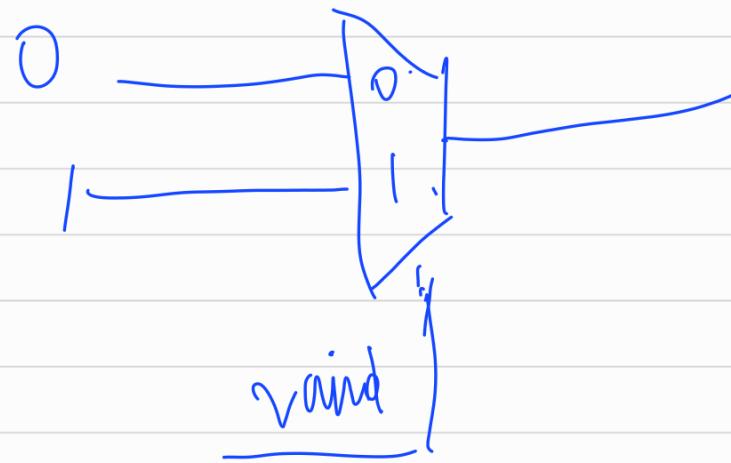
QK

$(65 \rightarrow 90)$ C

If its small char $(97 \rightarrow 122)$
then valid

If within $65 \rightarrow 90$ big char
then add 32
return valid





Steps:

Rx
Tx , wiring
Rx talks to Tx

basic Word logic

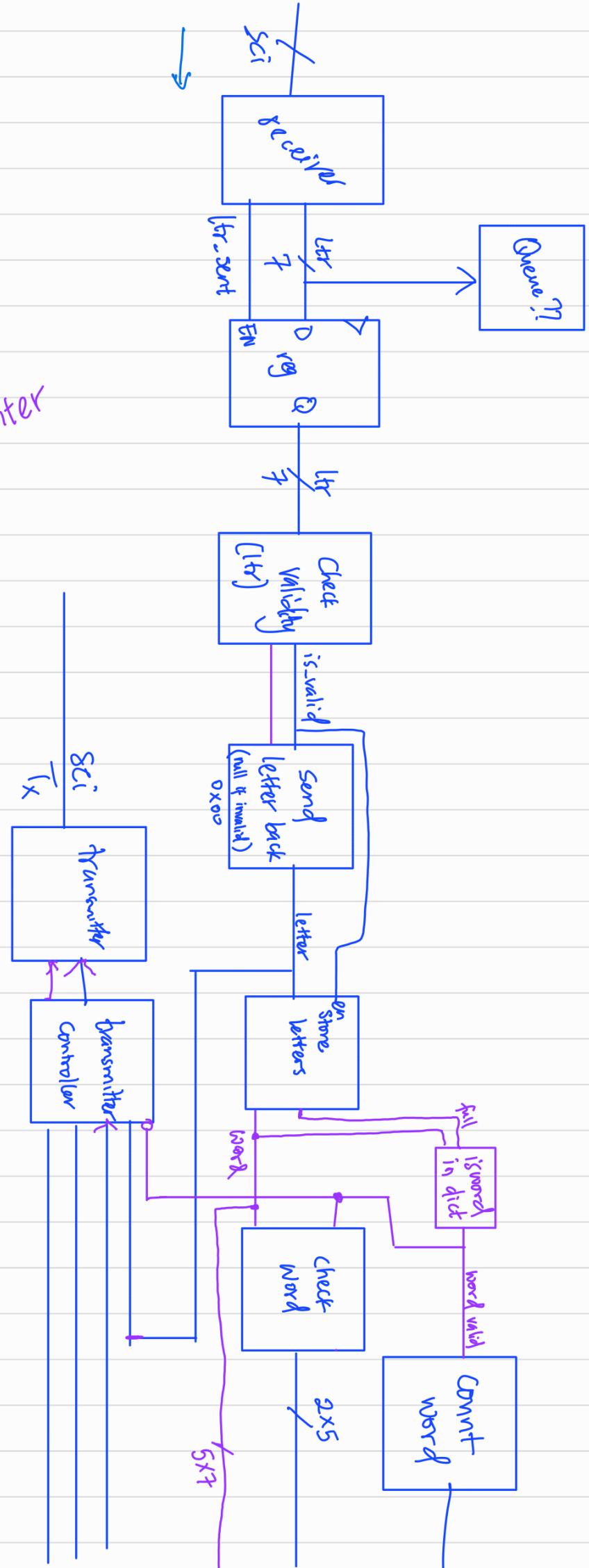
$Rx \rightarrow \text{word logic} \rightarrow Tx$

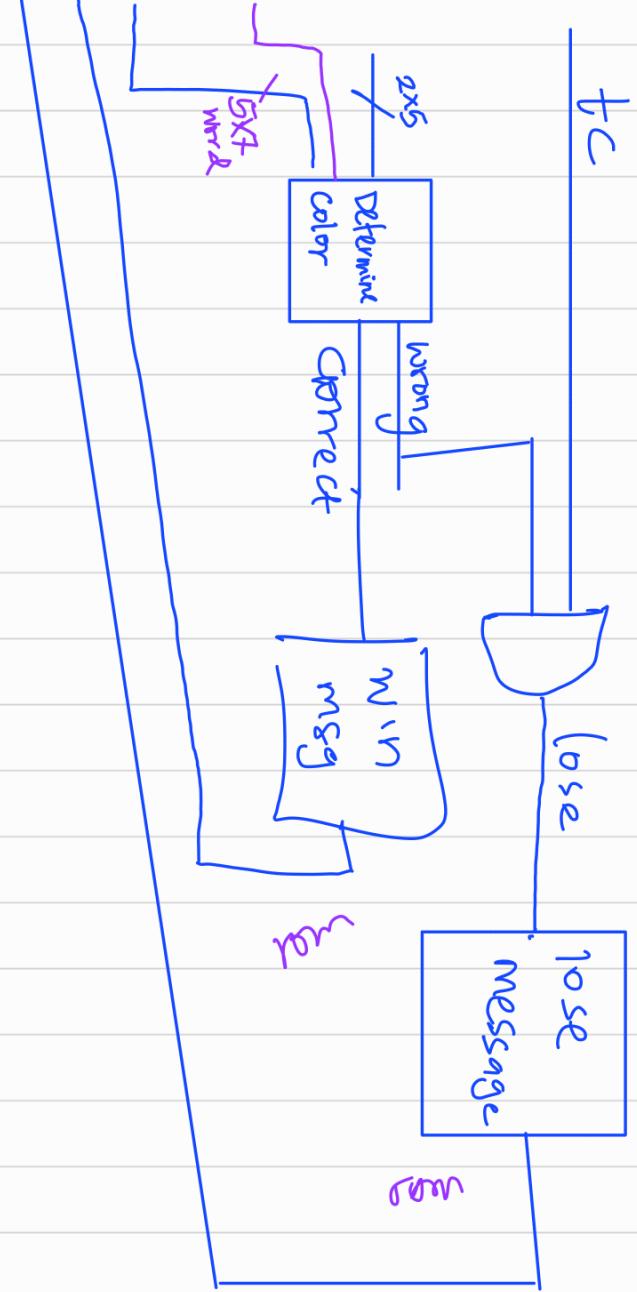
ROM

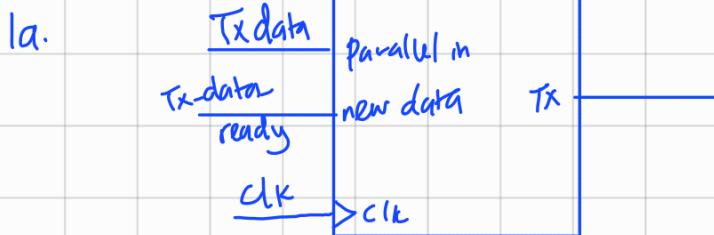
$Rx \rightarrow \text{word logic} \rightarrow \text{rom} \rightarrow Tx$

wait 2 cycles
 before reading
 account for back space
 don't validate until enter

from word to word



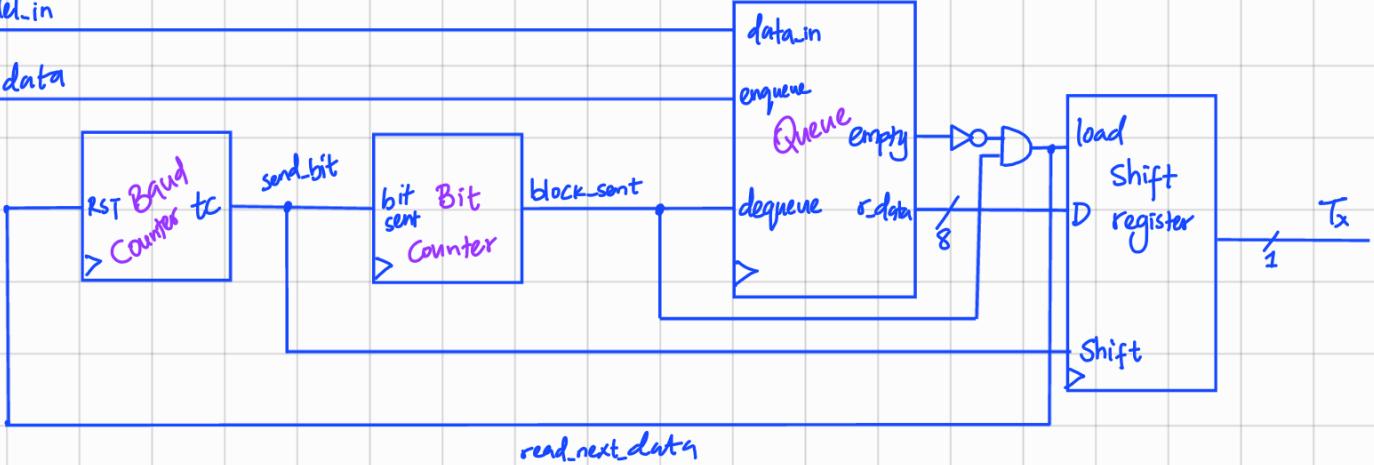




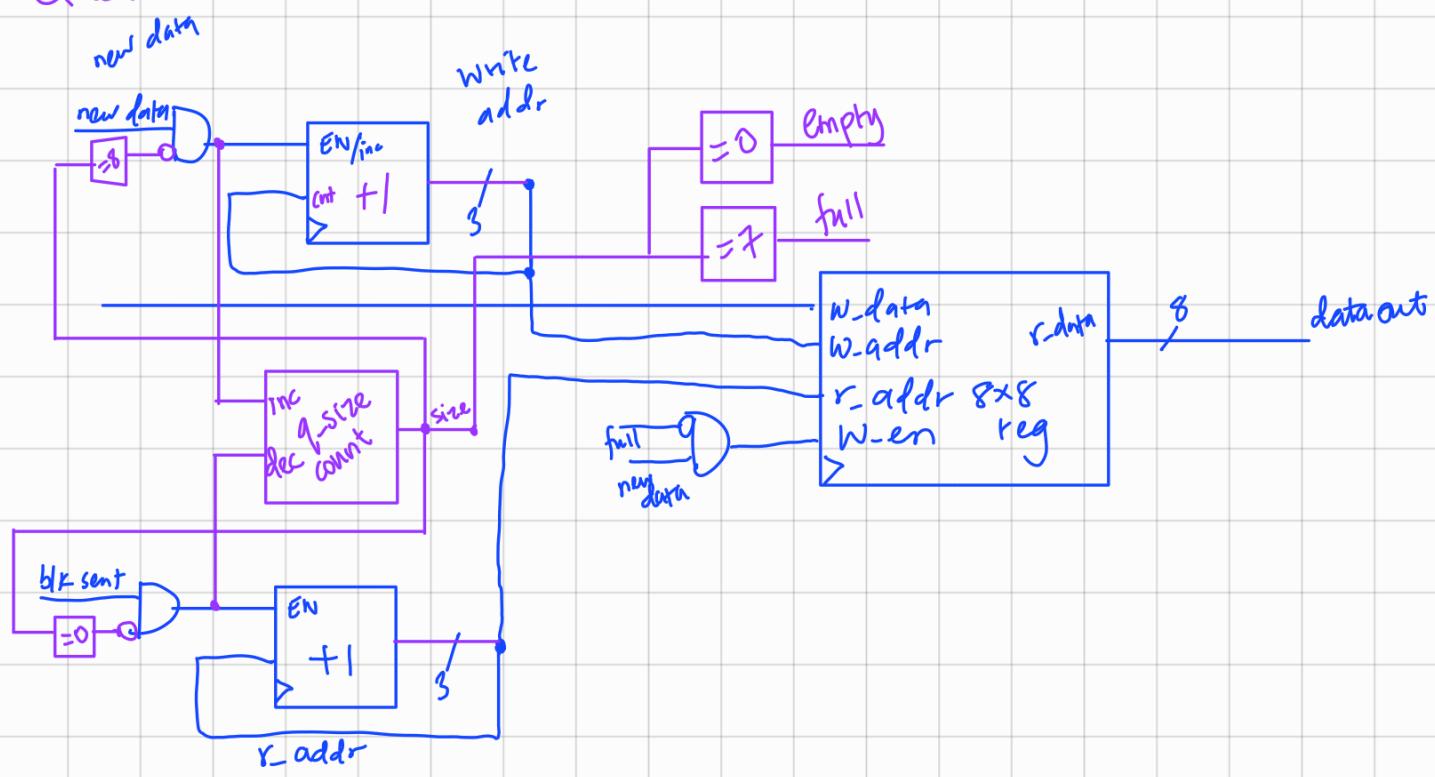
Transmitter

Parallel_in

new_data

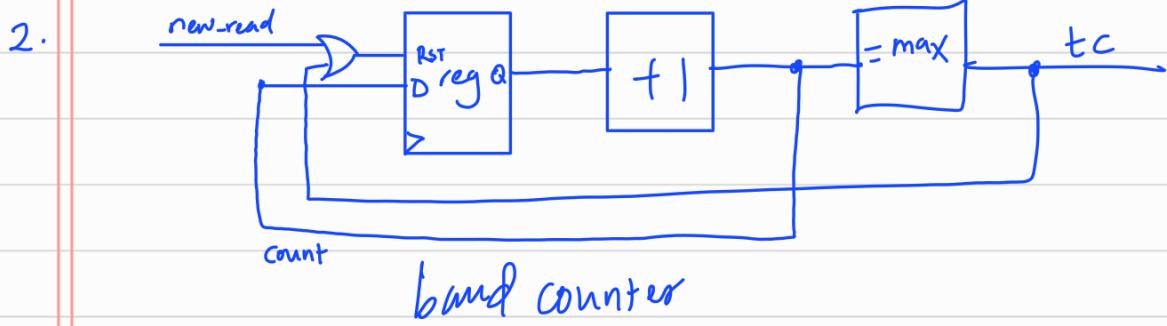


Queue



Bit Counter

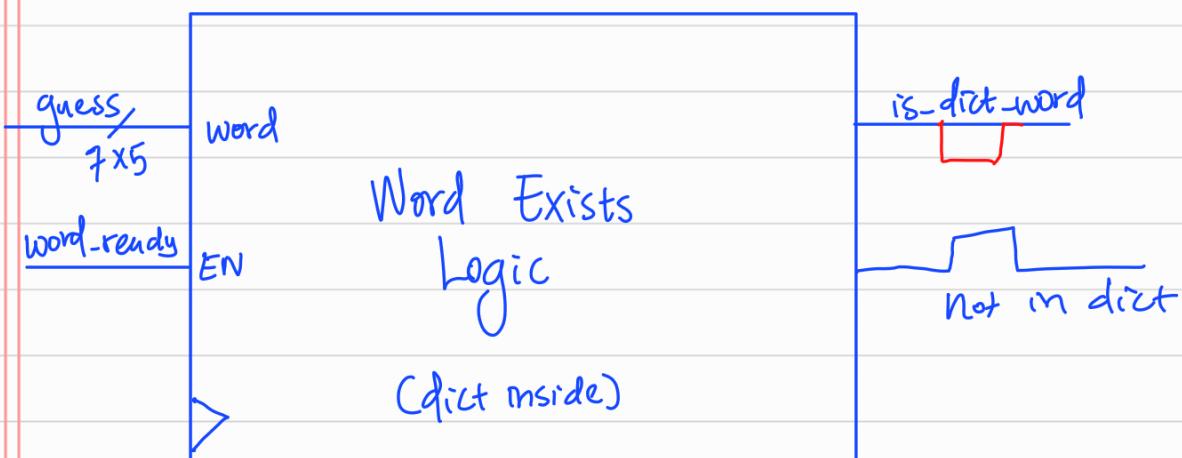
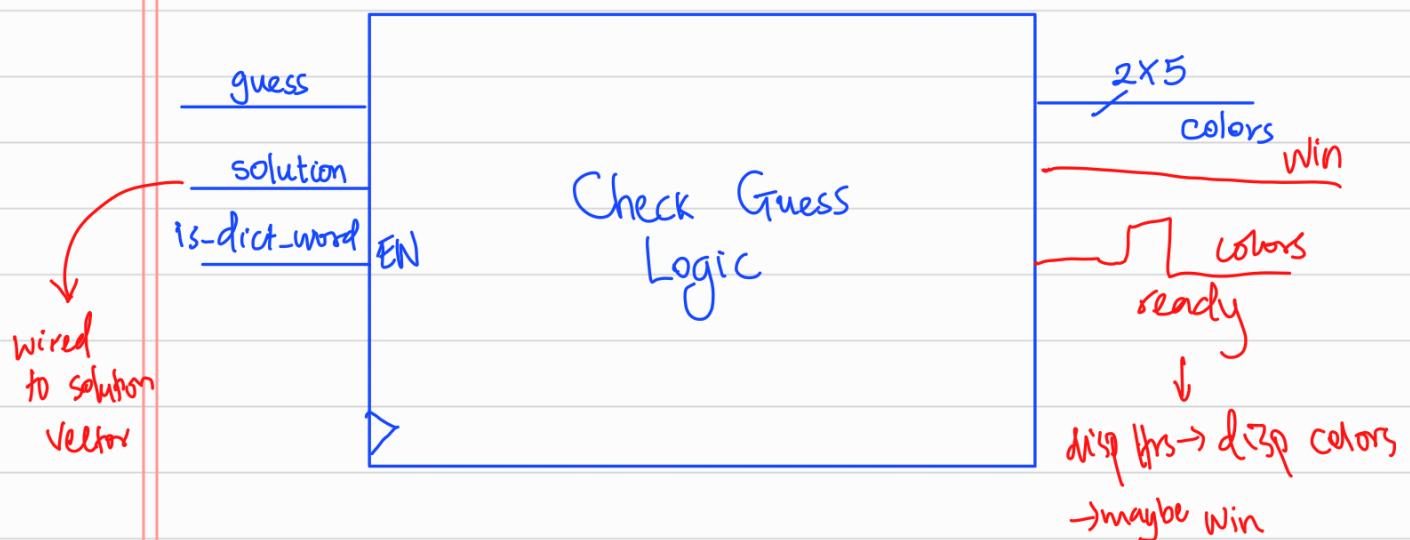
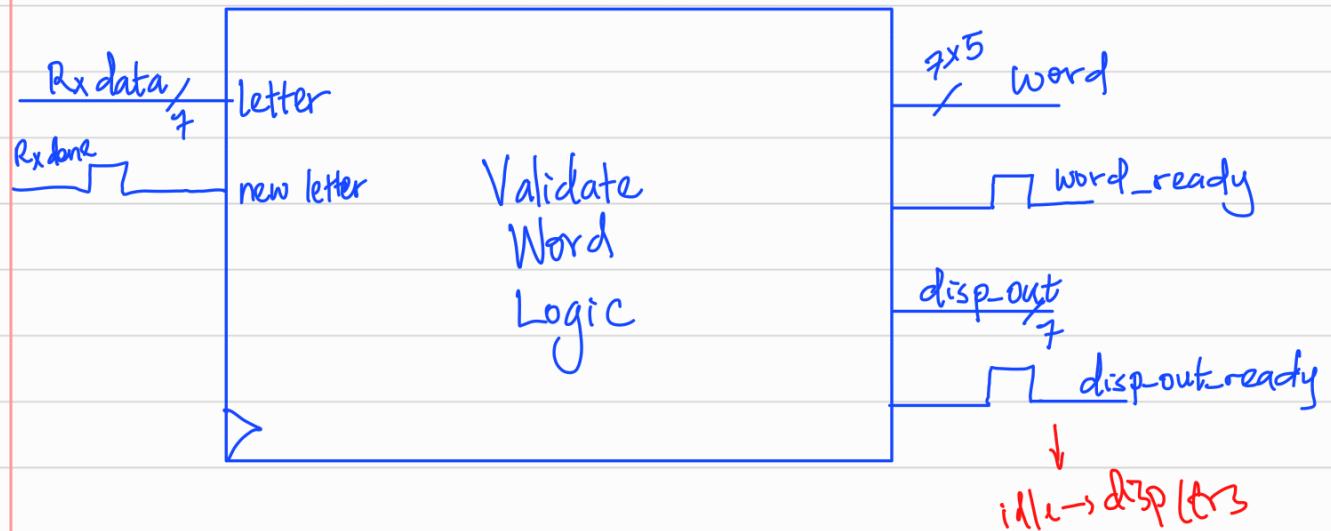


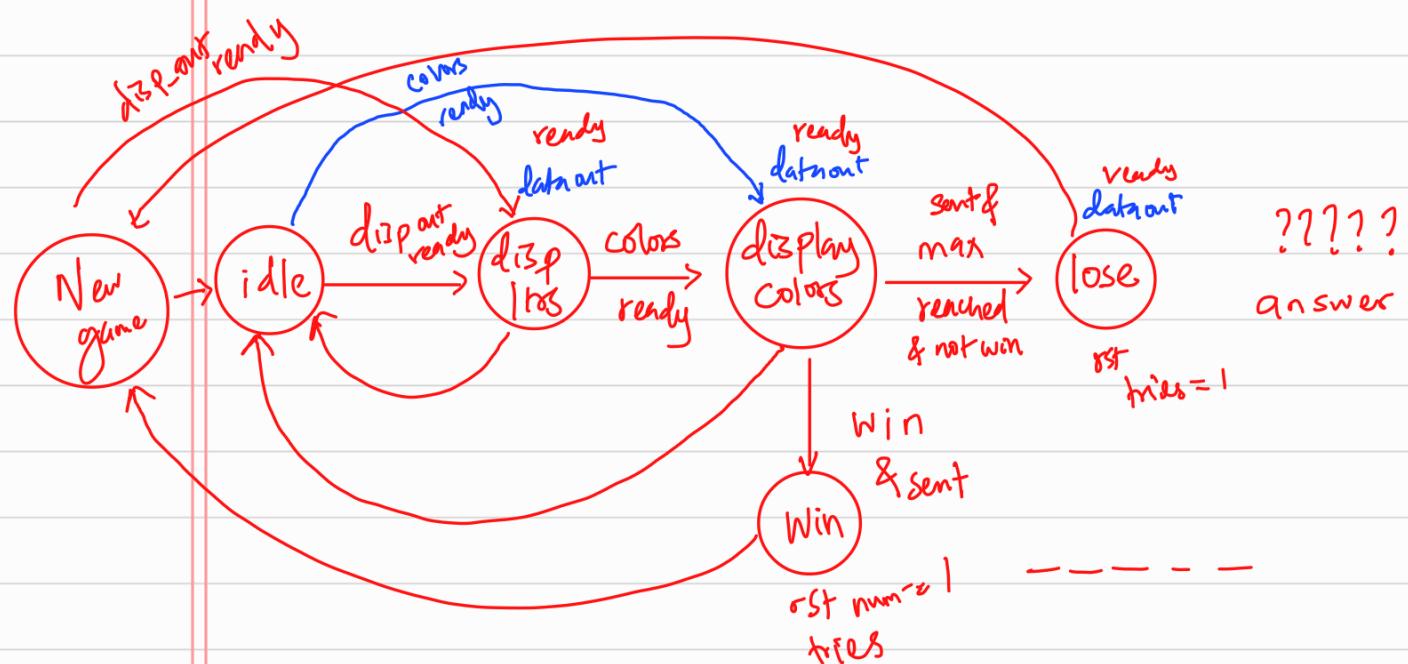
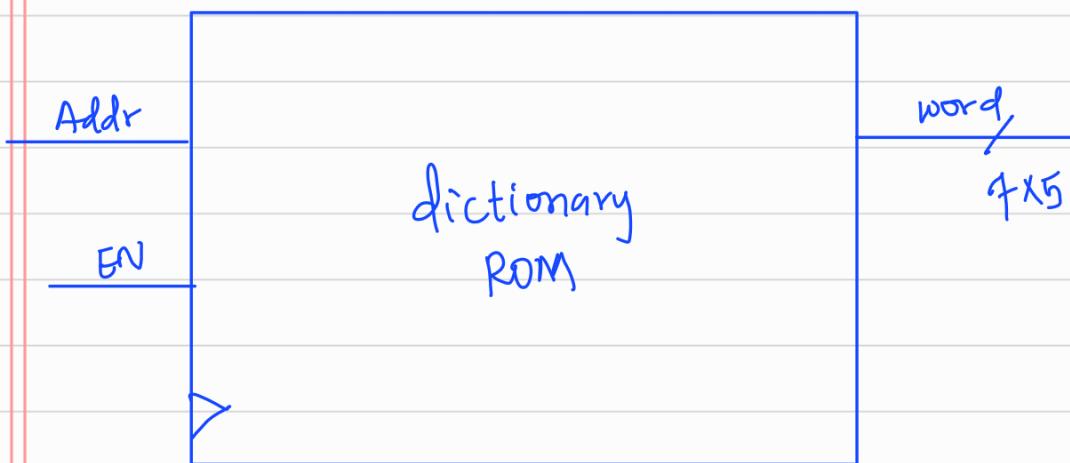
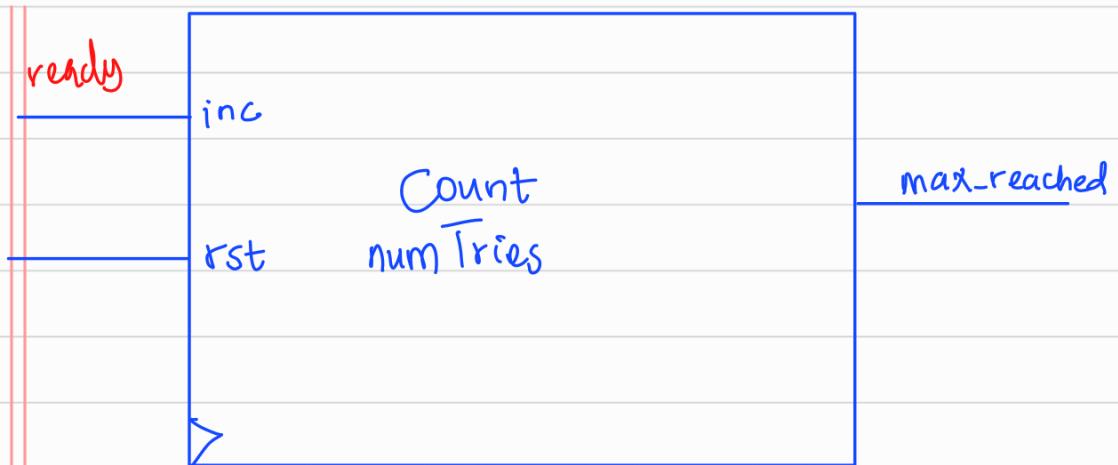


<https://www.edaplayground.com/x/9bFb>

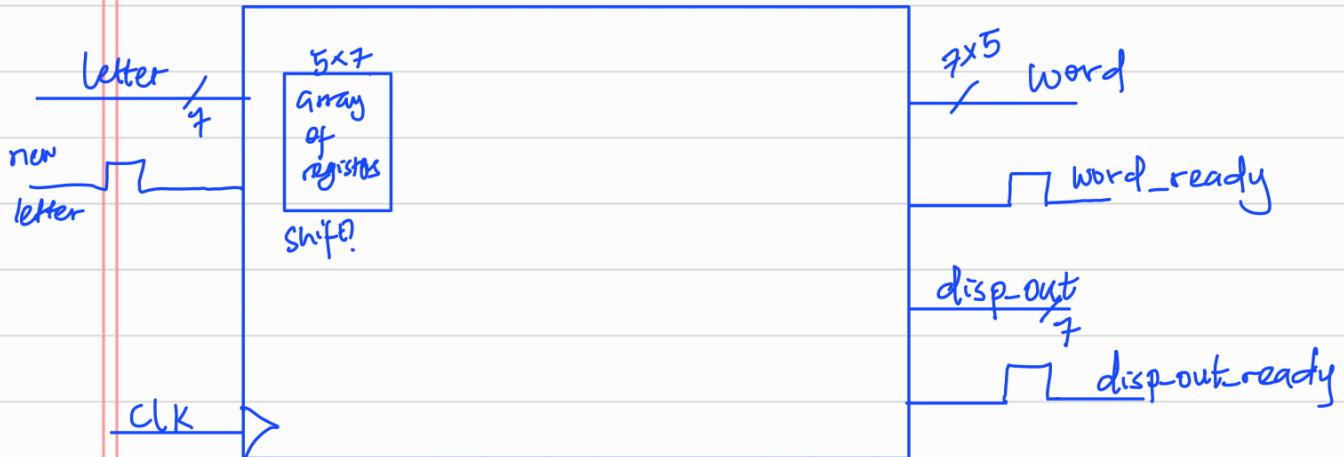
inputs
what is typed
backspace?
enter
letter is accepted
store the word

Determines
is a letter, so store



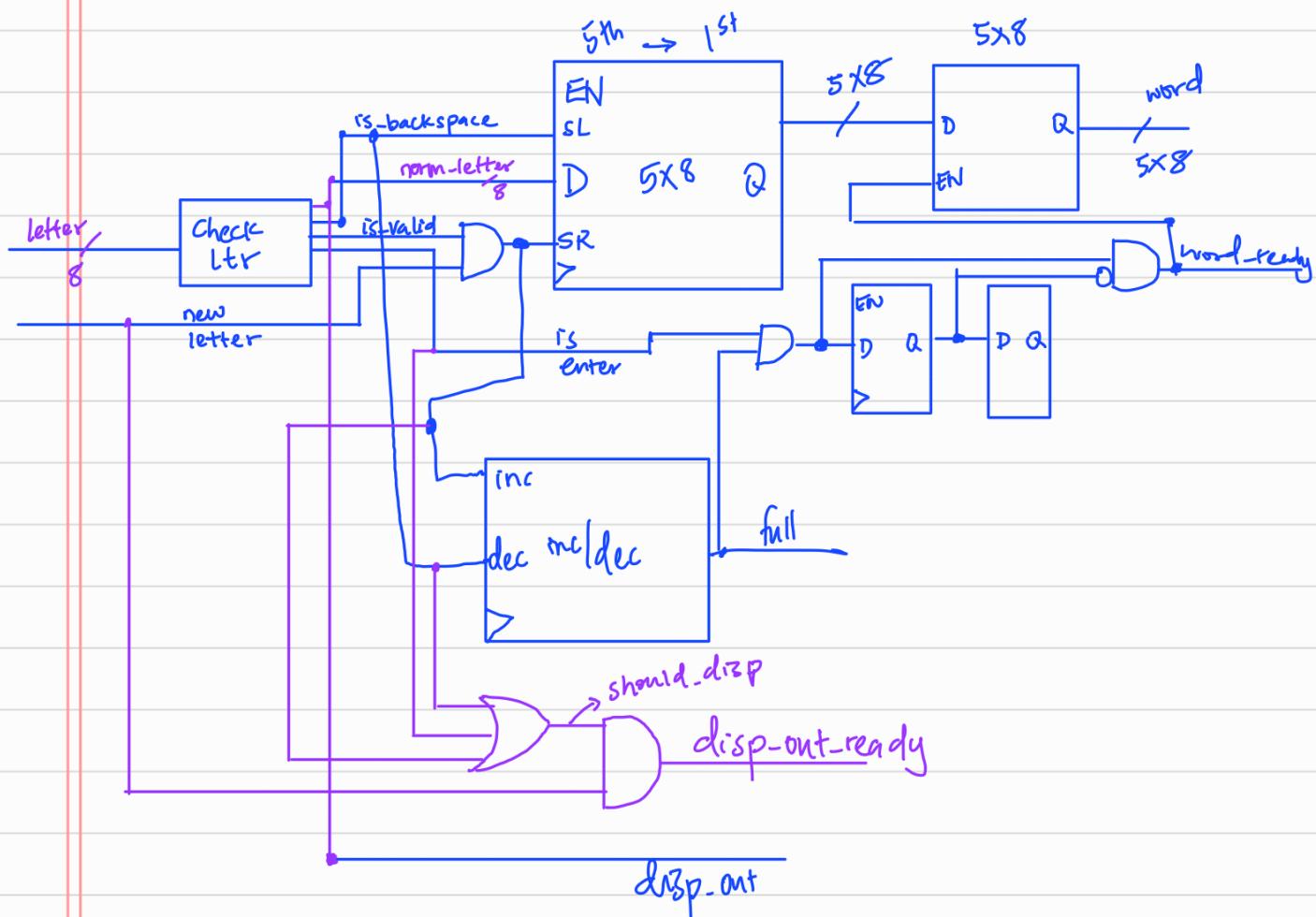


Validate word logic

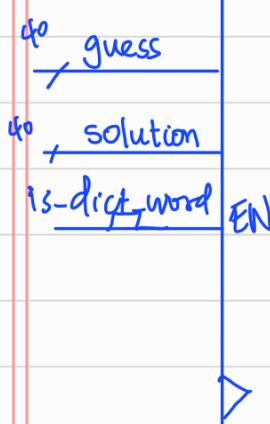


e⁸ word = a p p l e

e l p p a



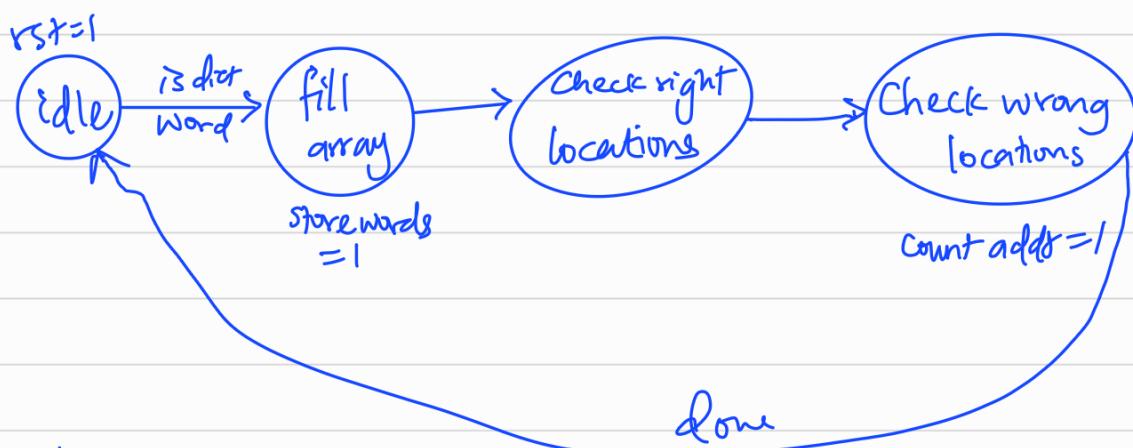
Check Guess logic



Check Guess Logic

2x5	colors
[]	ready
00	→ WLWP WLWP
10	→ RLWP or CLWP
11	→ RL RP CLCP
01	→ RL RP CLCP

letter, place



colors

L P

CL	CP	blk	yellow	green
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	0	1

blk: \overline{LP}

yellow: \overline{LP}

green: P

5 bytes
40 bits

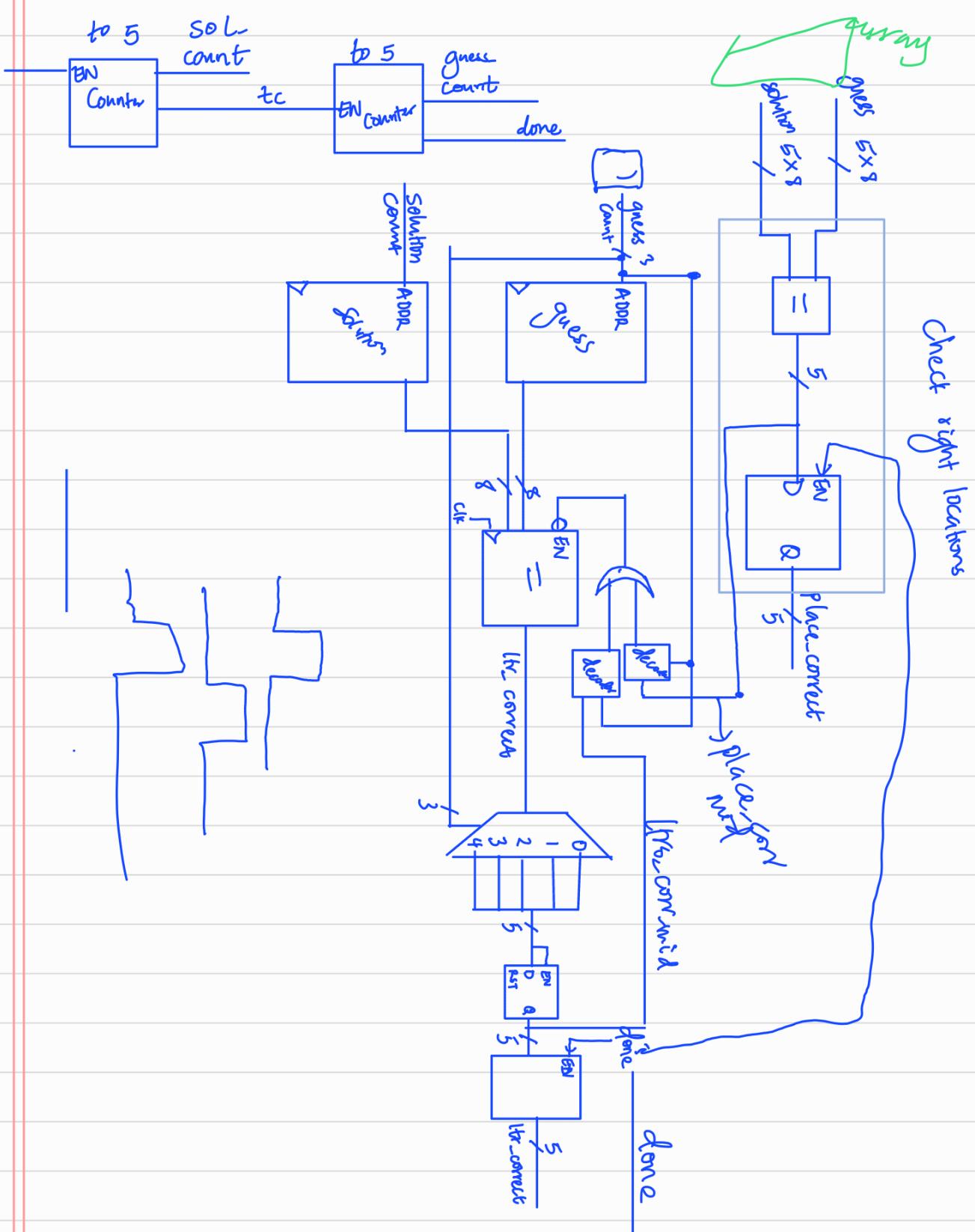
bytes

(wordloc_Xbyte size + 7)

clr_hk : 5 bits
clr_plc : 5 bits

0 → 7

8 → 15



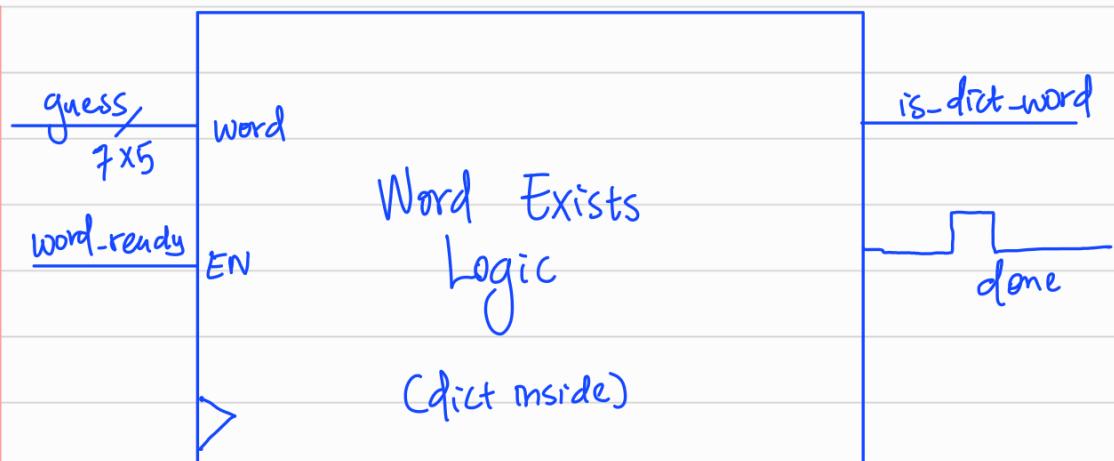
a	p	p	l	e	x	t	
10	00	00	00	10	h	e	d
CP	D	0	0	0	e	e	s
CL	1	0	0	0	00	00	d
					11/01	00	s

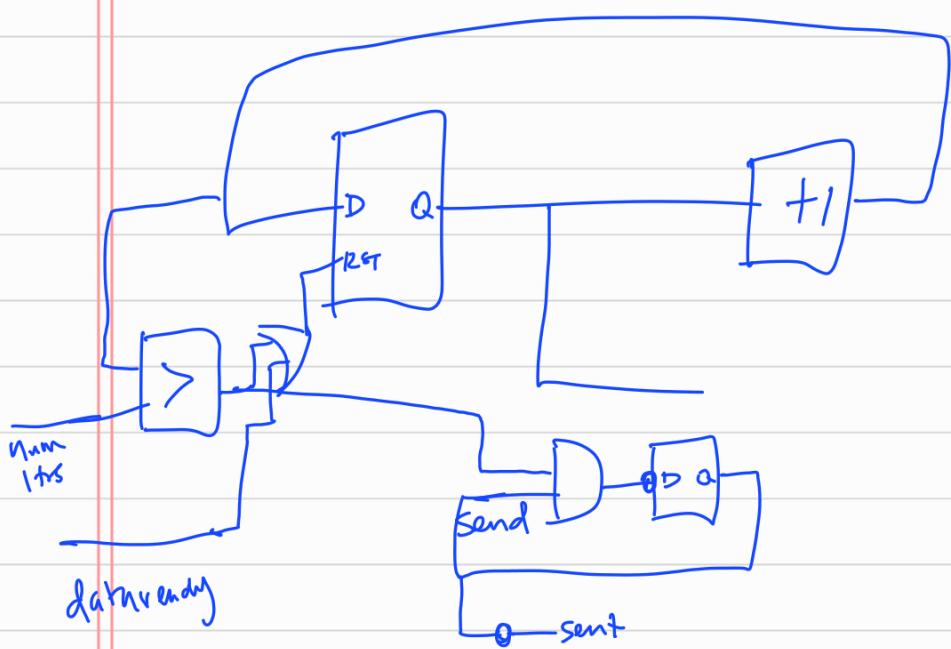
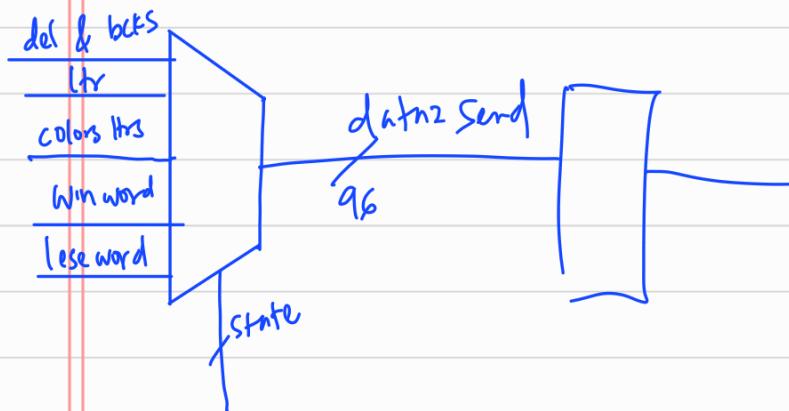
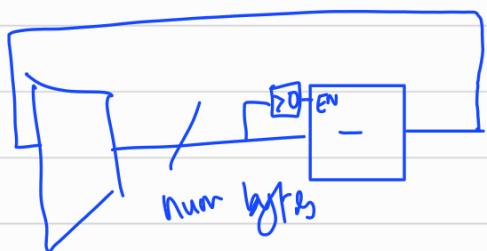
g	g	x	t	e
11/01	11/01	10	10	10
CP	1	1	0	0
CL	0/1	0/1	1	1

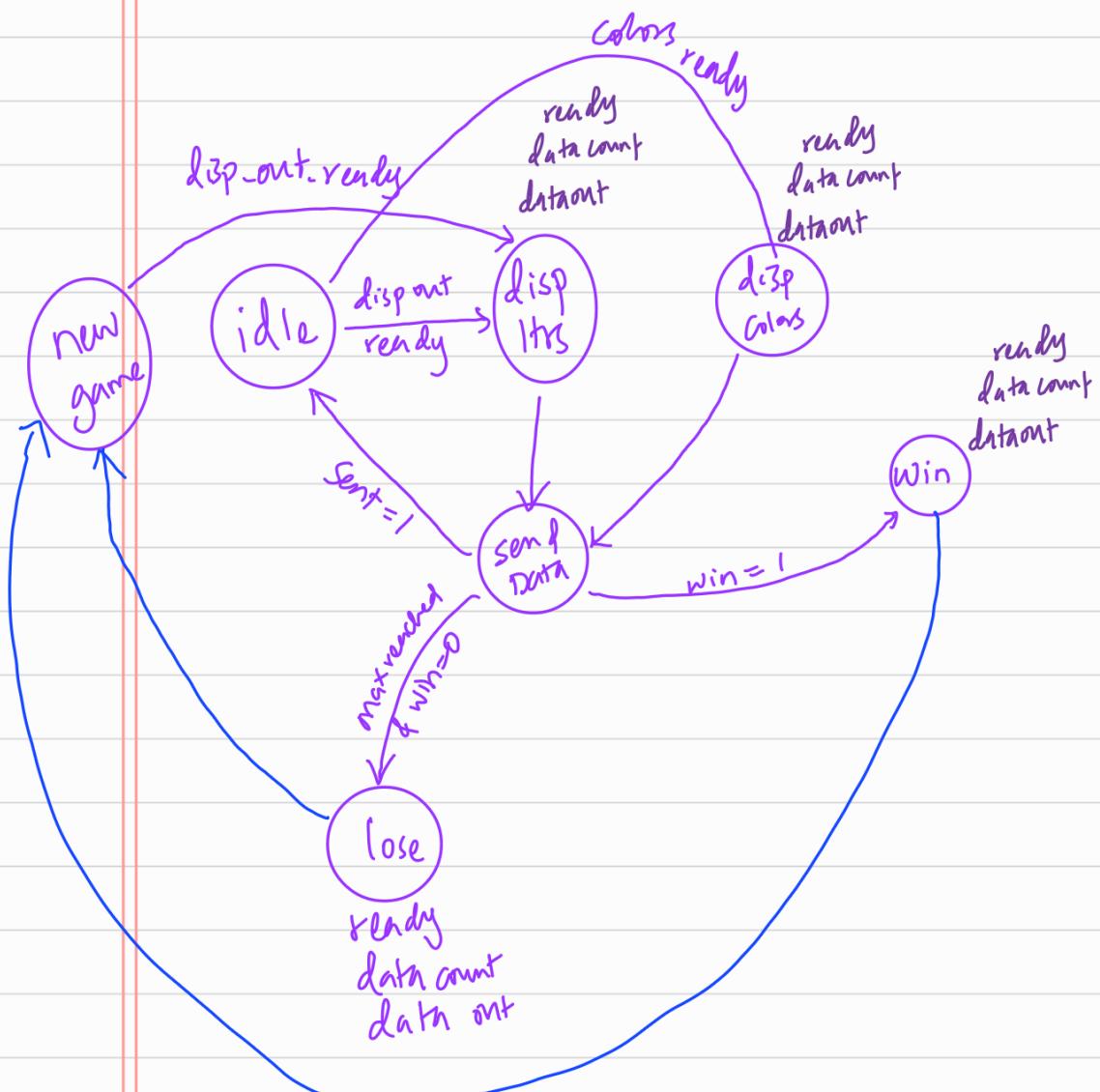
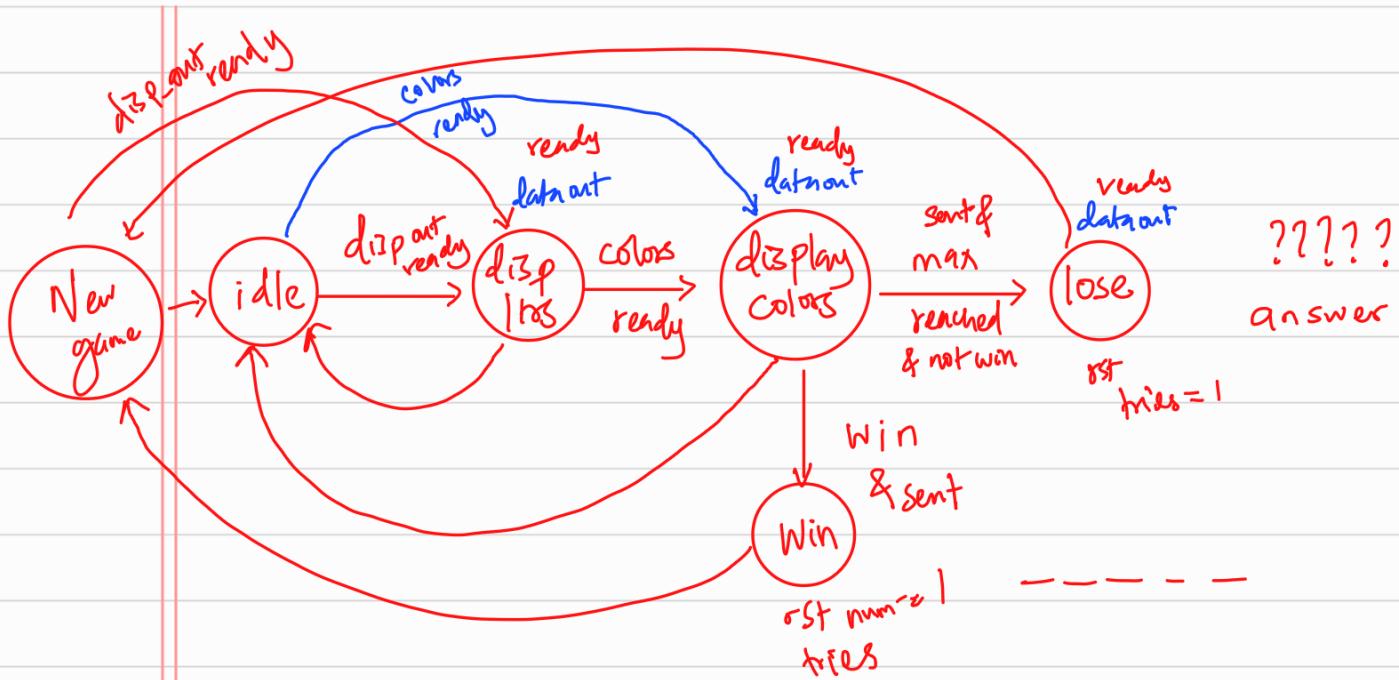
1 → 2

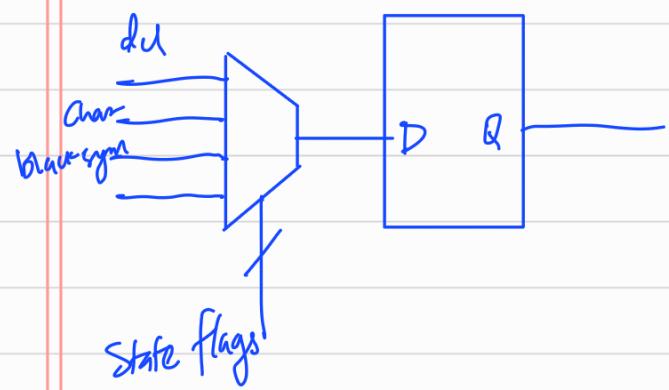
e vs e

ques - ltr correct (g_idx)
sol - ltr correct (s_idx)









new ltr	full	β_{alpha} / d letter	enter	$\beta_{\text{backspace}}$	readyout
/	0 0	0 0	0 0	0 1	0 1
/	0 0	0 0	1 1	0 1	0 1
/	0 0	1 1	0 0	0 1	1 1
/	0 0	1 1	0 1	1 0	1 1
/	0 0	1 1	1 1	0 1	1 1
/	1 1	0 0	0 0	0 1	0 1
/	1 1	0 0	0 1	1 0	1 1
/	1 1	0 0	1 1	0 1	1 1
/	1 1	1 1	0 0	0 1	0 1
/	1 1	1 1	0 1	1 0	1 1
/	1 1	1 1	1 1	1 1	1 1

EB

	00	01	11	10
00	0			0
01				
11	0			
10	0			

FV

new ltr

& not $(\overline{FEB} + \overline{FVB})$

