New XOR/XNOR and Full Adder Circuit for Low Voltage and Power Applications

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Abstract

In this paper, a new full adder circuit was developed by an assistance report paper from Hanho Lee and Gerald E. Sobelman. It is an essential point to have low voltage operation as the dynamic power dissipation is proportional to $V^2_{dd.}$ The new designed full adder has low power dissipation.

Keywords—Full adder circuits; XNOR, XOR.

1. INTRODUCTION

This paper explains a circuit design idea for a low power and low voltage full adder circuitry. XOR and XNOR circuits are fundamental parts of full adder circuits. A disadvantage of the circuit is a low power dissipation at a low supply voltage. Another primary design limitation is power dissipations. Low power solutions are stepping-stones for the successful implementations of circuits. Decreased power dissipation is essential in the development circuit of mine. It is a critical issue to control power dissipation because of the equation that consists of the square term in the power dissipation. Moreover, glitches consume a great amount of power. Therefore, it is possible to reach low power levels by decreasing glitches in the circuit. The circuit is designed by using the transmission gate theory [1]. It is crystal clear that an NMOS transistor allows the '0' signal totally, however, it does have poor performance on '1' signal transmission. In contrast with NMOS, a PMOS transistor can transmit a '1' signal completely as long as a '0' signal is reduced in the threshold voltage of PMOS. In this report, the simulation results and analysis of the full adder circuit is completed and explained. This report is organized as follows. In Section 2, the operation principle of the circuit is reviewed. Section 3 explains the proposed XOR and XNOR circuits. The simulation results are discussed in Section 4. The results are summarized in Section 5.

A	B	A XOR B	A XNOR B
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Table 1. The truth table of XOR and XNOR

2. OPERATION PRINCIPLE OF THE CIRCUIT

Full Adder is a digital system that capable of adding 2 digital n-bit binary numbers, n may change according to circuit implementation. It performs addition operations on 3 one-bit binary numbers. Thus, it produces the sum of three inputs and carry value.

$$S = (A \oplus B) \oplus C_{in}$$
$$C_{out} = (A \cdot B) + (C_{in} \cdot (A \oplus B))$$

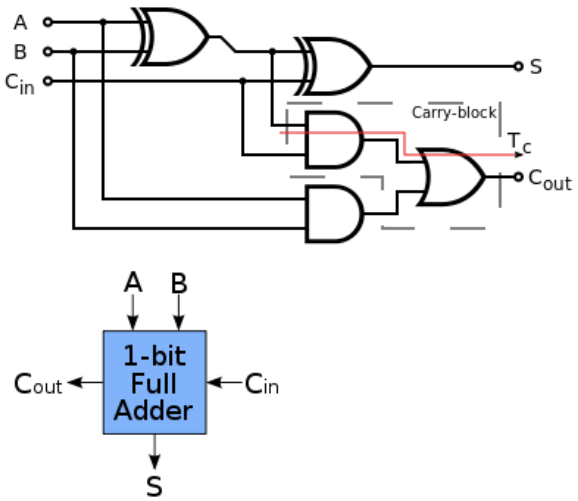

Figure 1 A full adder circuit diagram

No	A	B	Cin	S	Cout	X -S LH (ns)	X-S HL (ns)	X-Cout LH (ns)	X-Cout HL (ns)	*Pdiss* LH (mW)	Pdiss HL (mW)
1	0	1	↑↓	↓↑	↑↓	25.20	29.10	0.03230	0.3555	-1.6477	112.442
2	1	0	↑↓	↓↑	↑↓	24.30	28.40	0.03035	0.04555	-1.6437	111.302
3	1	1	↑↓	↑↓	1	0.04038	0.03842			0.016177	0.010242
4	0	↑↓	1	↓↑	↑↓	122.0	15.30	58.880	295.30	22.193	733.03
5	1	↑↓	0	↓↑	↑↓	50.35	199.90	460.20	460	-0.33988	181.203
6	1	↑↓	1	↑↓	1	205.10	75.20			-1.3434	18.4724
7	↑↓	0	1	↓↑	↑↓	160.5	180.8	45.80	40.95	16.390	33.574
8	↑↓	1	0	↓↑	↑↓	0.620	14.40	35.80	30.50	14.756	4.6460
9	↑↓	1	1	↑↓	1	204.55	135.60			-14.668	124.6848
10	0	↑↓	↑↓	0	↑↓			0.02010	0.01320	110.85	253.30
11	1	↑↓	↑↓	1	↑↓			0.01440	0.01010	-2.44.5	301.65
12	↑↓	0	↑↓	0	↑↓			0.03045	0.03550	-2.9850	295.40
13	↑↓	1	↑↓	1	↑↓			0.03750	0.02650	-3.5992	253.40
14	↑↓	↑↓	0	0	↑↓			3.250	3.585	-3.1590	240.50
15	↑↓	↑↓	1	1	↑↓			34.50	32.50	-3.5500	285.50
16	↑↓	↑↓	↑↓	↑↓	↑↓	0.002850	0.002560	0.00355	0.003285	-2.1580	224.5
Average						27.5647	140.0104	36.91995	49.92003	27.20608	160.46848

Table 2. Simulation results of the designed circuit. (Power dissipation, Propagation Delay)

No	A	B	Cin	S	Cout	X -S HL (ns)	X-S LH (ns)	X-Cout HL (ns)	X-Cout LH (ns)	*Pdiss* LH (mW)	Pdiss HL (mW)
1	0	1	↑↓	↓↑	↑↓	186.150	172.800	84.050	94.5050	15.270	31.345
2	1	0	↑↓	↓↑	↑↓	182.350	173.970	79.900	96.650	14.223	30.903
3	1	1	↑↓	↑↓	1	65.546	133.543			3.174	18.840
4	0	↑↓	1	↓↑	↑↓	190.938	177.752	90.5843	96.3553	8.403	35.420
5	1	↑↓	0	↓↑	↑↓	187.125	185.050	86.436	106.353	12.300	33.023
6	1	↑↓	1	↑↓	1	60.950	121.630			0	22.340
7	↑↓	0	1	↓↑	↑↓	183.150	170.819	83.1020	94.4353	7.430	35.020
8	↑↓	1	0	↓↑	↑↓	177.543	173.542	81.843	96.5446	7.420	34.542
9	↑↓	1	1	↑↓	1	69.5454	119.545			0	26.500
10	0	↑↓	↑↓	0	↑↓			83.342	96.242	1.543	33.443

11	1	↑↓	↑↓	1	↑↓			86.423	51.234	0	26.445
12	↑↓	0	↑↓	0	↑↓			4.63E+01	94.0353	1.345	33.040
13	↑↓	1	↑↓	1	↑↓			84.1253	47.453	0	38.830
14	↑↓	↑↓	0	0	↑↓			48.352	103.234	2.654	35.454
15	↑↓	↑↓	1	1	↑↓			90.1090	47.956	0	45.345
16	↑↓	↑↓	↑↓	↑↓	↑↓	65.4534	83.2534	49.234	47.642	0	46.356
Average						136.365	150.625	73.9409	82.5632	40.6523	33.6572

Table 3. Standard Circuit Results with 10 pF Capacitor.

3. CIRCUIT AND SIMULATION RESULT

As the simulation results are shown on Table 2,3 above. It can be said that the most energy efficient implementations are obtained from XNOR and XOR. Furthermore, the circuits are ideally suitable for low voltage applications. I have conducted several simulations for performance comparison. *LTSpice* is used for simulation and I used CMOS technology at a 5 V supply voltage. I added 10 pF capacitors and 10 Ohm resistors for appropriate circuit nodes and rising times of the input signals. I set the signals at 1 nanosecond. Our design has some essential characteristics such as number of transistors, working principles. The rise and fall times are nearly identical with the transmission gate XOR. Moreover, it is rapid and has the lowest power dissipation, and much lower power-delay on the low supply voltage.

Pass Transistor Logic

In integrated circuits, the pass transistor logic provides the opportunity of reducing the number of transistors to turn difficult logic circuits into simpler circuits by eliminating redundant transistors [3]. When *B* is '1', top device turns on and copies the input *A* to output *F*. The bottom device turns on and passes '0' when *B* is low.

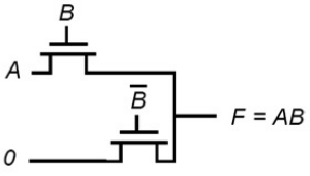

Figure 2 Pass Transistor Diagram

I found the power delay and power-delay product from 4.2 to 5 V by simulation for four different circuits. The efficiency of the 18-transistor full adder is the best among other circuits.

There is larger power dissipation in High-to-low transition but less propagation delay than the standard circuits at a low supply voltage. The designed full adder works properly even at a low supply voltage.

Transmission Gate Theory

A transmission gate is described as an electronic device which can selectively pass or block a signal from the input to the output [2]. It is the complementary solid-state switch that is comprised of a PMOS & NMOS transistors. It is also named as analog switch. It simply isolates multiple signals quickly.

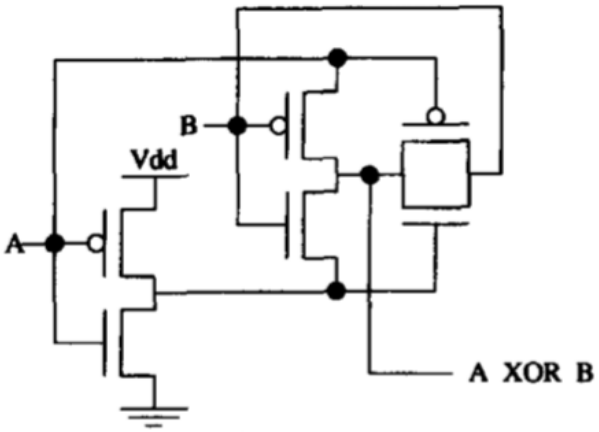

Figure 3 Transmission Gate of XOR Circuit

In the full adder design, the transmission gates are preferred as building blocks for logic circuitry. The complementary logic '0' is applied to node A when the voltage on node A is a logic '1' which allows both the transistors to conduct and pass the signal from IN to OUT.

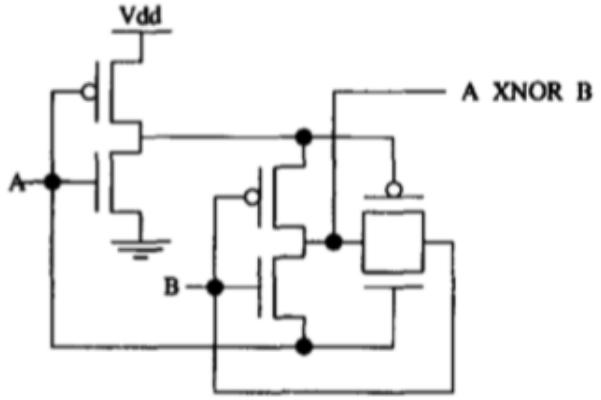

Figure 4 Transmission Gate of XNOR

When the voltage on active-low A is logic '0', A is applied the complementary logic '1'. It provides a negligible degradation in the characteristics of the signals in my circuit.

Additional Resistor, Diode, and Capacitors

As explained in electronics blogs, there are two diodes in a MOSFET, back to back: one by drain and bulk and the other by source and bulk. When a bulk is tied to a source in a discrete MOSFET, it shorts out the diode between them. Therefore, the other diode between the bulk and the drain can be forward biased. It is not a problem if a MOSFET works as an amplifier as the diode is always reverse biased.
On the contrary, if a MOSFET is used as a pass transistor, there is a condition by the time this diode is forward biased. For example, for an NMOS pass transistor, with the condition of Drain = 0 V, Gate = 0 V, Source = 5 V, the source voltage drops to 0.7 V because the diode is active. A simple solution to the problem is to put an external diode in series to a MOSFET in order to block forward biasing of the inherent diode. Preventing from a reverse current flow at the output side of a T-gate or pass transistor.
In two steps we can avoid from reverse current flow: Firstly, it is optional that adding a reverse diode to every pass transistor and a T-gate. Secondly, it would be also a solution to connect the body to either VDD (PMOS) or GND (NMOS).

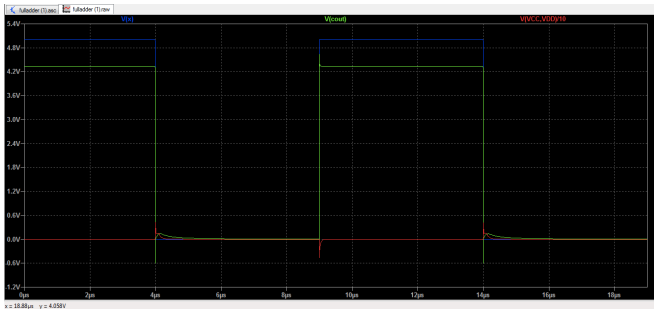
Figure 5 Power Dissipation Method

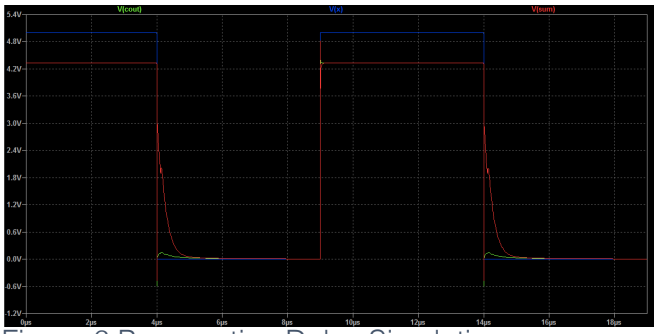
Figure 6 Propagation Delay Simulation

Propagation Delay Measurement

It is the length of time taken for the signal to reach its destination, 50% points. Simply, the duration between sender and receiver is calculated here. It has been a major obstacle in the development of high-speed electronic devices [4]. It is an essential case that reducing gate delays in such circuits like full adder enables us to process data at a faster level. In physics, it is particularly related to electromagnetic field.
One-half the total transition corresponds to 50 percent point between V_H and V_L: $V_{50\%} = \frac{\mathbf{Vhigh+\ Vlow}}{2}$
T pHL is high-to-low output transition. T pLH is low-to-high output transition. In the general case of full adder, these two delays are not equal.
The average propagation delay is defined by Tp $= \frac{\mathbf{TpLH+TpHL}}{2}$
It is obviously shown that the proposed full adder is preferable over the standard full adder. As reported in the measurement table, the proposed high-speed full adder is approximately 8 times faster than the standard full adder circuit in terms of propagation delay.

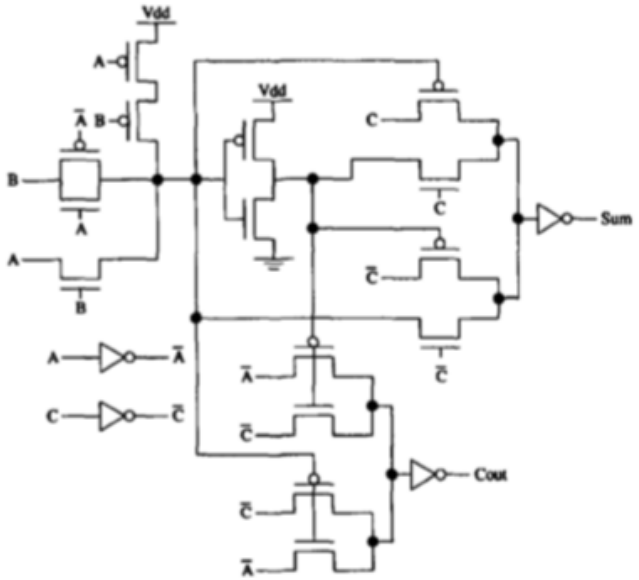

Figure 7 Proposed Full Adder Diagram

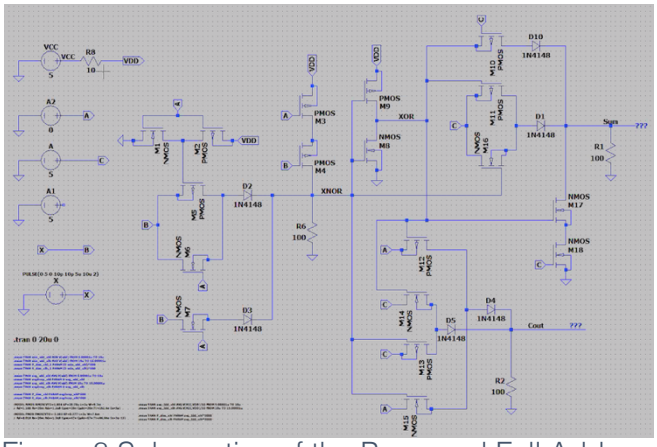

Figure 8 Schematics of the Proposed Full Adder

Full Adder

The full adder circuit consists of three input bits and two output bits. The three inputs: A, B, Ci where A and B bits to be added and the previous carry bit is assigned to Ci. Sum and Cout are outputs where S are the Sum bit and Cout is the carry bit generated for this sum. We can observe that the output of the sum is high whenever there are odd number of high inputs. On the other hand, Cout bit is high level if at least 2 or more inputs are high.

Dynamic Power Dissipation Measurement

In this section, I considered the primary contribution to power dissipation. The dynamic power dissipation, critical source of power dissipation, occurs during the process of charging and discharging the load capacitance of a logic gate. In the full adder, the 10-pF capacitor was being charged from VDD. I added a-10 Ohm resistor between VDD voltage source, power source, and the circuit. Next, I measured the average voltage drop. Then, the average current is calculated by dividing voltage source and the resistor. It is the product of that current and VDD. The essence of using LTSpice is the formulas they provide freely. I used Power dissipation formulas in LTSpice shown below in Figure 7. There are negative power dissipation results which are the signs of some reactive components inside full adder circuitry. Additionally, it is also critical that at high switching levels the dynamic behavior becomes dominant. In other words, it is dynamic power dissipation that proportional to the switching frequency of the logic gate, and the square of the logic voltage swing.

```
.meas TRAN avg_Idd_xhl AVG V(VCC,VDD)/10 FROM 5.00001u TO 10u
.meas TRAN avg_Idd_xlh AVG V(VCC,VDD)/10 FROM 10u TO 15.00001u

.meas TRAN P_diss_xhl PARAM avg_Idd_xhl*5000
.meas TRAN P_diss_xlh PARAM avg_Idd_xlh*5000
```

Figure 9 Power Dissipation Formulas LTSpice

As a coin has two sides, increasing the speed, reducing the propagation delay has its own benefits and drawbacks. The downside of the proposed high-speed full adder is having greater power dissipations which cause overtemperature in real cases. The power dissipation of the proposed high-speed full adder is larger than the standard circuit on high-to-low transition according to measurements comparison in Table 1 and Table 2.

Design Differences with the Standard Circuit

In electronics, building circuits with less components but greater results are stepping-stones for design requirements. Designing a digital circuit requires 4 steps to apply. Less noise, low power dissipation, smaller area, and low delay. Therefore, the number of components in the proposed full adder are lesser than the number of components in the standard full adder circuit, and it is a benefit. On the other hand, the more electronic components lead to greater power dissipation, areas, and large propagation delays.

Discussion

In this report, an exclusive-OR and exclusive-NOR have been proposed for CMOS implementation. Although the proposed XOR and XNOR circuits

have meaningful output levels in terms of design requirements, the high-power dissipation is a drawback at a low supply voltage. I have obtained useful design outputs in terms of low propagation delay product, less electronic components which play a key role in design factors. On the other hand, the power dissipation is greater than the standard circuit. Power dissipation has been a major factor of designing digital circuitry. Thus, low power dissipation is critical in terms of energy consumption. Therefore, my proposed 18-transistor full adder circuit is energy efficient and ideally suitable for low voltage applications.

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