

- 1) a)
1. Central processing unit (CPU)
 2. Main memory
 3. I/O
 4. System interconnection

- b)
1. Control unit
 2. Arithmetic and logic unit (ALU)
 3. Registers
 4. CPU interconnection

2) a)

Average access time = avg. seek time + avg. rotational delay + transfer time + controller overhead + queuing delay

Time taken for 1 full rotation = $60/20000 \text{ s} = 3 \text{ ms}$

avg rotational delay = $1/2 \times \text{time taken for one full rotation} = 1.5 \text{ ms}$

In 1 full rotation, 1 track or 500 sectors can be transferred. Or 500 sectors transferred in 3 ms. Then file of 3000 sectors transferred in $(3 \times 3000)/500 = 18 \text{ ms}$

Transfer time = 18 ms

Controller overhead + queuing delay is assumed to be zero. Since the organization of the disk is sequential, assuming the file is read sequentially, only 1 seek time and 1 rotational delay is taken for the first positioning of the read/write header.

Average access time = $3 + 1.5 + 18 = 22.5 \text{ ms}$

It takes 22.5 ms to read the file.

b)

The file consists of 3000 sectors. Given, 1 sector = 512 Bytes

Thus, the file size = $3000 \times 512 \text{ Bytes} = 1500 \text{ KB}$

$= 1500/1024 \text{ MB} = \text{1,47 MB}$

4)

1. Register
2. Start of called procedure
3. Top of stack

5)

$$C1 = D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7$$

$$C2 = D1 \oplus D3 \oplus D4 \oplus D6 \oplus D7$$

$$C4 = D2 \oplus D3 \oplus D4 \oplus D8$$

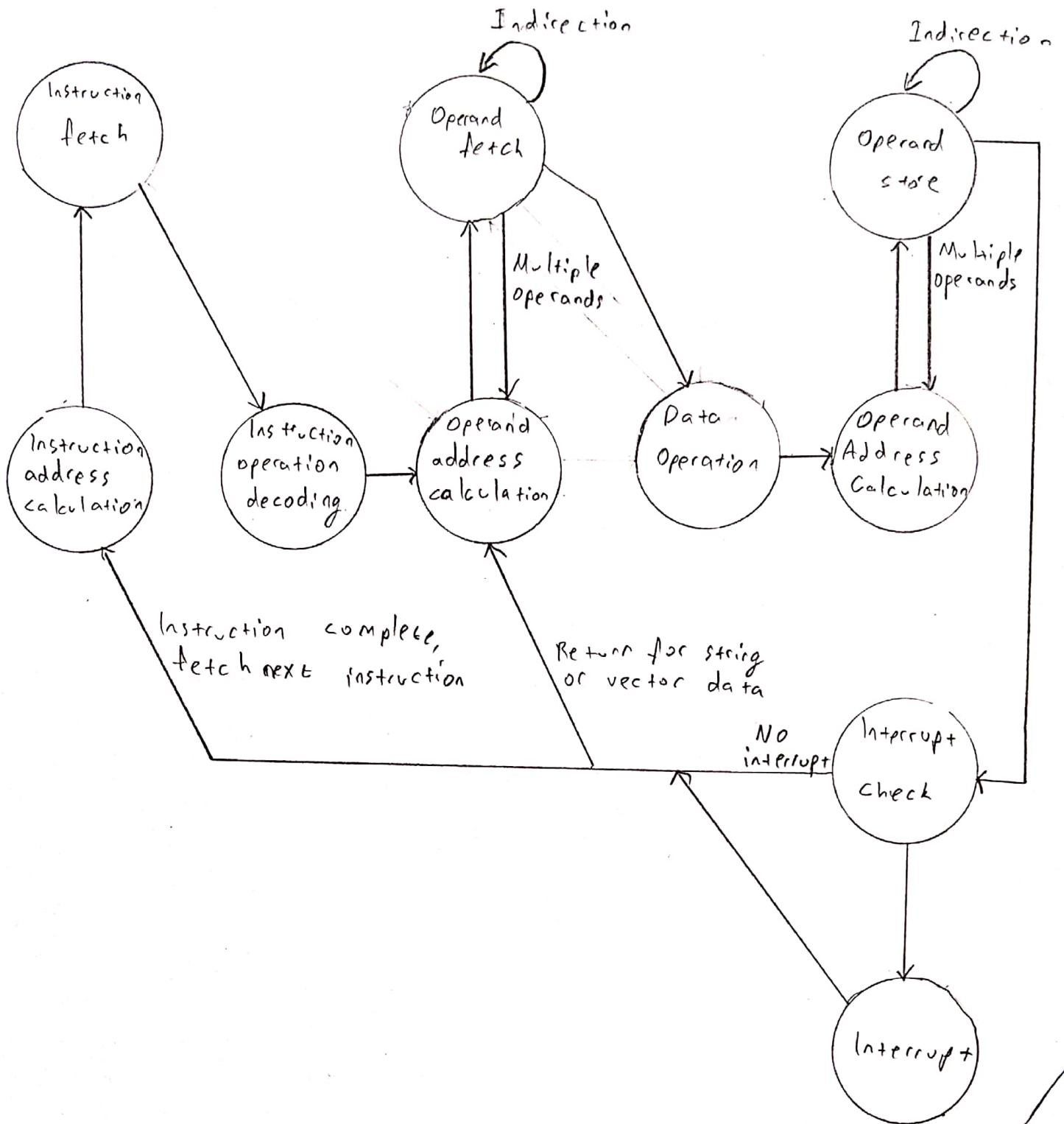
$$C8 = D5 \oplus D6 \oplus D7 \oplus D8$$

$$C8C4C2C1 = 0001$$

$$1101 \times 0R 0001 = 1100 \text{ (12. bit is incorrectly read)}$$

Thus 11010101 (12. bits is the table. 8. bits in the word)

8)



g)

i)

This instruction will shift the bit one by one to the left starting from LSB i.e. B0 and the MSB i.e. B7 is rotated to LSB and to the carry flag. The MODE field holds the value 01, which indicates operand1 is a register and operand2 is a memory addresses, the I field holds the value 00, which indicates, No instruction is used for both OPE1 and OPE2. OPE1 has the bin data 00000011, which indicates the Register R3, which holds the value 51. OPE2 has the bin data 10100101, which indicates the memory address [A5] which holds the value 03.

The instruction for the given representation is,

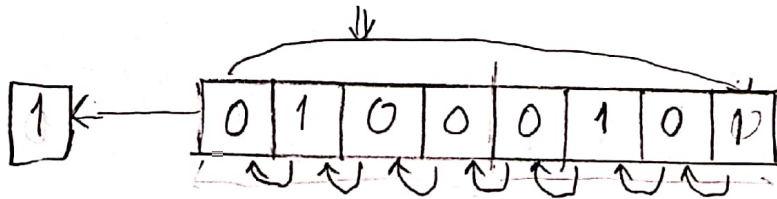
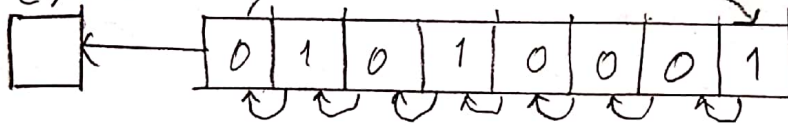
ROL R3, A5H

A5H represents memory address it is direct addressing mode.

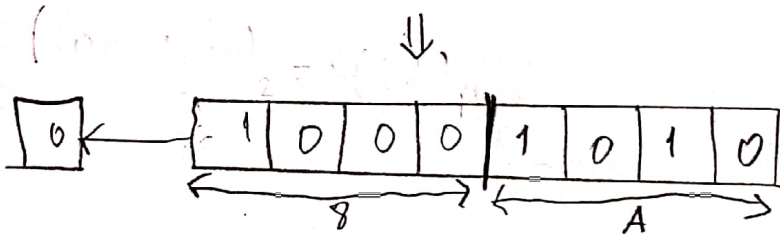
The value in the register R3 i.e. 51 is rotated left by 3 times as the value at address A5 is 03.

51 H \Rightarrow (01010001)₂

(Carry Flag)
CY



Result after
2nd state



Result after
3rd state

(10001010)₂ \Rightarrow (8A)_H

9.1)

Operands used	Result (hexadecimal)
OPE1 is Register 'R3' and OPE2 is memory address 'A5'	8463

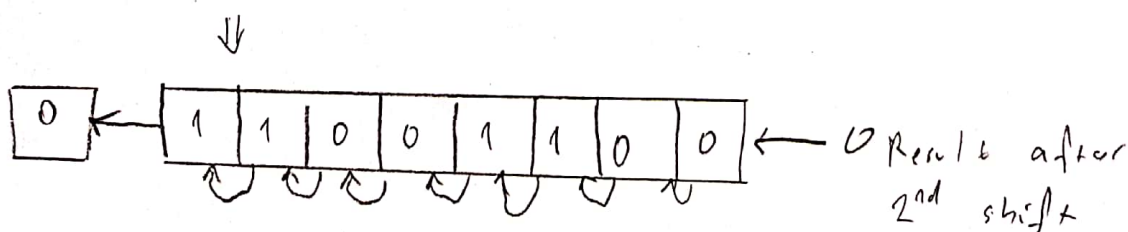
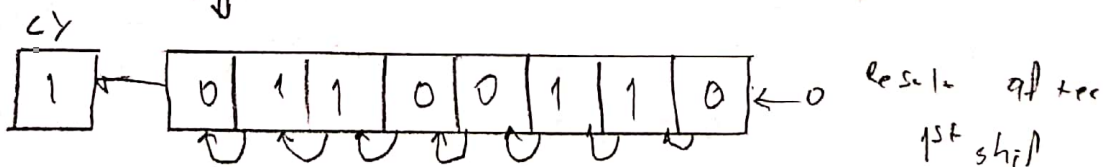
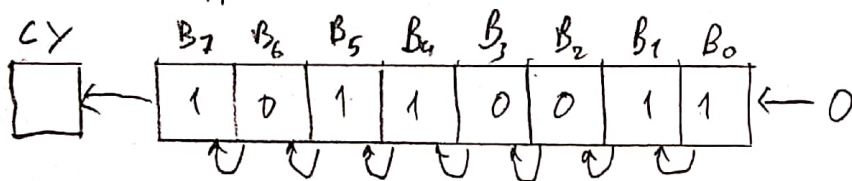
9.2i)

The OPCODE field holds the bin data 0001 which indicates the instruction SAL. Mode field holds the bin value 01 which indicates OPE1 is register and OPE2 is a memory address. I field holds the value 10 indicates indirection is used only for OPE2. OPE1 holds the bin value (00000001), represents the register R1 which holds the value B3. OPE2 holds the bin value (10100100) represents the memory address A4 which holds the value A1. Hence the instruction in indirect addressing mode, the memory address A4 points the location A1. The location A1 holds the value 03.

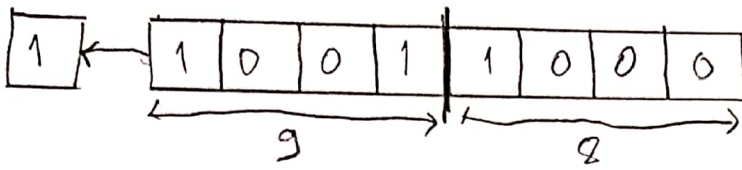
SAL R1, [A4]

[A4] is indirect addressing mode, so the R1 is shifted arithmetic left by 03 times.

$$R_1 \Rightarrow (B3)_H \Rightarrow (10110011)_2$$



9.ii)

Result after
3rd shift

$$(10011000)_2 \Rightarrow (98)_H$$

Operands used	Result
OPE1 is Register R1 and OPE2 is memory address [A4]	98

9.iii)

Opcode: 0010 \Rightarrow Shift Arithmetic Right (SAR)mode field = 01 \Rightarrow OPE1 is register, OPE2 is memory address

I-field holds value 11, indirection is used for both OPE1 and OPE2

OPE1 \Rightarrow 0000010 \rightarrow register R2, its value 00OPE2 \Rightarrow 10100010 \rightarrow memory A2, its value A3

SAR, R2, A2

10)

a)

1. LRU
2. FIFO
3. LFU
4. Random

b)

$$32 \text{ MB} = 33\,554\,432 \text{ Bytes}$$

$$128/4 = \frac{2^{17}}{2^2} = 2^{15} \quad 15 \text{ line}$$

$$\text{word} = 2$$

$$\begin{array}{ccc} \text{tag} & + & \text{Line} & + & \text{Word} & = & 25 \\ \downarrow & & \downarrow & & \downarrow & & \\ 8 & & 15 & & 2 & & \end{array}$$

Tag	Line	Word
8	15	2 bits

11)

a)

b)

Hazard #	Hazard type	Reason
1.	RAW	Here cx is read by instruction 6 before it can be written by instruction 4
2.	RAW	Here bx is read by instruction 6 before it can be written by instruction 5