Chih-Hung(Namo) Lu

285 8th Ave N ● APT#701 ● Seattle, WA 98109 ● 518-776-0077
chih-hung.lu@columbia.edu

EDUCATION

Columbia University, Fu Foundation School of Engineering and Applied Science Dec.2017
MS in Computer Science - 3.5 / 4.3

National Chiao Tung University, Department of Electronic Engineering Jun.2009
MS in Electrical Engineering - 4.1 / 4.3

TECHNICAL SKILLS

Programing Languages: Java, C/C++, Python, SQL, JavaScript, HTML&CSS, ARM Assembly, MIPS Assembly, Makefile

RELEVANT COURSEWORK

Distributed System, User Interface, Database, Programming Language and Translator, Database, Data Structure, Computer Networks, Operating System, Probability & Statistics, Graph Theory, Computer Architecture, Analysis of Algorithm, Software Engineering

HONORS

Patent: https://patents.justia.com/patent/20110153709

- Presented invention relates to compressor tree synthesis algorithm Jun.2011

WORK EXPERIENCE

Amazon Web Services, Inc (Software Development Engineer), USA Mar.2018 – Now

- Refined node repair workflow on top of AWS Simple Workflow by resigning Paxos distinguished proposer, which reduced 95% latency
- Implement authority checker in heartbeat mechanism of distributed services to prevent bad service receive client's request
- Implement performance bench automation workflow to support multiple testing targets, and result diagnostics

Amazon.com (Software Development Engineer Intern), USA May.2017 – Aug.2017

- Designed dynamic web content validation workflow by request redirection to replace incomprehensive static validation
- Implement data access object model (DAO) on top of AWS DynamoDB for data sharing between distributed validation services
- Implement memory cache to reduce latency between application and database
- Designed RESTful API gathering content differences between two versions in Amazon in-house object storage database
- Adopted worker pool to reduce run time from 21 minutes to 6 minutes per API call

RealTek Inc. (Senior Member of Technical Staff), Taiwan Nov.2015 – Aug.2016

- Designed bare-metal software platform running packet off-loading process to reduce loading from main CPU

MStar Semiconductor (Senior Software Engineer), Taiwan Aug.2010 – Sep.2015

- Developed embedded Linux platform, and troubleshot system crash issues like data un-coherence and interrupt non-response
- Designed, analyzed and troubleshot TCP/IP Ethernet software module, and solved packet loss as well
- Improved networking performance from 7X to 8X Mbps by designing multithread packet transmission in Ethernet module

PROJECT EXPERIENCE (https://github.com/mud2man)

Floor Plan Language Compiler (OCaml, C) Sep.2017 – Dec.2017

- Designed C-Like language compiler on LLVM platform linked with OpenGL library to generate floor plan graph
- Floor Plan Language supported user-defined function, user-defined structure, and built-in data type

Tweet Trend Map (JavaScript, HTML, CSS) Sep.2017 – Dec.2017

- Accomplished a web application to do sentiment analysis of real time Twitter data by using Microsoft Azure Text Analytics API
- Applied JQuery Location Picker to show positive, neutral and negative sentiment Tweets within user-specified region

Mutable Replay (Java) Sep.2016 – May.2017

- Designed Maven plugin Mdiff which can differentiate Java source code using Longest Common Subsequence and ASM 4.0
- Designed dynamic analysis on top of Mdiff, record-and-replay platform ChroniclerJ to check replay ability with code change

Restaurant.io (Python, SQL) Jan.2017 – May.2017

- Implemented web application about restaurant recommendation based on Flask platform, and used PostgreSOL as data base

Linux RR Scheduler & File System Driver (C) Jan.2017 – May.2017

- Designed Linux 4.4.50 scheduling policy supporting round-robin CPU scheduling in SMP system
- Designed brand new file system driver based on self-defined file system format, which can support file read, write, add and delete

Intra-domain Routing Emulation (Java) Jan.2017 – May.2017

- Designed distance-vector routing protocol that allows dynamic change in network topology, and detect link weight with Go-Back-N protocol using multithreading

RESEARCH EXPERIENCE

Electronic Design Automation Lab at National Chiao Tung University, Taiwan Aug.2007 – Aug.2009
"Delay Optimal Compressor Tree Synthesis for LUT-Based FPGA" (C++)

- Designed Integer-Linear-Programming algorithm to synthesize compressor trees, which reduced depth of compressor tree by 32 %
- Implemented post-processing method to reduce area of synthesized compressor tree by 21% on average