Report of Router 1X3 implementation using Fusion Compiler

Fusion Compiler Unified Flow

The Main "run.tcl" script

```
### Technology setup ###

source -echo ./setup.tcl

create_lib -technology $TECH_FILE -ref_libs $REFERENCE_LIBRARY router_core.dlib

analyze -format verilog [glob rtl/*.v]

elaborate router1x3
set_top_module router1x3
save_lib

### S D C ###
create_clock -period 10.0 -name router_clock [get_ports clock]

### Parasitics ###
read_parasitic_tech -layermap ../ref/tech/saed32nm_tf_itf_tluplus.map -tlup
../ref/tech/saed32nm_1p9m_Cmax.lv.nxtgrd -name maxTLU
read_parasitic_tech -layermap ../ref/tech/saed32nm_tf_itf_tluplus.map -tlup
../ref/tech/saed32nm_1p9m_Cmin.lv.nxtgrd -name minTLU

report_lib -parasitic_tech router_core.dlib
get_site_defs
set_attribute [get_site_defs unit] symmetry Y
set_attribute [get_site_defs unit] is_default true
set_attribute [get_layers {M1 M3 M5}] routing_direction horizontal
set_attribute [get_layers {M2 M4 }] routing_direction vertical
get_attribute [get_layers M?] routing_direction
report_ignored_layers
set_ignored_layers -max_routing_layer M6
report_ignored_layers

### Upf ###
```

```
load_upf ./scripts/router_core.upf
commit_upf
check_mv_design

## Modes and corners ###
source ./scripts/router_scenario.tcl
report_scenario

# Stages of compile fusion ###
set_app_option -name dft.insertion_post_logic_opto -value false
set_app_option -name place.coarse.continue_on_missing_scandef -value true
compile_fusion -to initial_map
compile_fusion -to logic_opto
compile_fusion -to initial_place
compile_fusion -to initial_drc
compile_fusion -to initial_opto
compile_fusion -to final_place
compile_fusion -to final_opto
save_lib
save_block


###floor planning###
initialize_floorplan
initialize_floorplan -shape L -orientation W -side_ratio {2 2 1 2} -core_offset {10}
shape_blocks
create_placement -floorplan
legalize_placement
set_block_pin_constraints -self -allowed_layers {M1 M2 M3 M4 M5 M6 M7 M8}
place_pins -self
change_selection [get_ports *clock]
gui_set_setting -window [gui_get_current_window -types Layout -mru] -setting showPinGuide -
value true
create_pin_constraint -type individual -ports [get_ports *clock] -width 0.1 -length 0.4
place_pins -self
source -echo scripts/pns.tcl

### CHECK PG NETS DRC####
check_pg_connectivity
check_pg_drc
check_pg_missing_vias
save_block
save_lib

## Setup
####################################
```

```
report_clock

### S D C ###
create_clock -period 10.0 -name router_clock [get_ports clock]


####################################
####################################
## Option A: Classic CTS
####################################
set_app_options -name clock_opt.flow.enable_ccd -value false
set_app_options -name cts.compile.enable_local_skew -value true
set_app_options -name cts.optimize.enable_local_skew -value true
clock_opt -to route_clock
report_clock_qor

####################################
## Post-CTS optimization
####################################
## make sure hold scenarios are enabled
report_scenarios
report_qor -summary

#Set up the design for signal routing
source scripts/route_setup.tcl
clock_opt -from final_opto
save_block

####################################
## Final Task
report_qor -summary
report_timing

#      check for any issues that might cause problems during routing
#      the app option allows for more detailed reporting
set_app_options -name route.common.verbose_level -value 1
check_design -checks pre_route_stage
set_app_options -name route.common.verbose_level -value 0

#      Antenna
source -echo ../ref/tech/saed32nm_ant_1p9m.tcl
report_app_options route.detail.*antenna*

#      Set application options for track and detail routing
set_app_options -name route.track.timing_driven     -value true
set_app_options -name route.track.crosstalk_driven -value true
```

```
set_app_options -name route.detail.timing_driven    -value true
set_app_options -name route.detail.force_max_number_iterations -value false

#      Check the power supplies
report_power_domains

# Have a look at the secondary PG routing for the level shifters:
change_selection [get_cells -hierarchical -filter is_level_shifter&&full_name=~*ROUTER*]

## Routing
#####################################
route_auto
check_routes
route_detail -incremental true -initial_drc_from_input true
#      Shorts? can't be fixed? Try deleting shapes, then run:
route_eco -utilize_dangling_wires true -open_net_driven true
save_block


####################
# Filler cell insertion
set SH_FILLERS "*/SHFILL128_HVT */SHFILL64_HVT */SHFILL3_HVT */SHFILL2_HVT
*/SHFILL1_HVT"
create_stdcell_fillers -lib_cells $SH_FILLERS
connect_pg_net
remove_stdcell_fillers_with_violation

## Post-Route Optimization
#####################################route_opt
route_opt
rename_block -to_block router_TOP/route_opt
save_lib
report_qor -summary

####check for errors###
report_timing
report_global_timing
check_error
report_constraints
report_congestion
check_lvs
report_power
```

The Main “setup.tcl” script

```
lappend search_path scripts design_data

set TECH_FILE      "../ref/tech/saed32nm_1p9m.tf"
set REFLIB         "../ref/CLIBs"

set REFERENCE_LIBRARY [join "
    $REFLIB/saed32_hvt.ndm
    $REFLIB/saed32_lvt.ndm
    $REFLIB/saed32_rvt.ndm
    $REFLIB/saed32_sram_lp.ndm"]
```

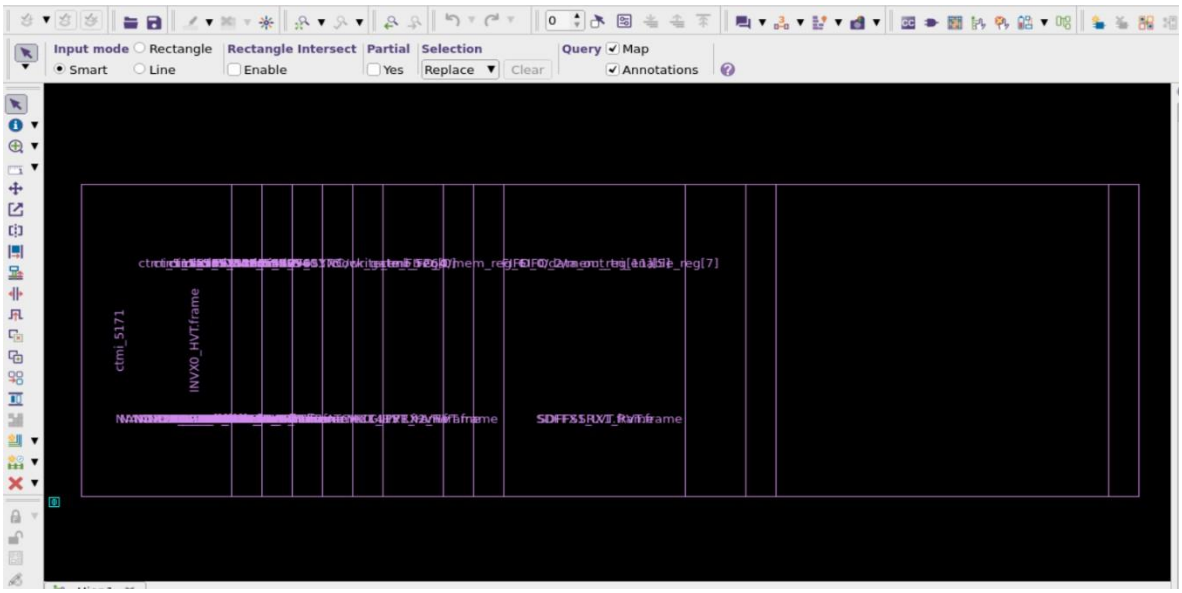

Fig. View Before compile_fusio

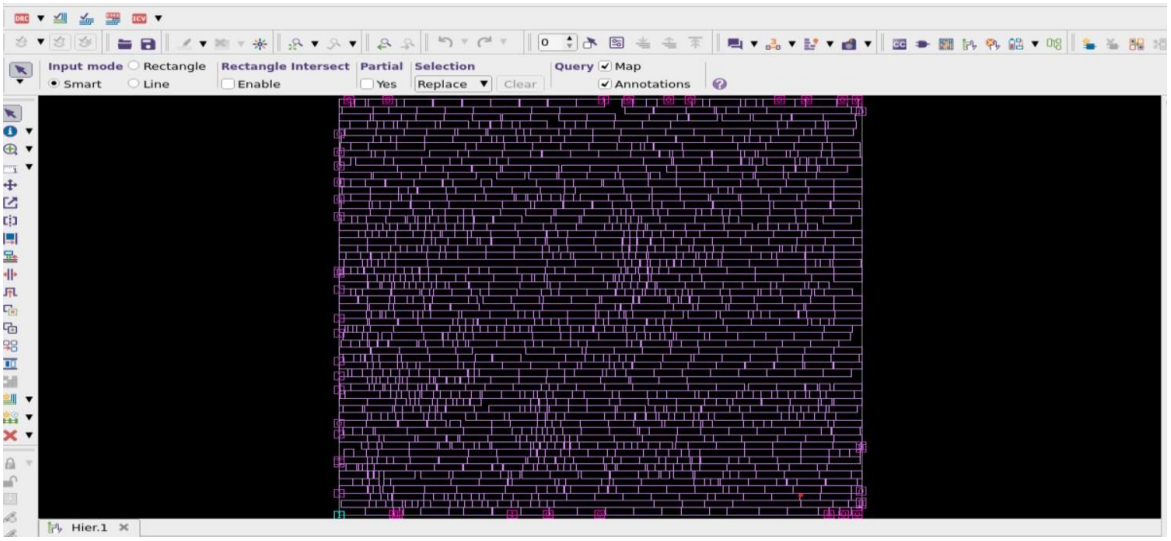

Fig. View After compile_fusion

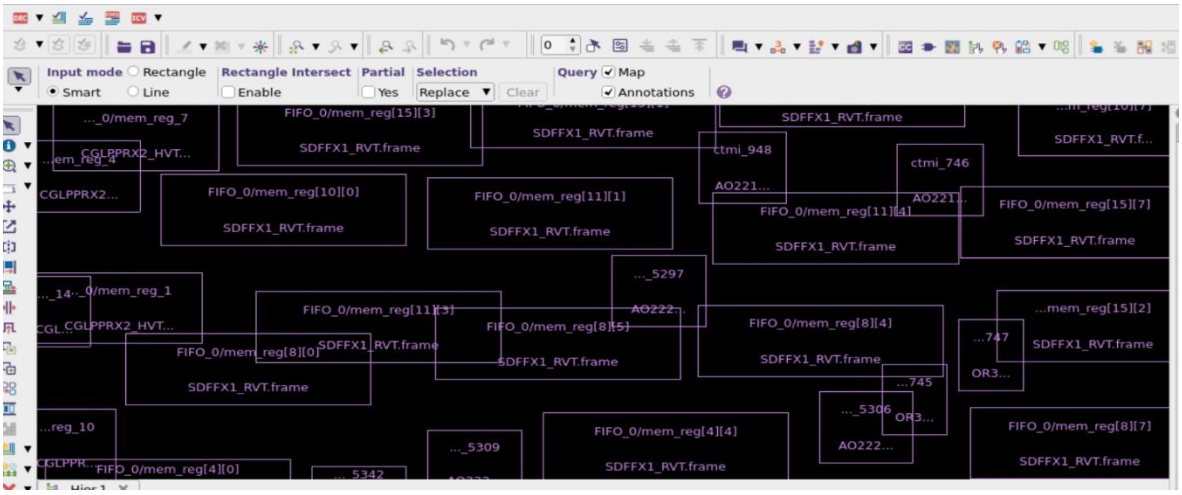

Fig. View After compile_fusion

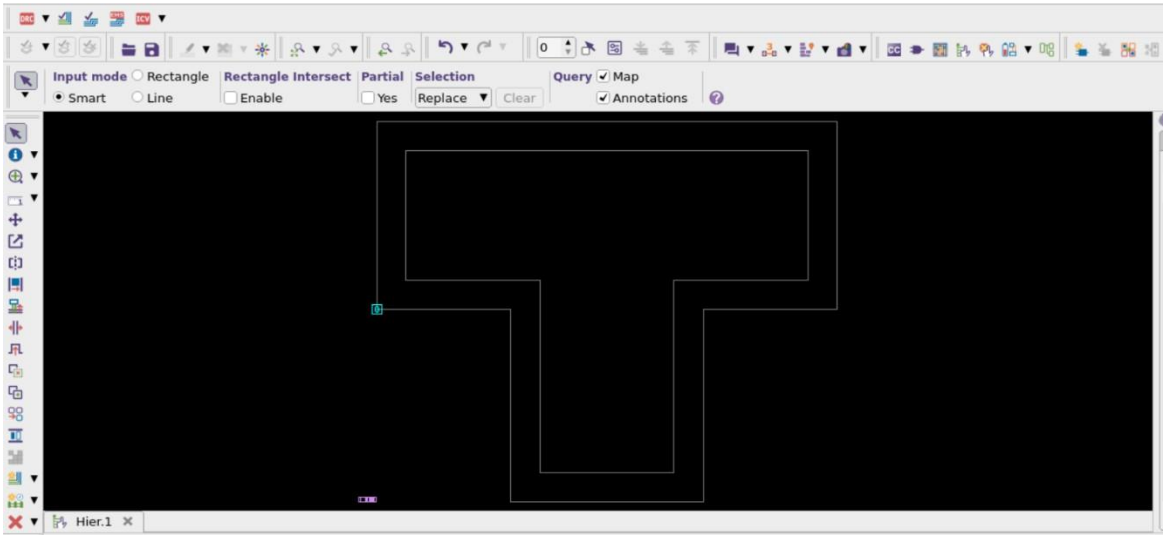

Fig. View After Floorplan Initialization

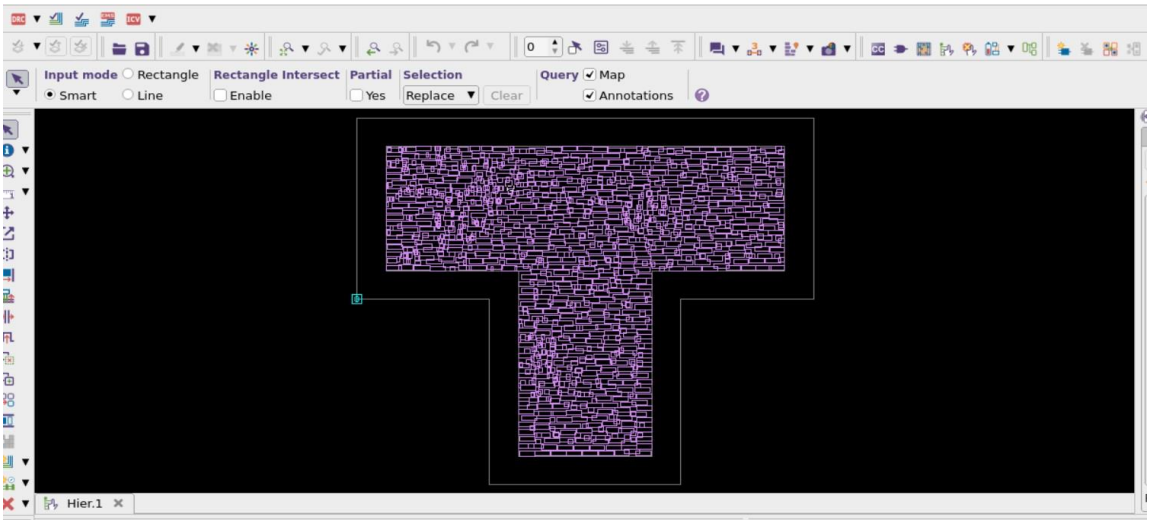

Fig. View After Placement (Not Legalized)

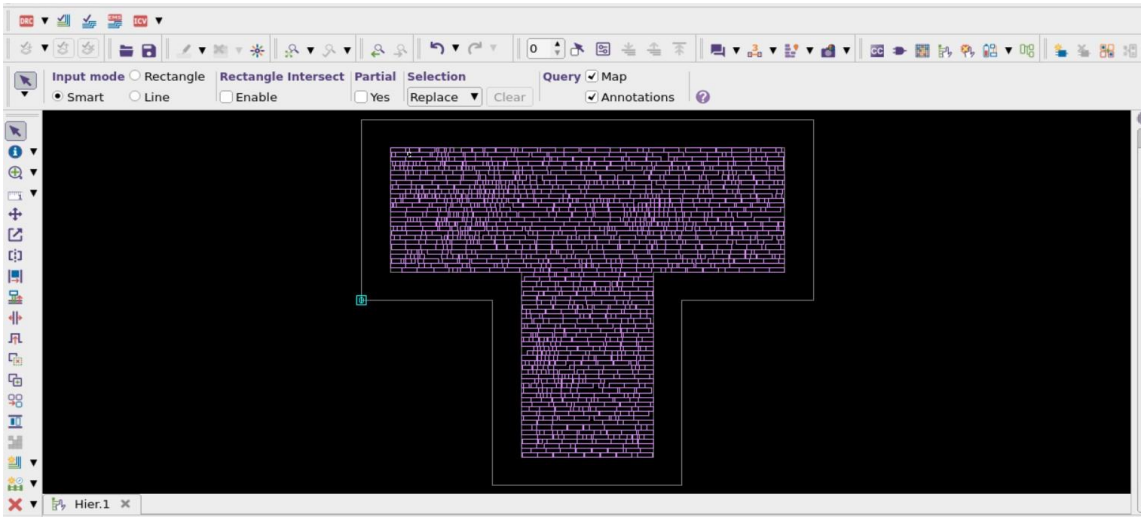

Fig. View after legalized placement

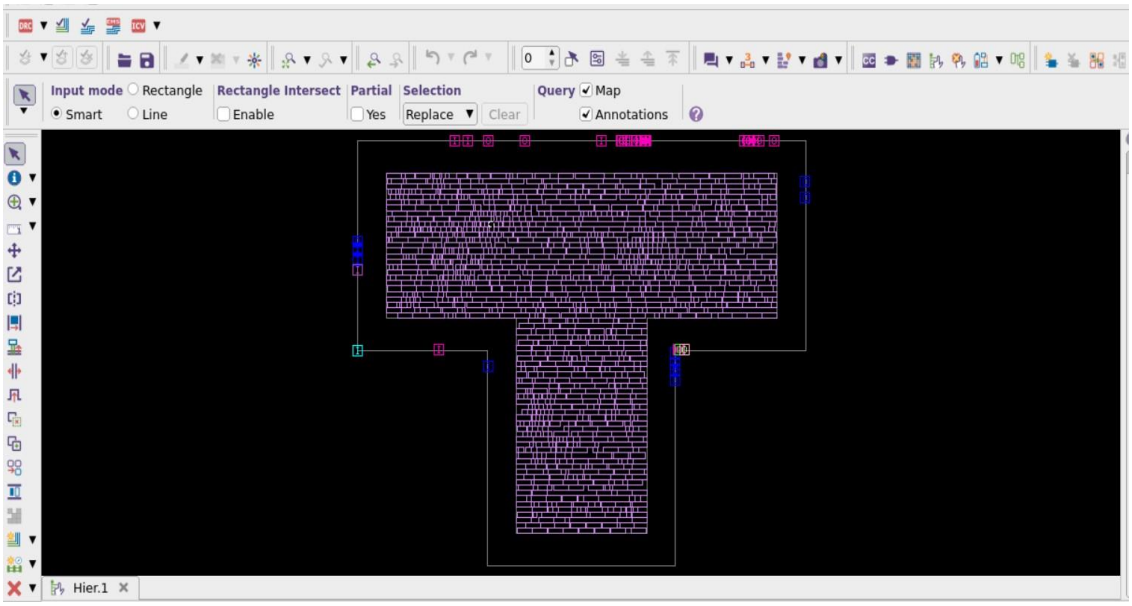

Fig. View After Placing the Pins

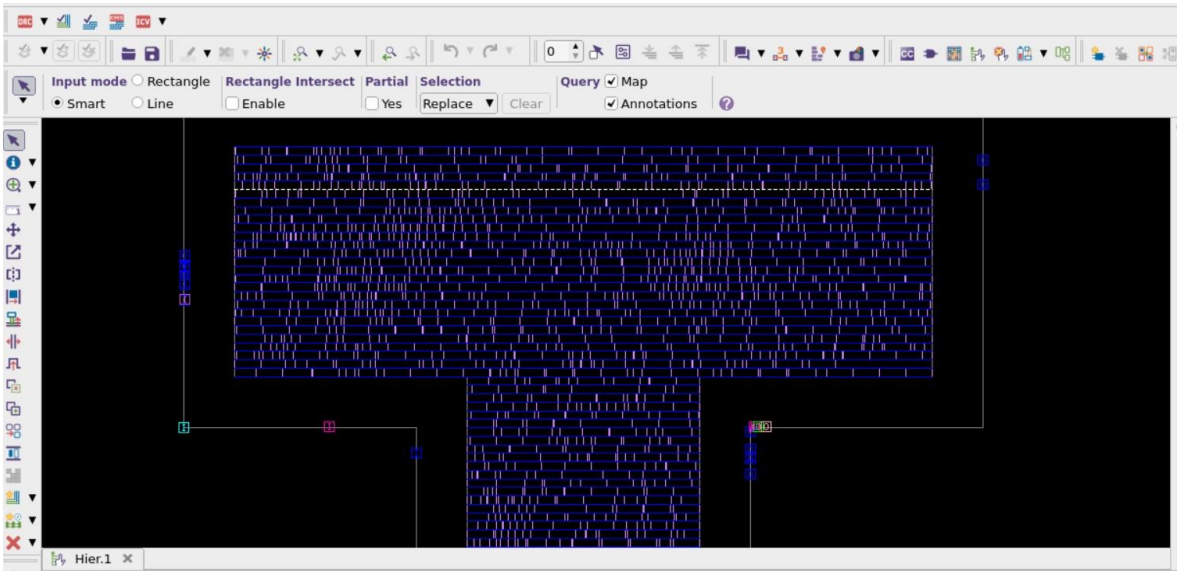

Fig. View after PG Mesh

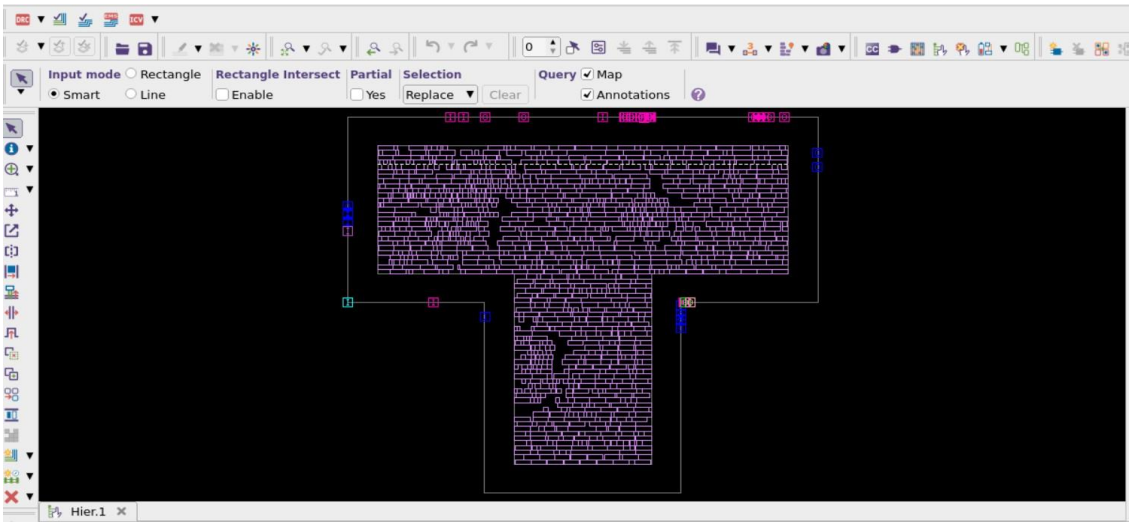

Fig. View after clock_opt -to build_clock

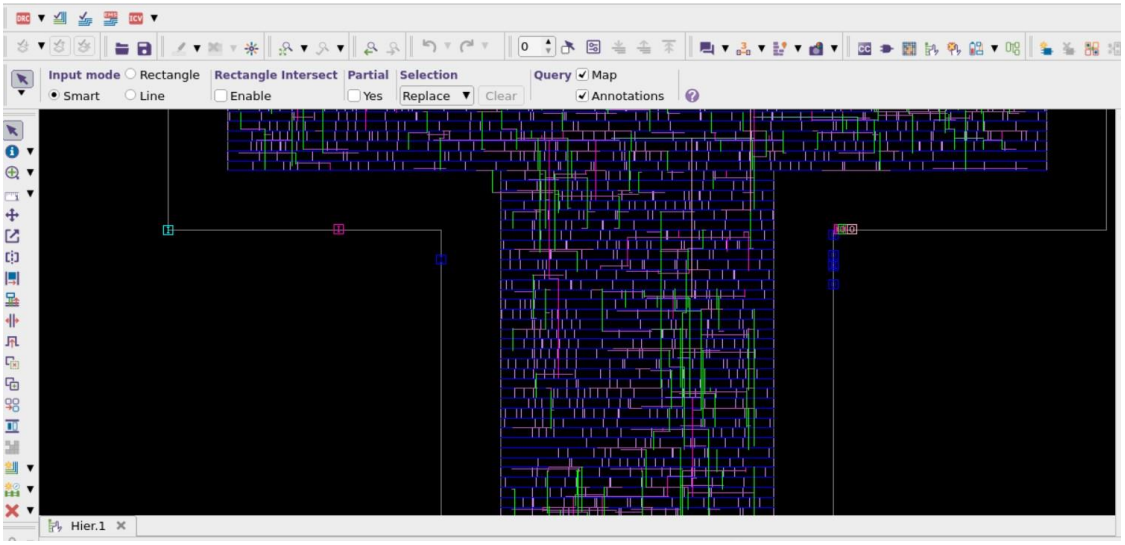

Fig. View after clock_opt -to build_clock

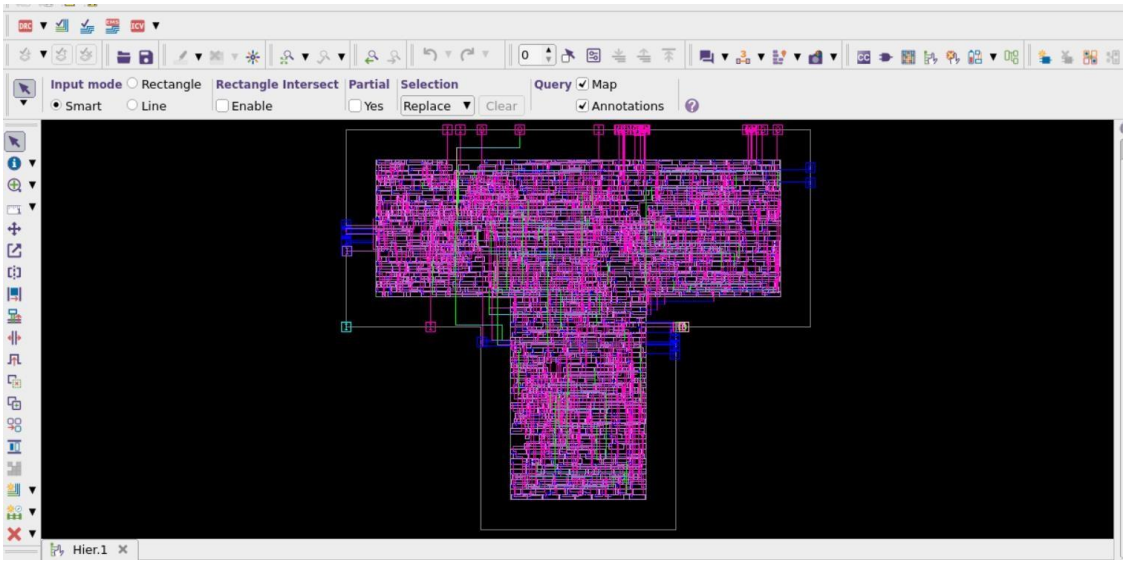

Fig. View after clock_opt -from final_opto

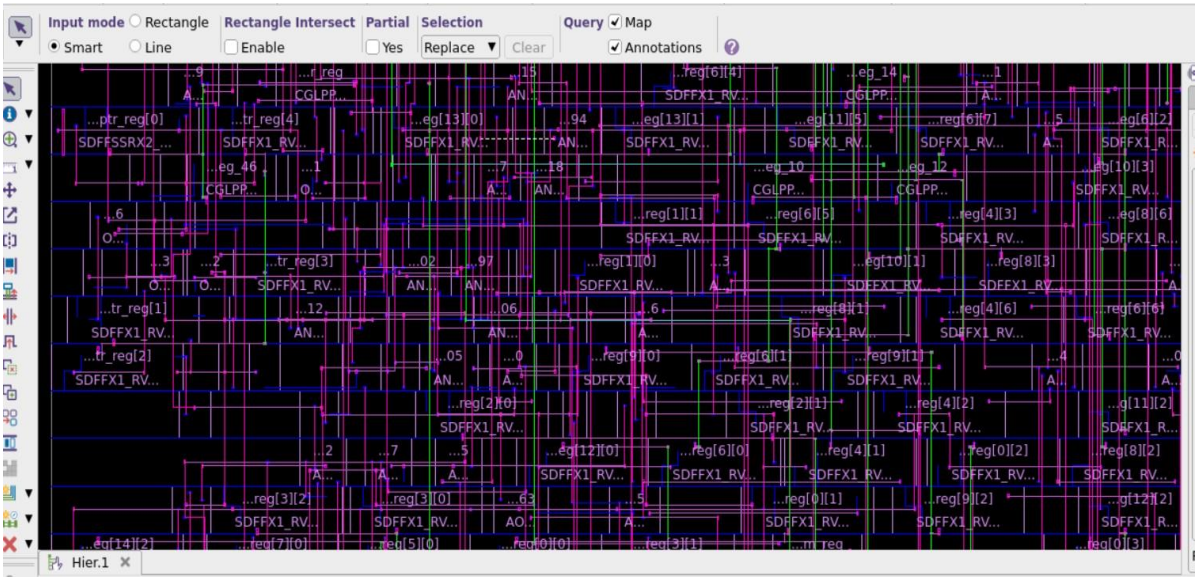

Fig. View after clock_opt -from final_opto

Fig. View after route_auto and route_opt

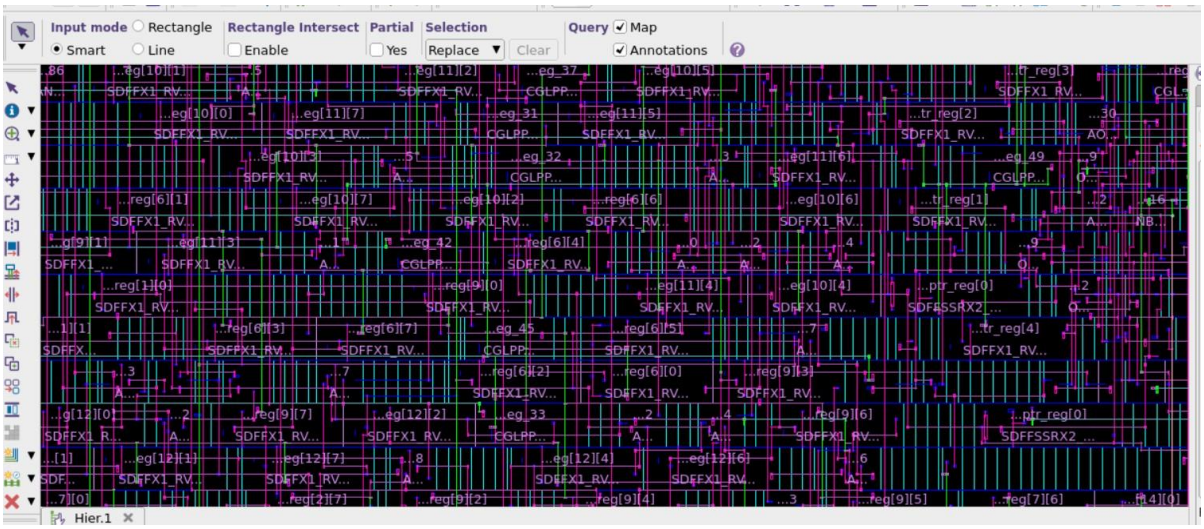

Fig. View after route_auto and route_opt

Design reports

Report timing

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
        -pba_mode path
Design : router_top
Version: U-2022.12-SP6
Date   : Wed  Aug 10 12:26:54 2024
****************************************
```

Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis, AWP, PBA Mode Path'. (TIM-050)

```
  Startpoint: fifo_1/rptr_reg[3] (rising edge-triggered flip-flop clocked by router_clock)
  Endpoint: fifo_1/data_out_reg[7] (rising edge-triggered flip-flop clocked by router_clock)
  Mode: func
  Corner: ss_125c
  Scenario: func::ss_125c
```

Path Group: router_clock
Path Type: max

Point	Incr	Path
clock router_clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.36	0.36
fifo_1/rptr_reg[3]/CLK (SDFFX1_RVT)	0.00	0.36 r
fifo_1/rptr_reg[3]/QN (SDFFX1_RVT)	0.12	0.48 f
HFSBUF_329_1466/Y (NBUFFX2_HVT)	0.10	0.58 f
ctmi_4067/Y (OA222X1_HVT)	0.14	0.72 f
ctmTdsLR_2_3286_roptpi_3293/Y (AND3X1_HVT)	0.13	0.85 f
ctmi_4055/Y (NAND2X2_HVT)	0.16	1.01 r
ctmi_4232/Y (NAND2X0_HVT)	0.21	1.22 f
phfnr_buf_1432/Y (INVX0_HVT)	0.19	1.41 r
ctmi_4237/Y (AND4X1_HVT)	0.23	1.64 r
ctmi_4255/Y (AND3X2_HVT)	0.18	1.82 r
ctmi_4254/Y (AO22X1_HVT)	0.16	1.98 r
ctmi_4247/Y (AO221X1_HVT)	0.13	2.10 r
ctmi_4243/Y (AO221X1_HVT)	0.14	2.24 r
ctmi_4240/Y (AO221X1_HVT)	0.13	2.38 r
ctmi_684/Y (OR3X1_HVT)	0.13	2.50 r
ctmi_683/Y (AO221X1_HVT)	0.13	2.64 r
fifo_1/data_out_reg[7]/D (SDFFX1_RVT)	0.00	2.64 r
data arrival time	2.64	
clock router_clock (rise edge)	10.00	10.00
clock network delay (propagated)	0.21	10.21
fifo_1/data_out_reg[7]/CLK (SDFFX1_RVT)	0.00	10.21 r
library setup time	-0.12	10.10
data required time	10.10	

data required time	10.10
data arrival time	-2.64
slack (MET)	7.46

1

Report constraints

```
****************************************
Report : constraint
Design : router_top
Version: U-2022.12-SP6
Date   : Wed Aug 10 12:30:02 2024
****************************************

                                  Weighted
  Group (min_delay/hold)     Cost    Weight    Cost    Scenario
  -------------------------------------------
  **default**              0.00     1.00     0.00  func::ss_125c
  **async_default**        0.00     1.00     0.00  func::ss_125c
  **clock_gating_default** 0.00     1.00     0.00  func::ss_125c
  **in2reg_default**       0.00     0.10     0.00  func::ss_125c
  **reg2out_default**      0.00     0.10     0.00  func::ss_125c
  **in2out_default**       0.00     0.10     0.00  func::ss_125c
  router_clock             0.00     1.00     0.00  func::ss_125c
  -------------------------------------------
  min_delay/hold                          0.00

                                  Weighted
  Group (max_delay/setup)    Cost    Weight    Cost    Scenario
  ___________________________________________
  **default**              0.00     1.00     0.00  func::ss_125c
  **async_default**        0.00     1.00     0.00  func::ss_125c
  **clock_gating_default** 0.00     1.00     0.00  func::ss_125c
  **in2reg_default**       0.00     0.10     0.00  func::ss_125c
  **reg2out_default**      0.00     0.10     0.00  func::ss_125c
  **in2out_default**       0.00     0.10     0.00  func::ss_125c
  router_clock             0.00     1.00     0.00  func::ss_125c
  -------------------------------------------
  max_delay/setup                         0.00

  Constraint                         Cost
  -----------------------------------
  min_delay/hold                      0.00  (MET)
  max_delay/setup                     0.00  (MET)
  max_transition                      0.00  (MET)
  max_capacitance                     0.00  (MET)
  min_capacitance                     0.00  (MET)
1
```

Report global timing

```
****************************************
Report : global timing
        -format { narrow }
        -pba_mode path
Design : router_top
Version: U-2022.12-SP6
Date   : Sun Aug 12 16:15:50 2024
****************************************

No setup violations found.
No hold violations found.
```

Report congestion

```
****************************************
Report : congestion
Design : router_top
Version: U-2022.12-SP6
Date   : Wed Aug 10 12:38:10 2024
****************************************

Layer     |    overflow     |            # GRCs has
Name      | total  |  max  | overflow (%)      | max overflow
------------------------------------------------------------
Both Dirs |      27 |     6 |      19  ( 0.12%) |       1
H routing |      18 |     2 |      17  ( 0.22%) |       1
V routing |       9 |     6 |       2  ( 0.03%) |       1

1
```

Report utilization

```
****************************************
Report : report_utilization
Design : router_top
Version: U-2022.12-SP6
Date   : Wed Aug 10 12:34:56 2024
****************************************
Utilization Ratio:                          0.7078
```

Utilization options:
- Area calculation based on: site_row of block ORCA_TOP/route_opt
-Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area: 9539.5492
Total Capacity Area: 9539.5492
Total Area of cells: 6752.0978
Area of excluded objects:
- hard_macros : 0.0000
- macro_keepouts : 0.0000
- soft_macros : 0.0000
- io_cells : 0.0000
- hard_blockages : 0.0000
Total Area of excluded objects: 0.0000
Ratio of excluded objects: 0.0000

Utilization of site-rows with:
- Site 'unit': 0.7078

0.7078

Check_routes

Information: The command 'check_routes' cleared the undo history. (UNDO-016)
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = M5
Found antenna rule mode 4, diode mode 2:
layer M1: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M2: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M3: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M4: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M5: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M6: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M7: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M8: max ratio 1000, diode ratio {0.06 0 400 40000}
layer M9: max ratio 1000, diode ratio {0.06 0 8000 50000}
layer MRDL: max ratio 1000, diode ratio {0 0 1 0 0}
layer CO: , diode ratio {0 0 1 0 0}
layer VIA1: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA2: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA3: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA4: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA5: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA6: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA7: max ratio 20, diode ratio {0.06 0 200 1000}
layer VIA8: max ratio 20, diode ratio {0.06 0 200 1000}

layer VIARDL: max ratio 20, diode ratio {0 0 1 0 0}
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer CO. (ZRT-022)
Warning: Ignore 2 top cell ports with no pins. (ZRT-027)
Skipping 1 internal pins that are not physical. Set route.common.verbose_level to > 0 and run routing command to get skipped pin names.
Info: number of net_type_blockage: 0
Information: Via ladder engine would be activated for pattern must join connection in certain commands. Please refer to man-page for the command list. (ZRT-619)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 5.32 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 5.32 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)

Start checking for open nets ...

Total number of nets = 1361, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen

Check 1361 nets, 0 have Errors

[CHECK OPEN NETS] Elapsed real time: 0:00:00
[CHECK OPEN NETS] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[CHECK OPEN NETS] Stage (MB): Used 0 Alloctr 0 Proc 0
[CHECK OPEN NETS] Total (MB): Used 27 Alloctr 27 Proc 9109
Printing options for 'route.common.*'
common.eco_route_fix_existing_drc : true
common.verbose_level : 0

Printing options for 'route.detail.*'
detail.antenna : true
detail.eco_route_use_soft_spacing_for_timing_optimization: false
detail.force_max_number_iterations : false
detail.timing_driven : true

Printing options for 'route.auto_via_ladder.*'

*****Start reporting antenna related parameters*****
Antenna/diode mode:
Antenna mode 4; diode mode 2
Metal lay (M1)0; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)

Cut lay (VIA1)1; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M2)1; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA2)2; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M3)2; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA3)3; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M4)3; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA4)4; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M5)4; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA5)5; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M6)5; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA6)6; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M7)6; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA7)7; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M8)7; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 400.000 40000.000 0.000)
Cut lay (VIA8)8; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 200.000 1000.000 0.000)
Metal lay (M9)8; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.060 0.000 8000.000 50000.000 0.000)
Cut lay (VIARDL)9; maxRatio 20.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.000 0.000 1.000 0.000 0.000)
Metal lay (MRDL)9; maxRatio 1000.000 maxPRatio 2147483648.000 maxNRatio 2147483648.000; vector (0.000 0.000 1.000 0.000 0.000)
Top lay antenna ratio fix threshold == -1
Antenna max pin count threshold == -1
Check PG net == false
MergeGate == true
Break antenna to port mode == float
Break antenna to macro pin mode == normal
*****End reporting antenna related parameters*****
Warning: Skipping antenna analysis for net data_in[7]. The pin data_in[7] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[6]. The pin data_in[6] on cell ORCA_TOP

does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[5]. The pin data_in[5] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[4]. The pin data_in[4] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[3]. The pin data_in[3] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[2]. The pin data_in[2] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[1]. The pin data_in[1] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net data_in[0]. The pin data_in[0] on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net clock. The pin clock on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net resetn. The pin resetn on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net read_enb_0. The pin read_enb_0 on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net read_enb_1. The pin read_enb_1 on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net read_enb_2. The pin read_enb_2 on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Warning: Skipping antenna analysis for net pkt_valid. The pin pkt_valid on cell ORCA_TOP does not have enough gate area information. (ZRT-311)
Skipping antenna analysis for 14 nets as they don't have enough gate area info.

Begin full DRC check ...

Information: Using 1 threads for routing. (ZRT-444)
Checked 1/6 Partitions, Violations = 0
Checked 2/6 Partitions, Violations = 0
Checked 3/6 Partitions, Violations = 0
Checked 4/6 Partitions, Violations = 0
Checked 5/6 Partitions, Violations = 0
Checked 6/6 Partitions, Violations = 0
[DRC CHECK] Elapsed real time: 0:00:02
[DRC CHECK] Elapsed cpu time: sys=0:00:00 usr=0:00:02 total=0:00:02
[DRC CHECK] Stage (MB): Used 0 Alloctr 0 Proc 0
[DRC CHECK] Total (MB): Used 97 Alloctr 98 Proc 9109
Start net based rule analysis
Found 0 antenna instance ports
End net based rule analysis
[Antenna analysis] Elapsed real time: 0:00:00
[Antenna analysis] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Antenna analysis] Stage (MB): Used 0 Alloctr 0 Proc 0

[Antenna analysis] Total (MB): Used 98 Alloctr 99 Proc 9109

DRC-SUMMARY:
@@@@@@@ TOTAL VIOLATIONS = 0

Total Wire Length = 28478 micron
Total Number of Contacts = 12282
Total Number of Wires = 12246
Total Number of PtConns = 1880
Total Number of Routed Wires = 12209
Total Routed Wire Length = 28284 micron
Total Number of Routed Contacts = 12282
Layer M1 : 1037 micron
Layer M2 : 11954 micron
Layer M3 : 10281 micron
Layer M4 : 2801 micron
Layer M5 : 2210 micron
Layer M6 : 0 micron
Layer M7 : 0 micron
Layer M8 : 0 micron
Layer M9 : 0 micron
Layer MRDL : 0 micron
Via VIA45SQ_C(rot) : 246
Via VIA34SQ_C : 1002
Via VIA34SQ_C(rot) : 3
Via VIA23SQ_C : 25
Via VIA23SQ_C(rot) : 4948
Via VIA12SQ_C : 5915
Via VIA12SQ_C(rot) : 110
Via VIA12BAR_C : 26
Via VIA12BAR(rot) : 1
Via VIA12SQ_C_2x1 : 6

Redundant via conversion report:
- - - - - - - - - - - - - - - - - - - -

Total optimized via conversion rate = 0.05% (6 / 12282 vias)

Layer VIA1 = 0.10% (6 / 6058 vias)
Weight 1 = 0.10% (6 vias)
Un-optimized = 0.00% (0 vias)
Un-mapped = 99.90% (6052 vias)
Layer VIA2 = 0.00% (0 / 4973 vias)
Un-optimized = 0.00% (0 vias)

```
    Un-mapped    = 100.00% (4973    vias)
  Layer VIA3     =  0.00% (0      / 1005    vias)
    Un-optimized =  0.00% (0       vias)
    Un-mapped    = 100.00% (1005    vias)
  Layer VIA4     =  0.00% (0      / 246     vias)
    Un-optimized =  0.00% (0       vias)
    Un-mapped    = 100.00% (246     vias)

 Total double via conversion rate    =  0.05% (6 / 12282 vias)

  Layer VIA1     =  0.10% (6      / 6058    vias)
  Layer VIA2     =  0.00% (0      / 4973    vias)
  Layer VIA3     =  0.00% (0      / 1005    vias)
  Layer VIA4     =  0.00% (0      / 246     vias)

 The optimized via conversion rate based on total routed via count =  0.05% (6 / 12282 vias)

  Layer VIA1     =  0.10% (6      / 6058    vias)
    Weight 1     =  0.10% (6       vias)
    Un-optimized =  0.00% (0       vias)
    Un-mapped    = 99.90% (6052    vias)
  Layer VIA2     =  0.00% (0      / 4973    vias)
    Un-optimized =  0.00% (0       vias)
    Un-mapped    = 100.00% (4973    vias)
  Layer VIA3     =  0.00% (0      / 1005    vias)
    Un-optimized =  0.00% (0       vias)
    Un-mapped    = 100.00% (1005    vias)
  Layer VIA4     =  0.00% (0      / 246     vias)
    Un-optimized =  0.00% (0       vias)
    Un-mapped    = 100.00% (246     vias)
```

Verify Summary:

```
Total number of nets = 1361, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = 0
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked
```

Report_qor -summary

```
****************************************
Report : qor
        -summary
        -pba_mode path
Design : router_top
Version: U-2022.12-SP6
Date   : Wed Aug10 12:32:23 2024
****************************************
Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis, AWP, PBA Mode Path'. (TIM-050)

Timing

---------------------------------------------------------------
Context                    WNS         TNS         NVE
---------------------------------------------------------------
func::ss_125c      (Setup)        7.41        0.00          0
Design             (Setup)        7.41        0.00          0

func::ss_125c      (Hold)         0.15        0.00          0
Design             (Hold)         0.15        0.00          0
---------------------------------------------------------------

Miscellaneous

---------------------------------------------------------------
Cell Area (netlist):                        6752.10
Cell Area (netlist and physical only):      9539.55
Nets with DRC Violations:       0
1
```

Report_power

```
****************************************
Report : power
        -significant_digits 2
Design : router_top
Version: U-2022.12-SP6
Date   : Wed  Aug 10 12:38:50 2024
****************************************
Information: Activity propagation will be performed for scenario func::ss_125c.
Information: Doing activity propagation for mode 'func' and corner 'ss_125c' with effort level 'medium'. (POW-024)
Information: Timer-derived activity data is cached on scenario func::ss_125c (POW-052)
```

Infomation: Fast mode activity propagation power.rtl_activity_annotation setup is ignored. Always use accurate mode.
Information: Running switching activity propagation in scalar mode!

**** Information : No. of simulation cycles = 6 ****
Mode: func
Corner: ss_125c
Scenario: func::ss_125c
Voltage: 0.95
Temperature: 125.00

Voltage Unit : 1V
Capacitance Unit : 1fF
Time Unit : 1ns
Temperature Unit : 1C
Dynamic Power Unit : 1pW
Leakage Power Unit : 1pW

Switched supply net power scaling:
scaling for leakage power

Supply nets:
VDD (power) probability 1.00 (default)
VSS (ground) probability 1.00 (default)
Warning: Power table extrapolation (extrapolation mode) for port D on cell register/dout_reg[6] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.067463 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port CLK on cell register/dout_reg[6] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.073147 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell register/dout_reg[6] for parameter Cout. Lowest table value = 0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell synchronizer/address_reg[0] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.044937 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port CLK on cell synchronizer/address_reg[0] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.083256 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell register/dout_reg[4] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.067444 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port CLK on cell register/dout_reg[4] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.073147 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell

register/dout_reg[4] for parameter Cout. Lowest table value = 0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell synchronizer/count_0_reg[4] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.051517 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port CLK on cell synchronizer/count_0_reg[4] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.055084 (POW-046)
Note - message 'POW-046' limit (10) exceeded. Remainder will be suppressed.

Cell Internal Power = 2.73e+08 pW (85.7%)
Net Switching Power = 4.56e+07 pW (14.3%)
Total Dynamic Power = 3.19e+08 pW (100.0%)

Cell Leakage Power = 3.10e+08 pW

Attributes
---

u - User defined power group
i - Includes clock pin internal power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00 (0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00 (0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00 (0.0%)	
clock_network	2.19e+08	3.99e+07	1.02e+07	2.69e+08 (42.8%)	i
register	5.05e+07	1.21e+06	2.76e+08	3.28e+08 (52.1%)	
sequential	0.00e+00	0.00e+00	0.00e+00	0.00e+00 (0.0%)	
combinational	3.52e+06	4.47e+06	2.45e+07	3.24e+07 (5.2%)	
Total	2.73e+08 pW	4.56e+07 pW	3.10e+08 pW	6.29e+08 pW	1

Check_lvs

Information: Using 1 threads for LVS
[Check Short] Stage 1 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 1-2 Elapsed = 0:00:00, CPU = 0:00:00

```
[Check Short] Stage 2 Elapsed =    0:00:00, CPU =    0:00:00
[Check Short] Stage 2-2       Elapsed =    0:00:01, CPU =    0:00:01
[Check Short] Stage 3 Elapsed =    0:00:01, CPU =    0:00:01
[Check Short] End     Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] Init      Elapsed =    0:00:01, CPU =    0:00:01
Warning: Port VSS have no valid pin shapes. Skip this port. (RT-203)
Warning: Port VDD have no valid pin shapes. Skip this port. (RT-203)
[Check Net] 10%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 20%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 30%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 40%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 50%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 60%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 70%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 80%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] 90%       Elapsed =    0:00:01, CPU =    0:00:01
[Check Net] All nets are submitted.
[Check Net] 100%      Elapsed =    0:00:01, CPU =    0:00:01
Information: Detected open violation for Net VSS. BBox: (20.0000 20.2490)(144.0320
112.0150). (RT-585)
Information: Detected open violation for Net VDD. BBox: (20.0000 19.9700)(144.0320
110.9410). (RT-585)

============================================================
   Maximum number of violations is set to 20
   Abort checking when more than 20 violations are found
   All violations might not be found.
============================================================
Total number of input nets is 1361.
Total number of short violations is 0.
Total number of open nets is 2.
Open nets are VDD VSS
Total number of floating route violations is 0.

Elapsed =    0:00:01, CPU =    0:00:01
1
```

Final sdc

```
################################################################################
##
#
# Design name: ORCA_TOP
#
# Created by fc write_sdc on Wed Jan 24 13:25:46 2024
```

```
#
################################################################################
##

set sdc_version 2.1
set_units -time ns -resistance MOhm -capacitance fF -voltage V -current uA

################################################################################
##
#
# Units
# time_unit              : 1e-09
# resistance_unit        : 1000000
# capacitive_load_unit   : 1e-15
# voltage_unit           : 1
#  current_unit          : 1e-06
# power_unit             : 1e-12
################################################################################
##


# Mode: func
# Corner: ss_125c
# Scenario: func::ss_125c

# /tmp/fc_shell-be-2.LEVyeA, line 1
create_clock -name router_clock -period 10 -waveform {0 5} [get_ports {clock}]
set_propagated_clock [get_clocks {router_clock}]
#
/home/BPD19/S_Padmaja/VLSI_PD/Fusion_compiler_labs/FC_LABS/Router/scripts/mcmm_ro
ut  er_top.tcl, \
#  line 9
set_voltage 0.95 -object_list {VDD}
#
/home/BPD19/S_Padmaja/VLSI_PD/Fusion_compiler_labs/FC_LABS/Router/scripts/mcmm_ro
ut  er_top.tcl, \
#  line 10
set_voltage 0 -object_list {VSS}
# Warning: Libcell power domain derates are skipped!

# Set latency for io paths.
# -origin user
set_clock_latency -min 0.255508 [get_clocks {router_clock}]
# -origin user
set_clock_latency -max 0.266056 [get_clocks {router_clock}]
# Set propagated on clock sources to avoid removing latency for IO paths.
```

```
set_propagated_clock [get_ports {clock}]
set_clock_transition 0.0997375 [get_clocks {router_clock}]
```