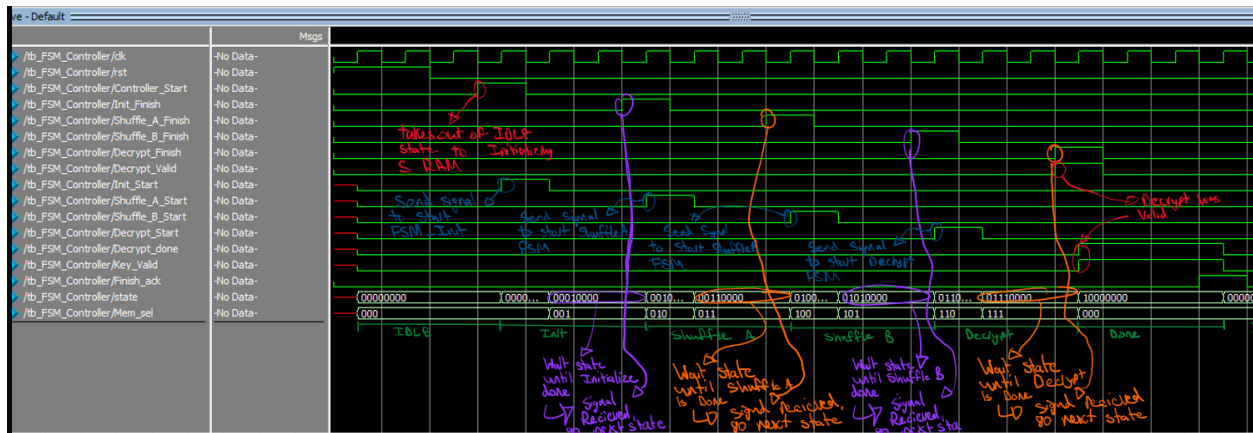
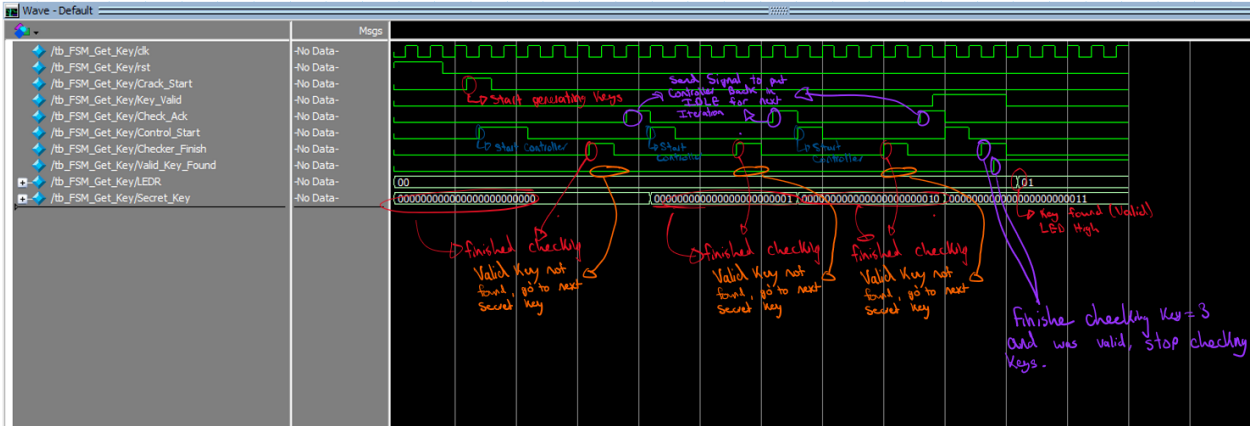


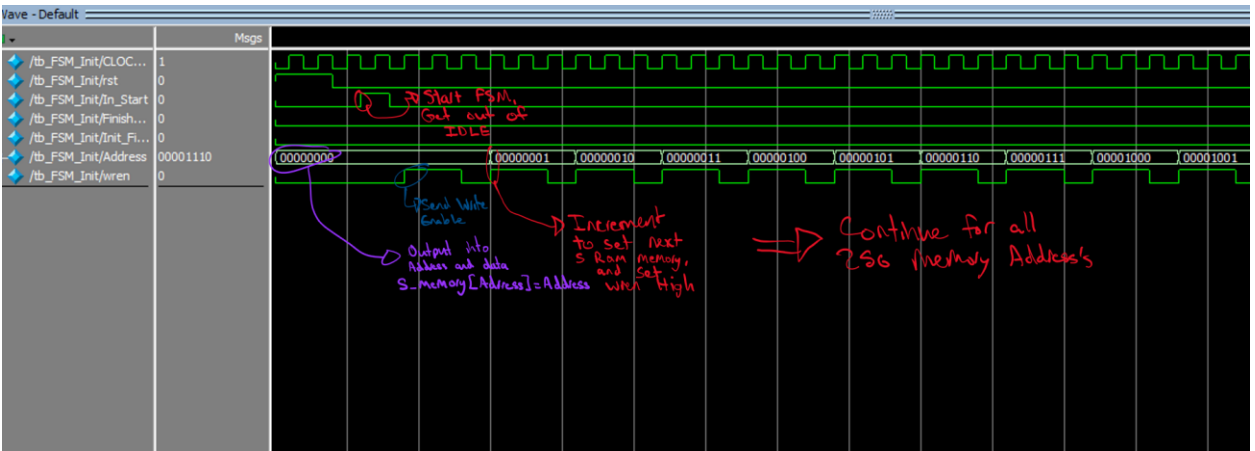
- FSM\_Checker:



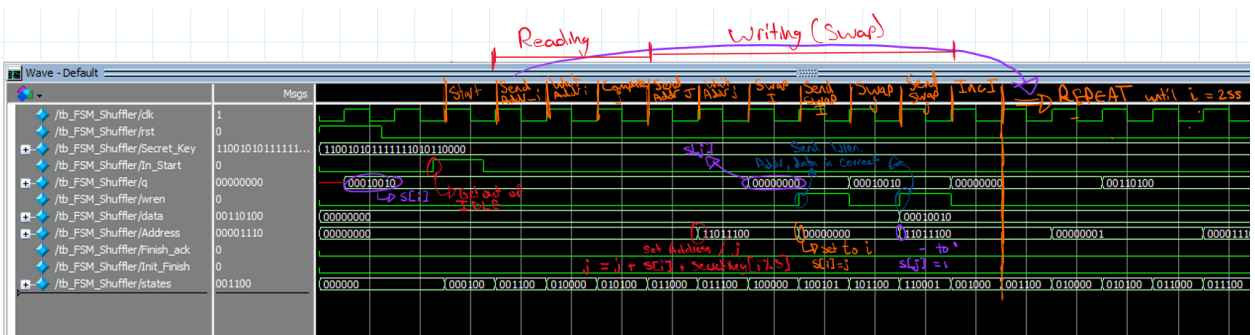
### FSM\_Get\_Key:



## FSM\_Init:



### FSM\_Shuffler:



[illegible]

Wave - Default

Msgs

/tb\_FSM\_Start/clock  
 /tb\_FSM\_Start/reset  
 /tb\_FSM\_Start/start

-No Data-  
 -No Data-  
 -No Data-

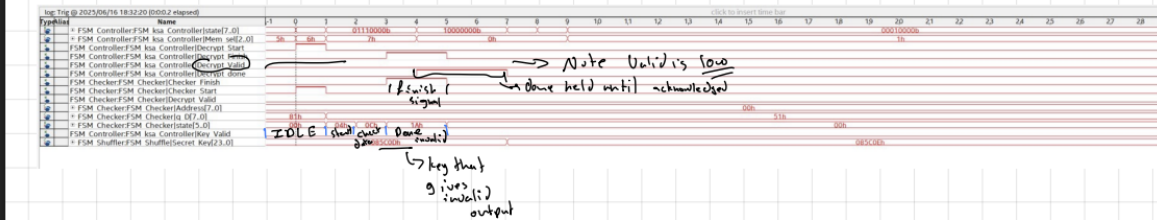
initial Reset  
 send start pulse  
 Continue to output 0 for lifetime

IDLE  
 START  
 IDLE - START

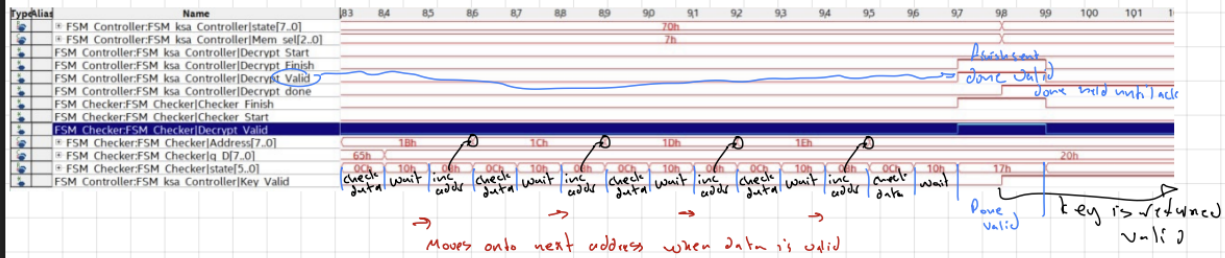
### FSM\_Checker:

## FSM-Checker (task 3)

fail



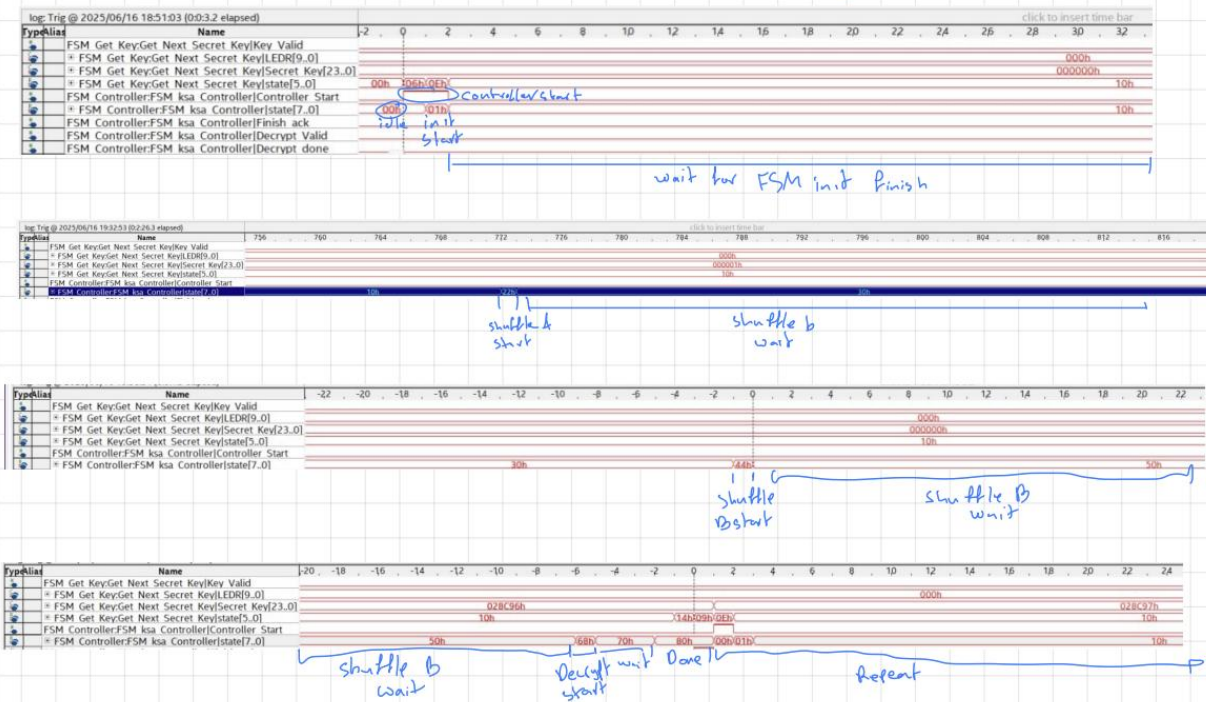
Pass



## FSM\_Controller:

fsm controller

Decrypt here  $\rightarrow$  checker



FSM\_Get\_key

log: Trig @ 2025/06/16 18:51:03 (00:3.2 elapsed)

click to insert time bar

Type	Alias	Name	Time	Source	Destination	Length	Info
129	FSM Get KeyGet Next Secret KeyKey Valid	FSM Get KeyGet Next Secret KeyKeyValid	0.000000	192.168.1.100	192.168.1.101	100	00000000 00000000
130	FSM ControllerFSM ksa ControllerController Start	FSM ControllerFSM ksa ControllerControllerStart	0.000000	192.168.1.101	192.168.1.100	100	00000000 00000000

Sends key to controller and waits for it to finish

Key increments

Controller finishes next key found

[illegible]



[illegible]

5.

Simulation files can be found under **rtl\<FSM Name>\** labelled as: **tb\_<FSM NAME>.sv**

These are testbench Verilog files that are built and ran on **Modelsim – Intel FPGA 10.5b**

6.

Task3 SOF is also available under **rtl\template\_de1soc\output\_files\rc4\_Task3.sof**