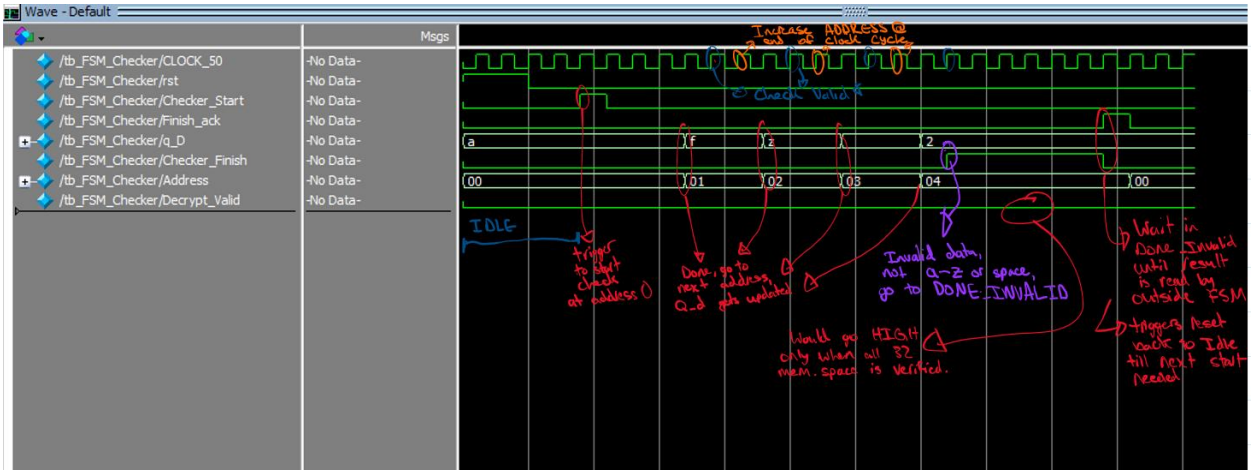
1. SOF Directory Location: **\rtl\template_de1soc\output_files\rc4.sof**

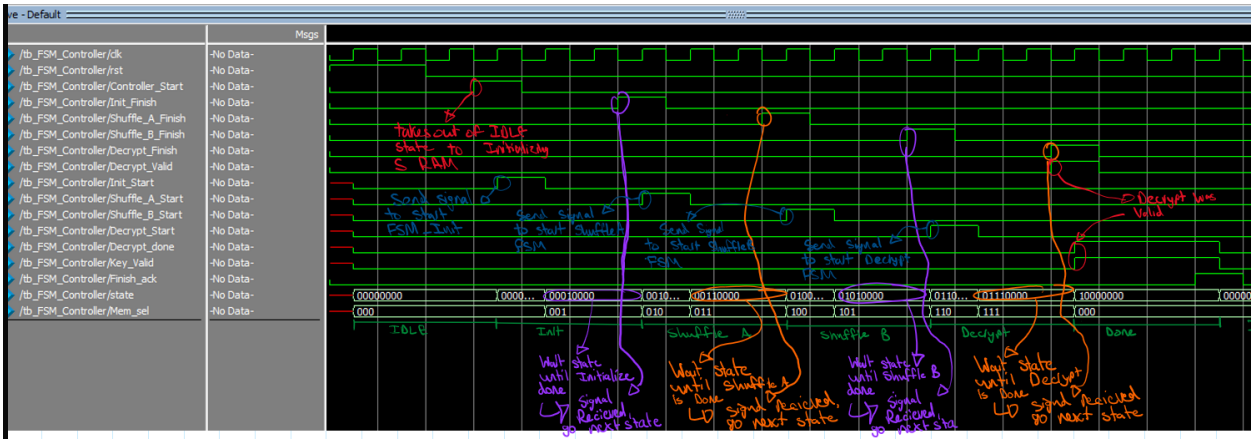
2. Lab is fully complete with Bonus

3. Simulation

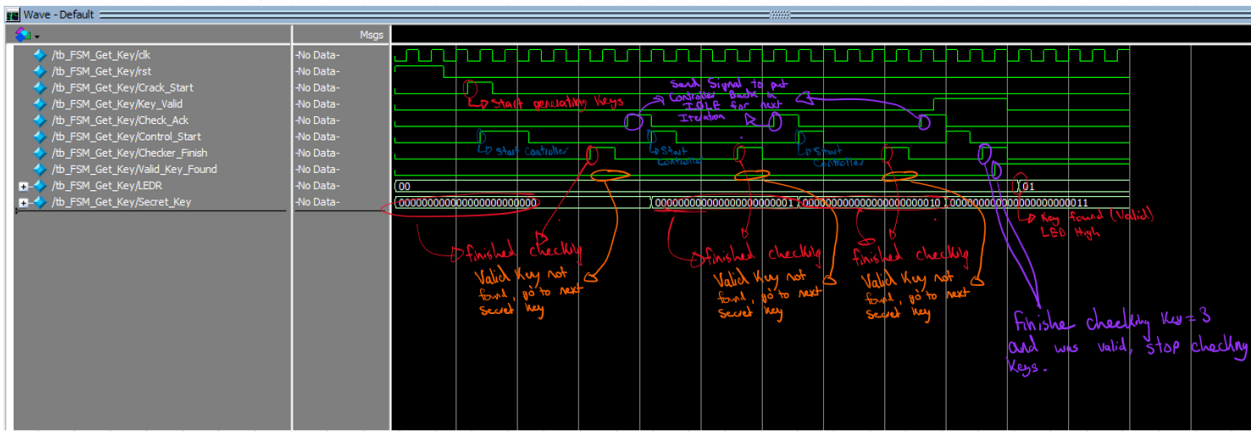
FSM_Checker:



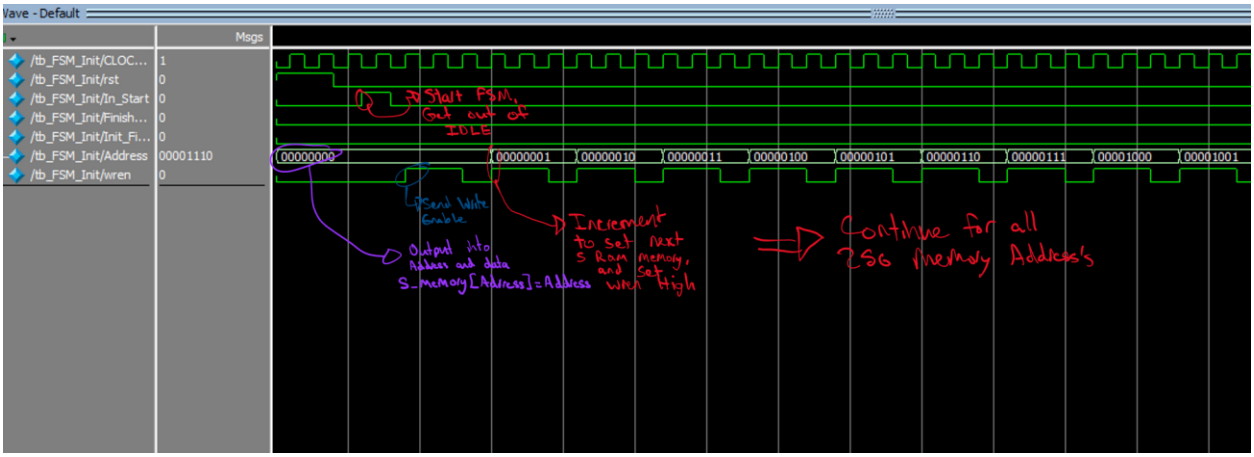
FSM_Controller:



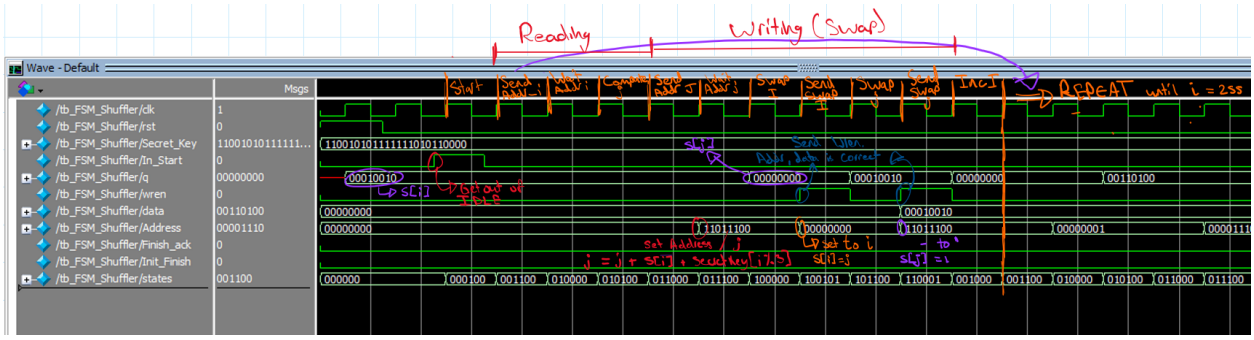
FSM_Get_Key:



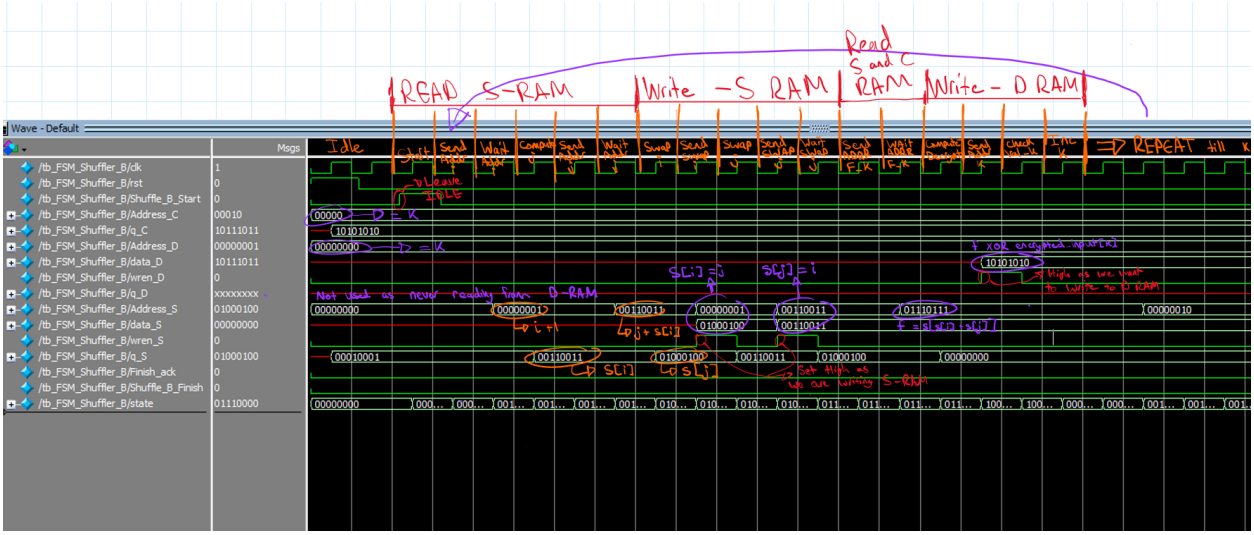
FSM_Init:



FSM_Shuffler:



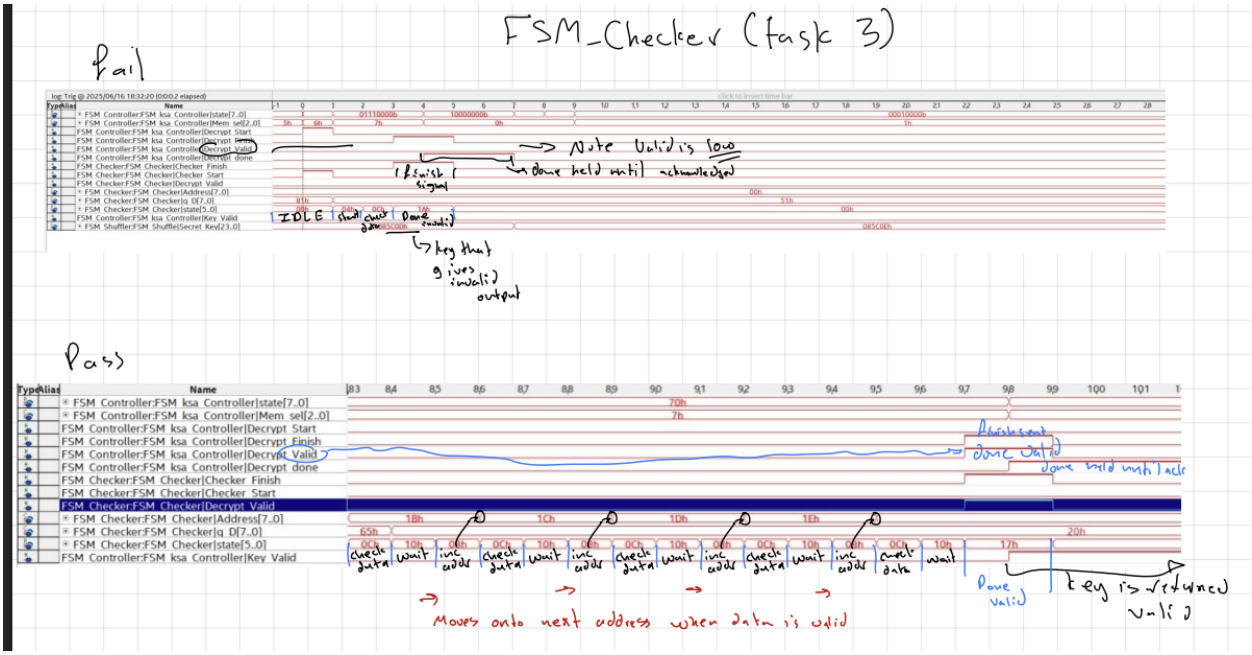
FSM_Shuffler_B:



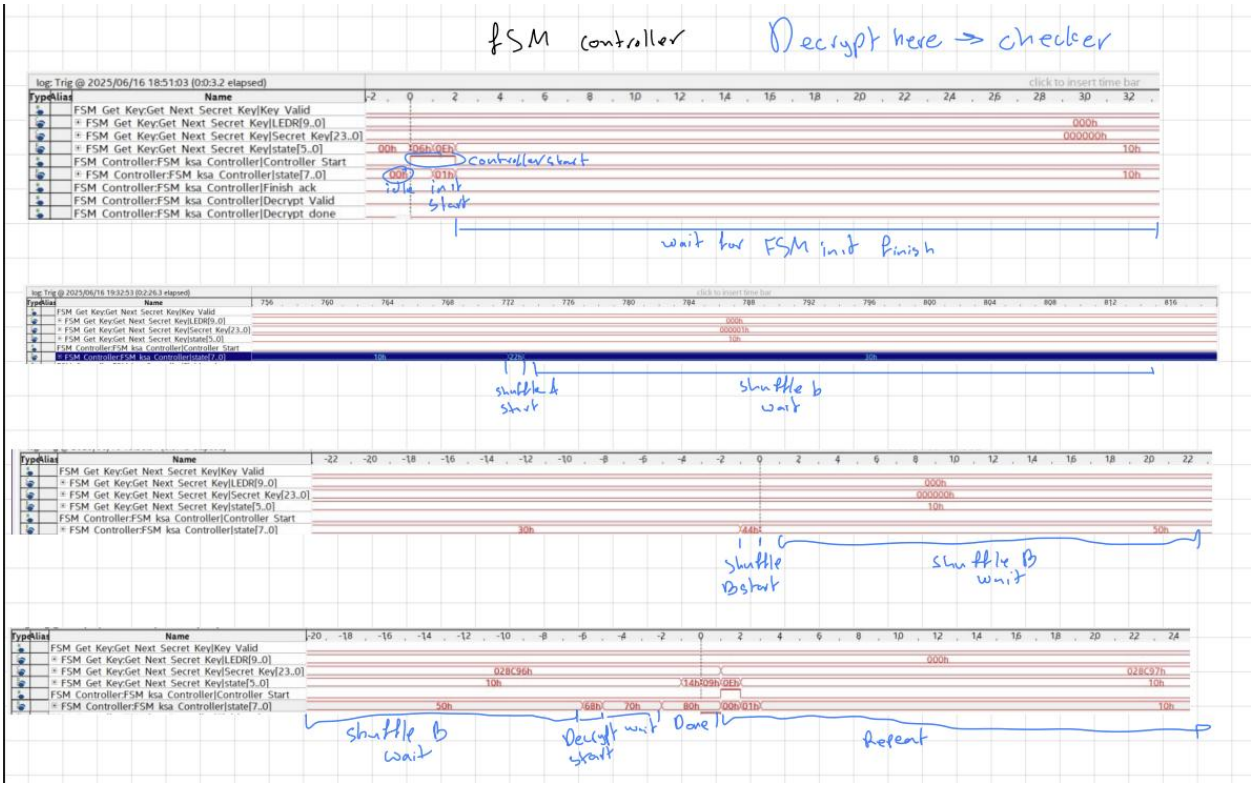
FSM_Start:

4. SignalTap

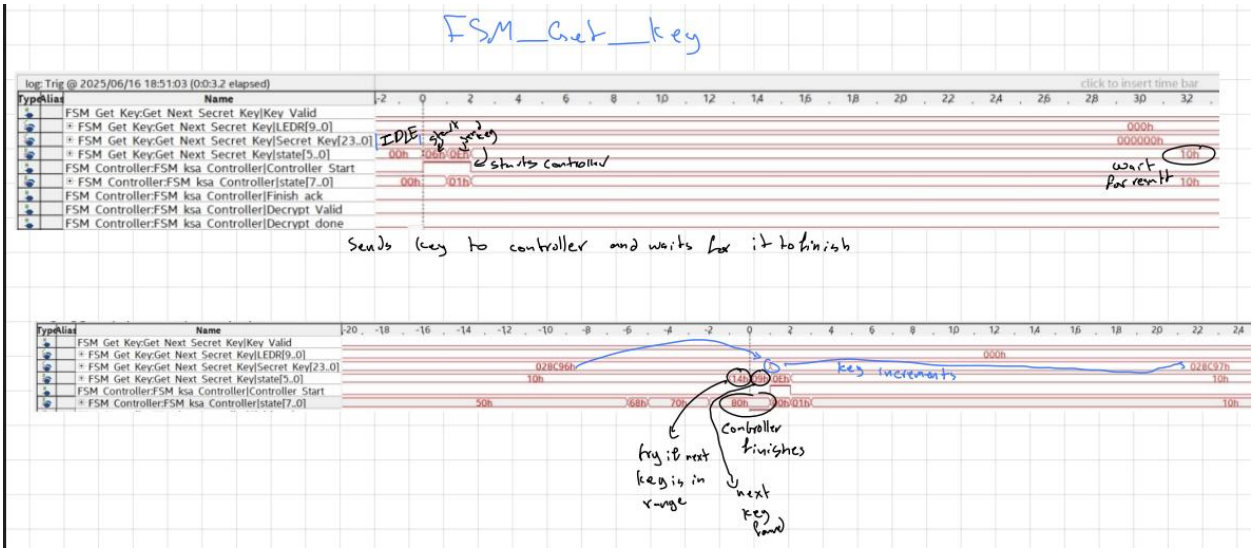
FSM_Checker:



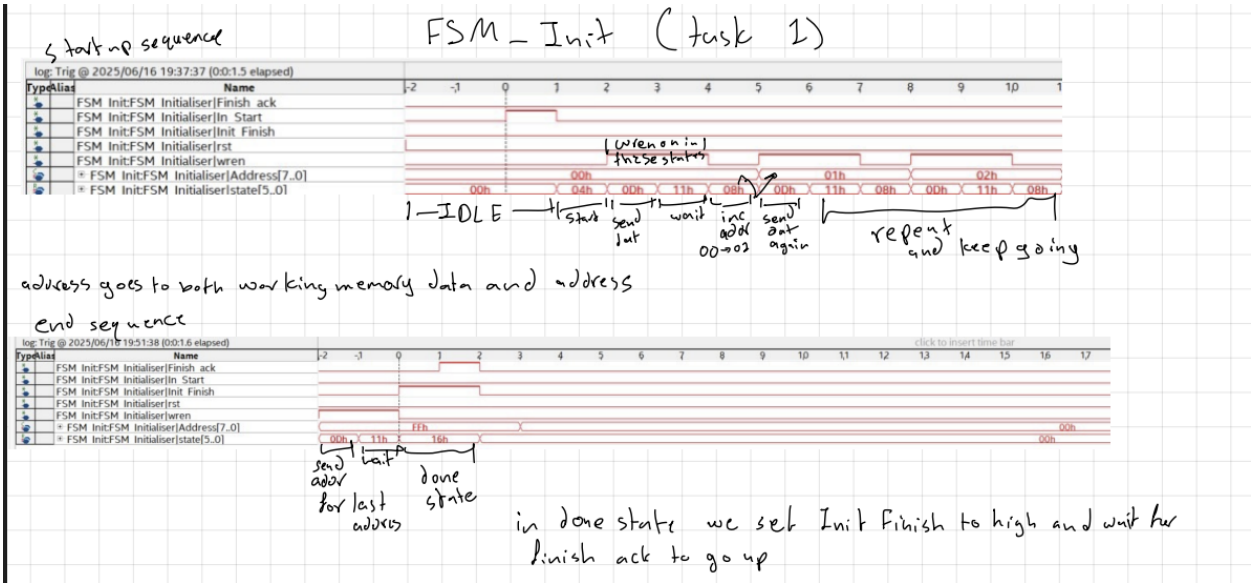
FSM_Controller:



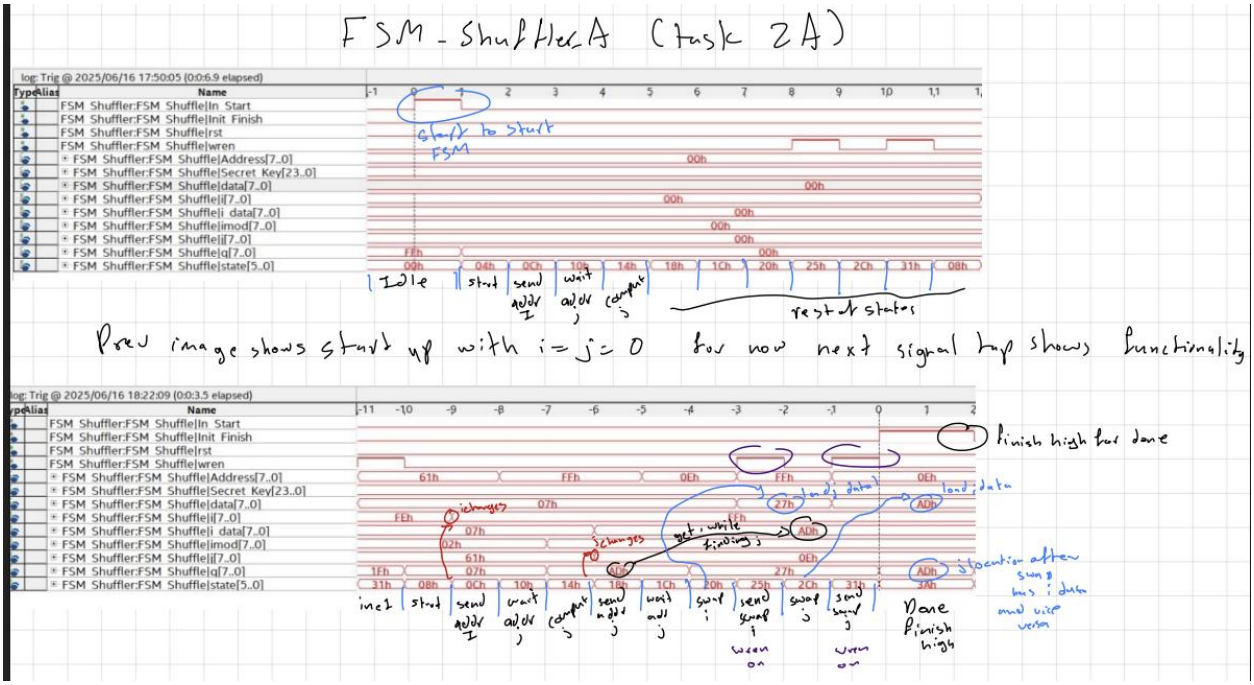
FSM_Get_Key:



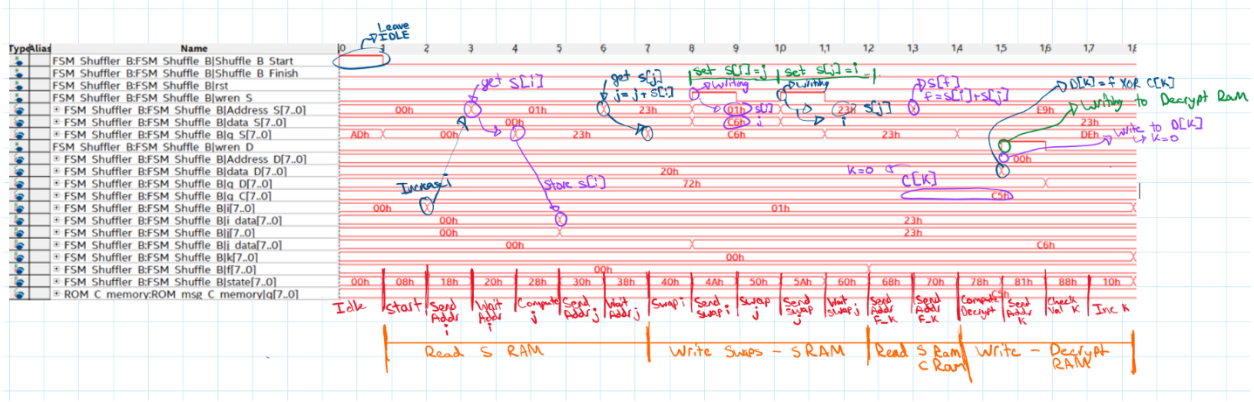
FSM_Init:

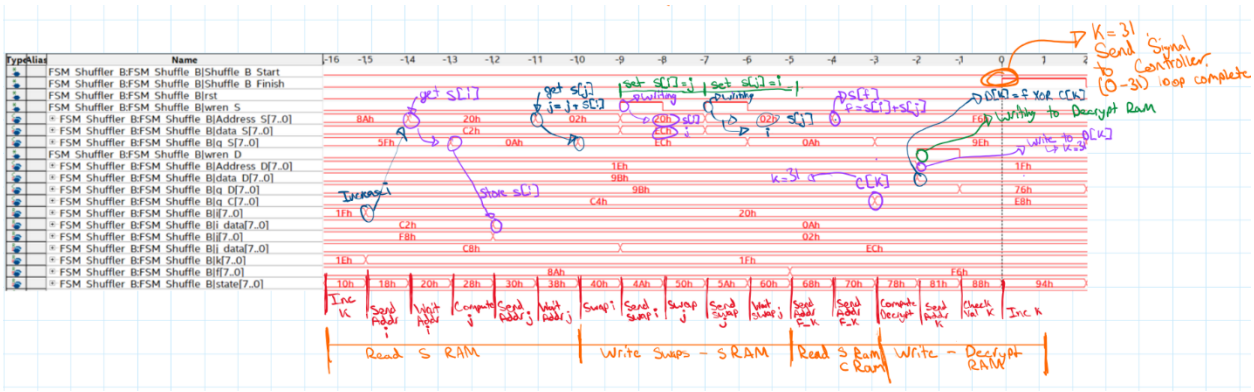


FSM_Shuffler:



FSM_Shuffler_B:





5.

Simulation files can be found under **rtl\<FSM Name>** labelled as: **tb_<FSM NAME>.sv**

These are testbench Verilog files that are built and ran on **Modelsim – Intel FPGA 10.5b**

6.

Task3 SOF is also available under **\rtl\template_de1soc\output_files\rc4_Task3.sof**