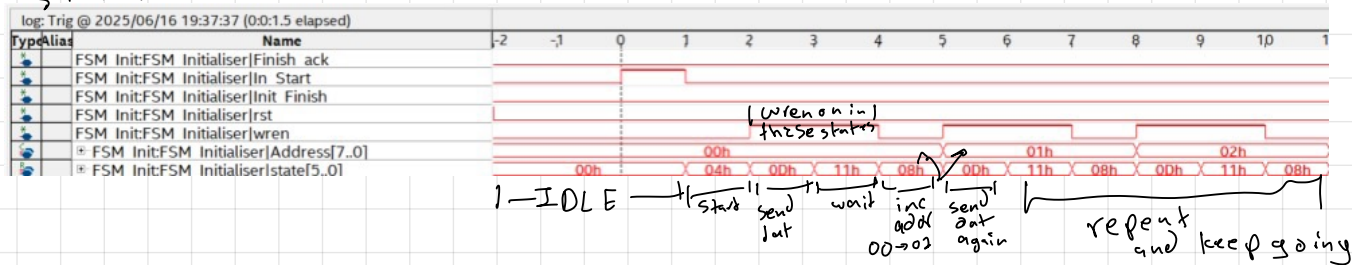


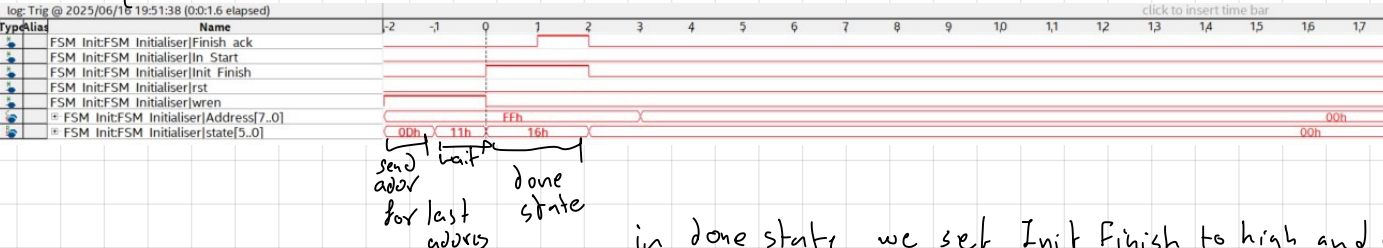
start up sequence

## FSM - Init (task 1)



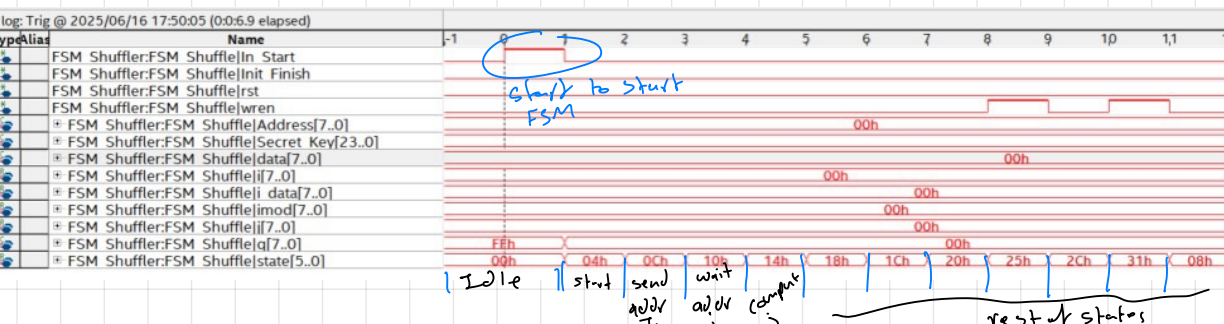
address goes to both working memory data and address

end sequence

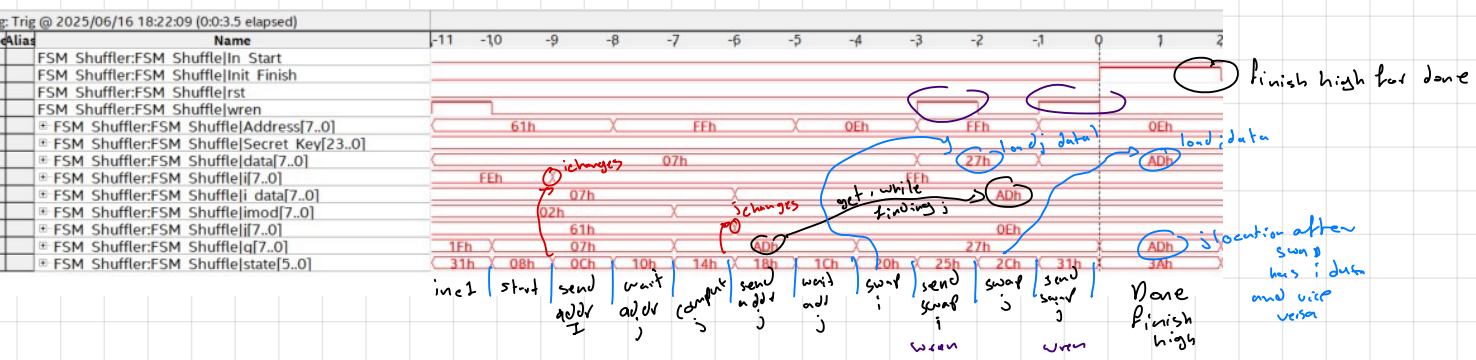


in done state we set Init Finish to high and wait for finish ack to go up

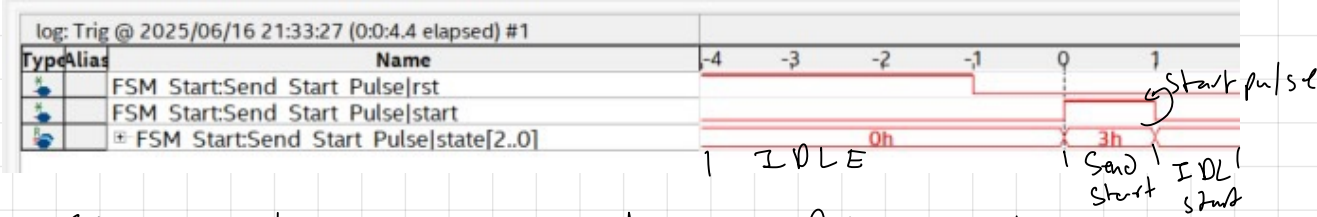
## FSM - Shuffler A (task 2A)



Prev image shows start up with  $i = j = 0$  for now next signal hup shows functionality



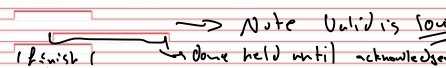
## FSM - Start



Starts the 4 instances of our RCU cracker

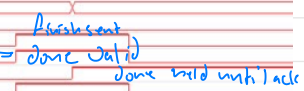
3 states

fail



↳ key that g gives invalid output

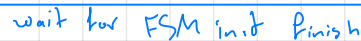
Pass)



→ Moves onto next address when data is valid

key is returned  
unless

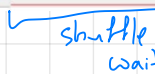
Decrypt here  $\rightarrow$  checker



shuttle bus  
wait



shuffle B  
wait

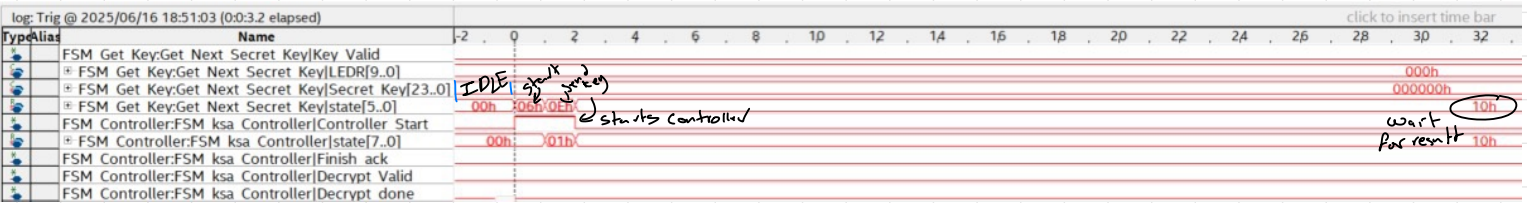


Deugt  
start

10

Repeat

# FSM\_Get\_Key



sends key to controller and waits for it to finish

