1. SOF Directory Location: **\rtl\template\_de1soc\output\_files\rc4.sof**

2. Lab is fully complete with Bonus

3. Simulation

FSM\_Checker:

A screenshot of a computer

AI-generated content may be incorrect.

FSM\_Controller: A computer screen shot of a black screen

AI-generated content may be incorrect.

FSM\_Get\_Key:A screen shot of a computer screen

AI-generated content may be incorrect.

FSM\_Init:  
A screen shot of a computer

AI-generated content may be incorrect.

FSM\_Shuffler:

A screen shot of a graph

AI-generated content may be incorrect.

FSM\_Shuffler\_B:

A black screen with colorful lines and text

AI-generated content may be incorrect.

4. SignalTap

5.

Simulation files can be found under **rtl\<FSM Name>\** labelled as: **tb\_<FSM NAME>.sv**

These are testbench Verilog files that are built and ran on **Modelsim – Intel FPGA 10.5b**