Project File:	STATE_MACHINE.xise	**Parser Errors:**	No Errors
Module Name:	STATE_MN	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.5	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	368	18,224	2%	
Number used as Flip Flops	366			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	2			
Number of Slice LUTs	1,179	9,112	12%	
Number used as logic	1,173	9,112	12%	
Number using O6 output only	988			
Number using O5 output only	15			
Number using O5 and O6	170			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	6			
Number with same-slice register load	5			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	451	2,278	19%	
Number of MUXCYs used	148	4,556	3%	
Number of LUT Flip Flop pairs used	1,303			
Number with an unused Flip Flop	942	1,303	72%	
Number with an unused LUT	124	1,303	9%	
Number of fully used LUT-FF pairs	237	1,303	18%	
Number of unique control sets	14			
Number of slice register sites lost to control set restrictions	58	18,224	1%	
Number of bonded IOBs	27	232	11%	
Number of LOCed IOBs	27	27	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	3	16	18%	
Number used as BUFGs	3			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.60			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		