Digital clock used components :

1 – 6 * 7448 ic

2 – 8 * 7490 ic

3 – 200 male to male wire

4 – 555 timer

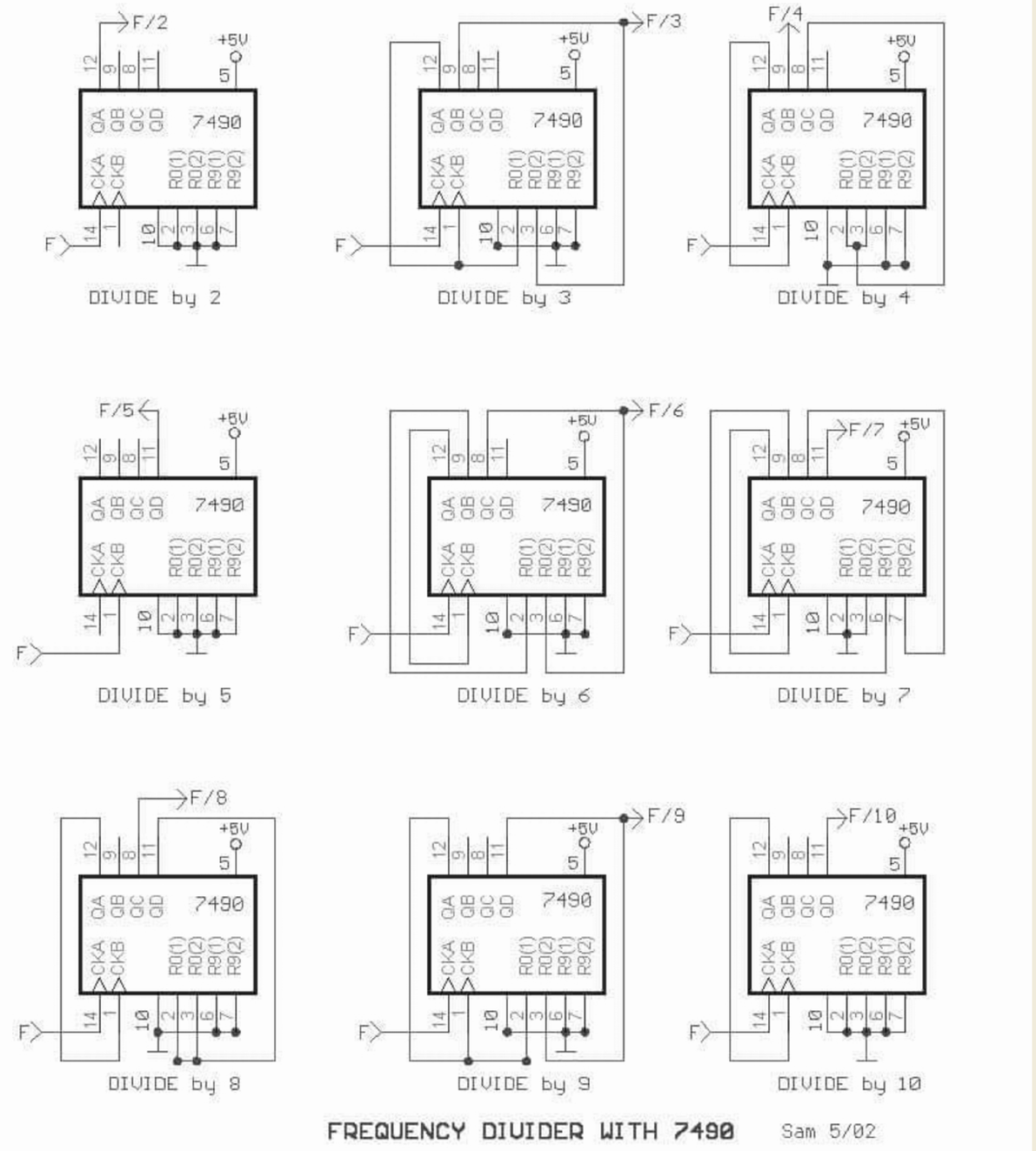
5- 2 * 10 micro farad capacitor

6- 4 * BreadBoard

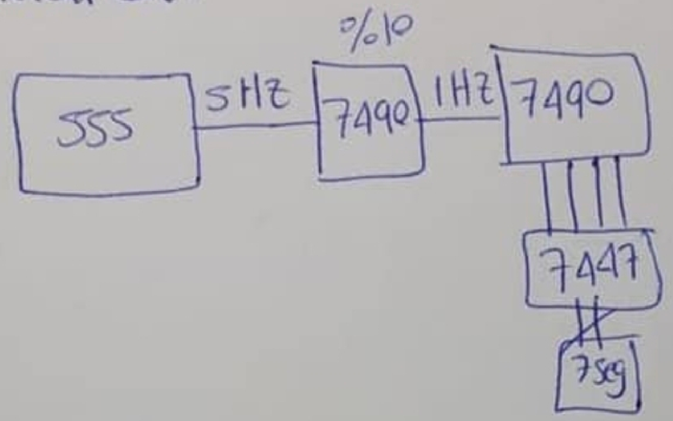
7- 6 * 7 segment cathode display

8- power supply

9 – 2 10k ohm resistors



Practical.

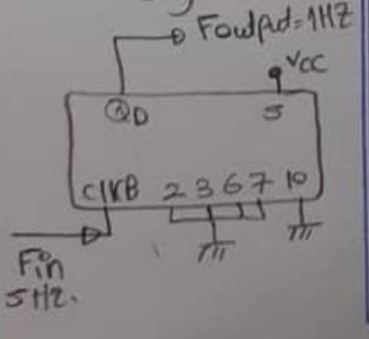


$R_1 = 88000$

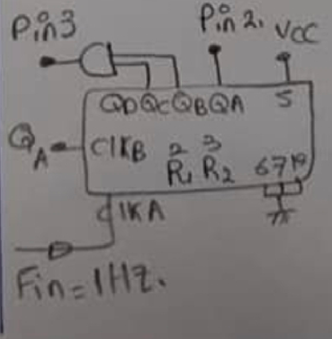
$R_2 = 100000$

$C = 1\mu F$ → 5Hz

1] divide by 5.



2] second Counter.

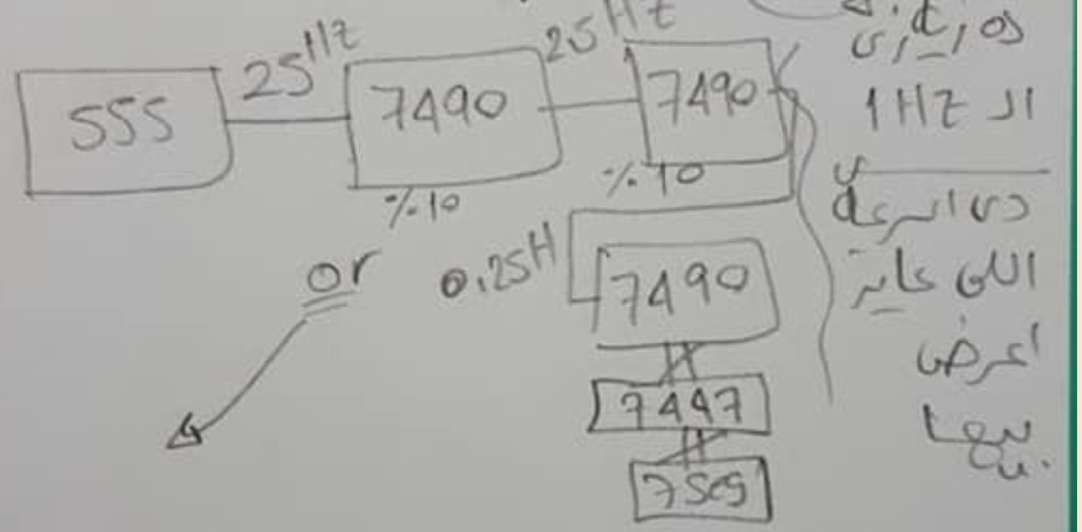


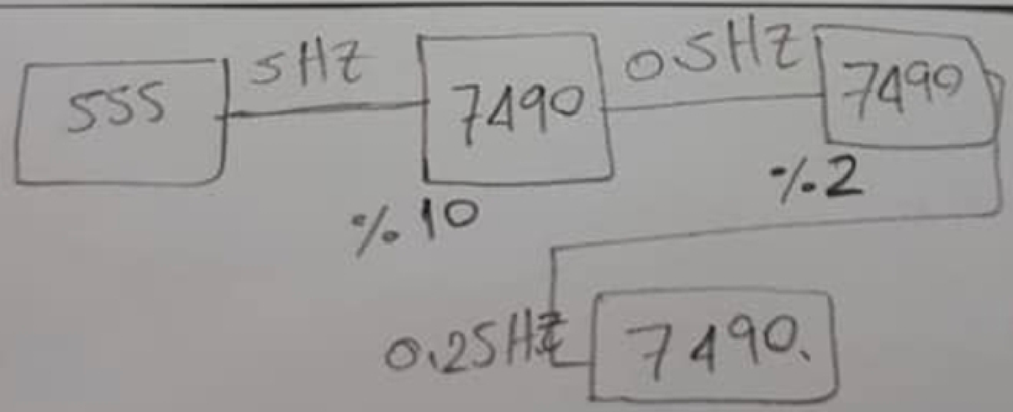
Count from 0 — 07

for 4sec

Sol

$$F = \frac{1}{T} = \frac{1}{4} = 0.25\ Hz.$$

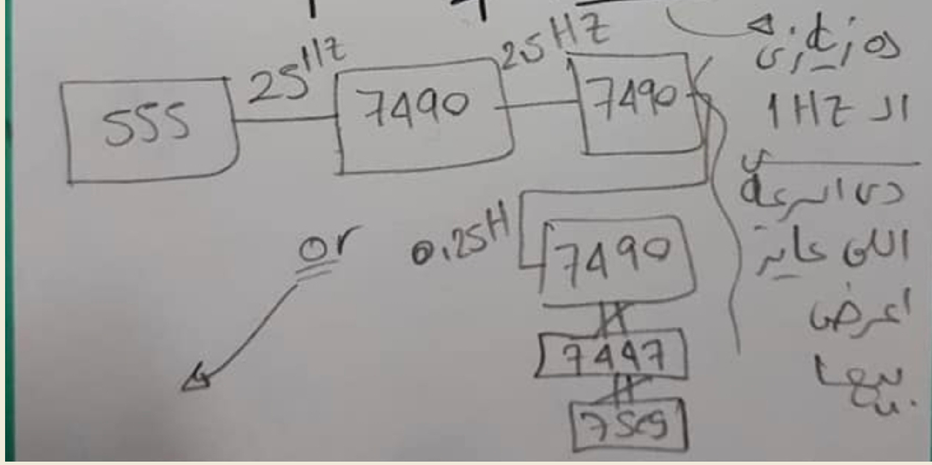


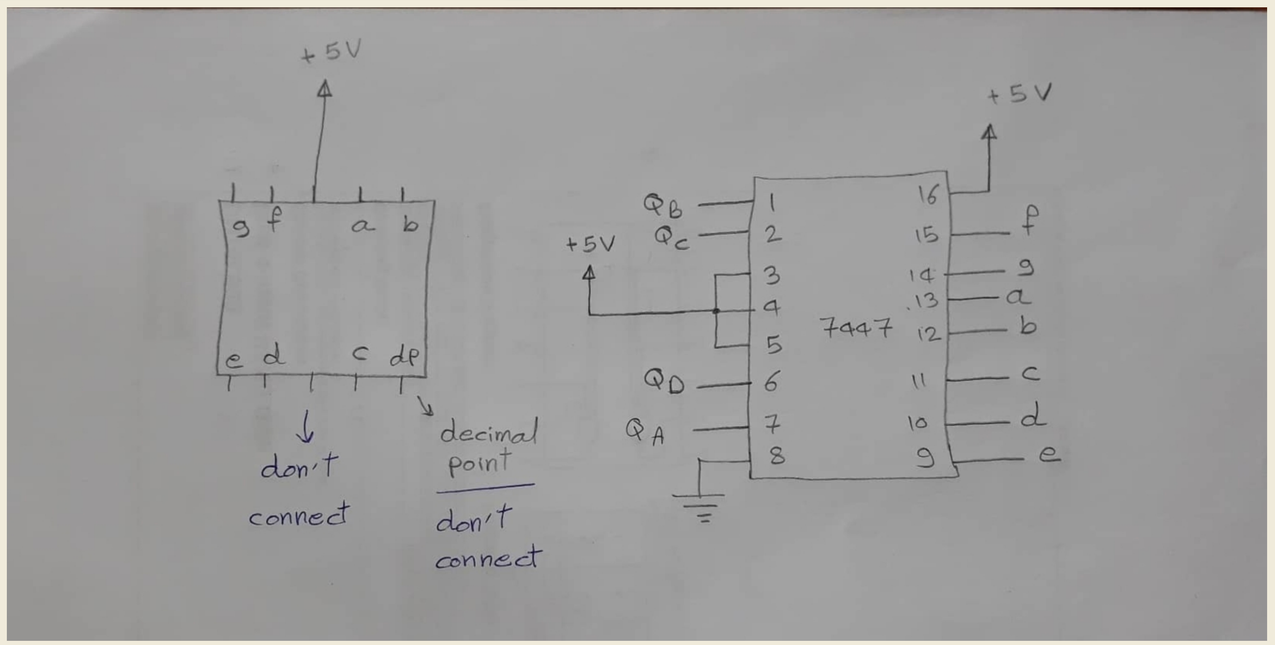


design a circuit to produce
Count from 0 → 7
for 4 sec

Sol

$$F = \frac{1}{T} = \frac{1}{4} = \boxed{0.25}\ Hz.$$





DEVICES

7SEG-COM-ANODE
74LS47
74LS90
555
3252W-1-101LF
3252W-1-501LF
7490
CAP
MINRES120K
POT
RES

Block Diagram

$$T = \frac{1}{f} \text{ Sec}$$

Counter

555 → 50 Hz → 7490 F/10 → 5 Hz → 7490 F/6 → 1 Hz → 7490 F/10 → $\frac{1}{10}$ Hz → 0→9

7490 F/6 → $\frac{1}{60}$ Hz → 0→5

59 sec

Astable timer

60 sec → $\frac{1}{60}$ Hz → 7490 F/10 → $\frac{1}{600}$ Hz → 7490 F/6 → $\frac{1}{3600}$ Hz → 7490 F/4 → 0→4

7490 F/2 → 0→2

gmin 0-9

5min 0→5

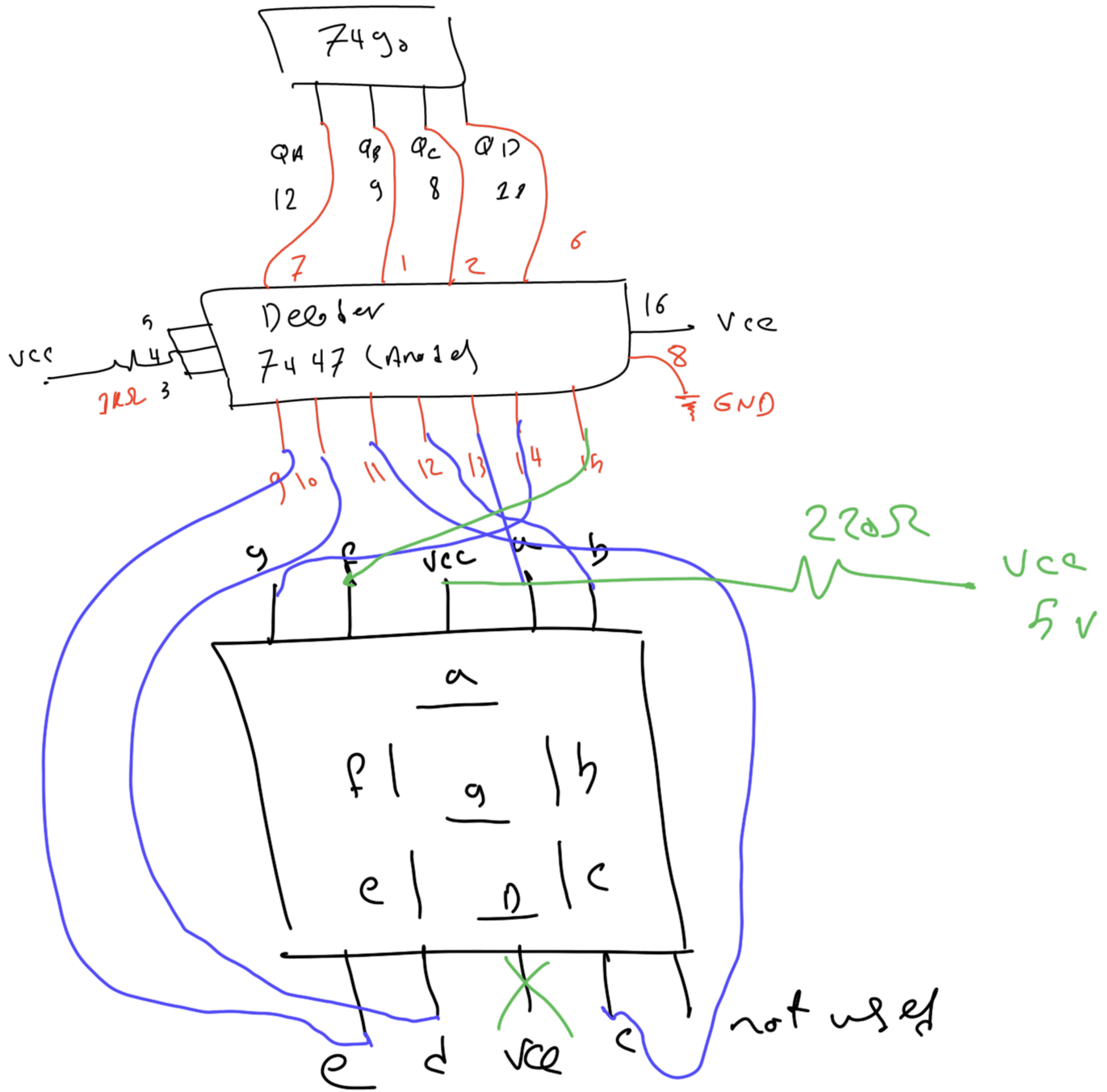
9 min

5 min

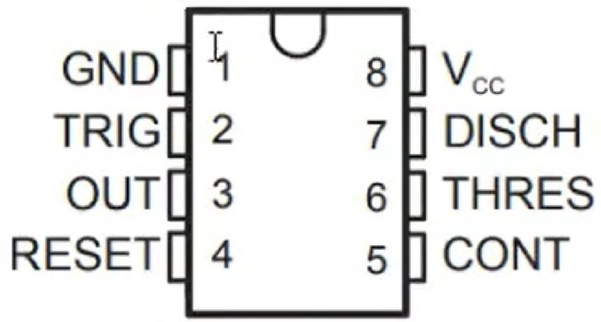
24 Hours

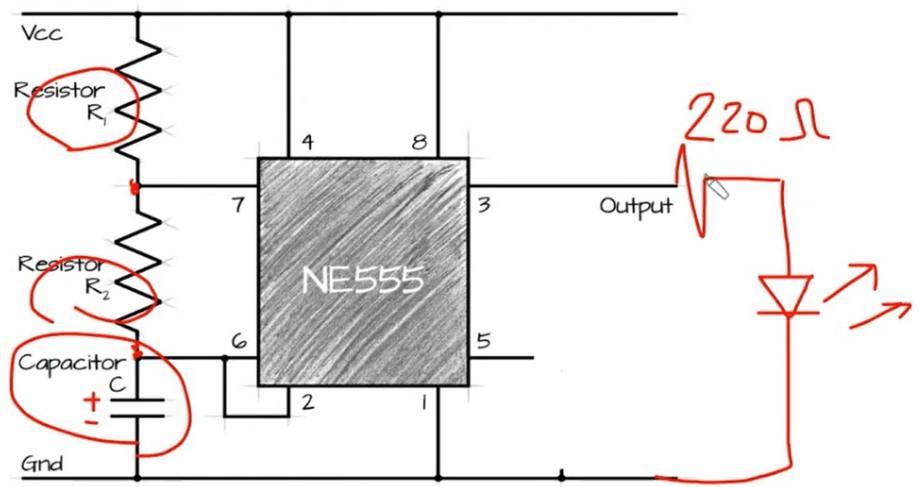
Reset

Counters


7490
QA
QB
QC
QD
12
9
8
11
7
1
2
6
Decoder
7447 (Anode)
16
Vcc
8
GND
5
4
VCC
3
10
11
12
13
14
15
220R
Vcc
5V
g
f
Vcc
a
b
a
f
g
b
e
d
c
e
d
Vcc
c
not used

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)





$$f = \frac{1.44}{(R_1 + 2R_2)C} = 5.1\,Hz$$

Capacitor (C)	1
Resistance 1 (R_1)	500
Resistance 2 (R_2)	14
Frequency	50.632 H2
Period (T)	19.750
Duty Cycle	50.88
Time High (T_1)	10.049

Capacitor (C)	47
Resistance 1 (R_1)	10
Resistance 2 (R_2)	10
Frequency	1.023
Period (T)	977.130
Duty Cycle	66.67
Time High (T_1)	651.420