Dated: _____ Computer Architecture:

⇒ VLSI → Very large scale integration.
↓ chotī se choti jaga mai zyada se zyada circuits ka ajana.

RISC → Reduced Instruction set Architecture
⇒ Isi waja se High level programming Languages aayiein.
jin mai single instruction mai hum bauhat saaray kaam kr sakte hain as compared to Assembly.

⇒ Computer Architecture ∝ Cost of the System. (As the area of the system is reduced, cost ↓

⇒ Research on Warehouse scale computers.

⇒ Embedded computers : Computers used for single tasks such as microwave, calculator etc.

02/10/2025 23:16

Dated: _____

## Computer Architecture:

Computer Architecture determines a computer component to exchange electronic signals to enable input, processing and output.

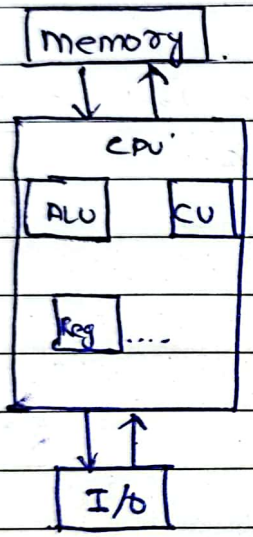
BLOCK DIA OF A communication SYSTEM.


memory → RAM.

## Bandwidth

The difference b/w min and max. speed is known as Band width.

VON-NEUMANN ARCHITECTURE




## Latency

Wo time jo kisi req, process ya packet ko queue (line) mein intezar krne mai lgta hai.

Latency = Prop time + transmission time + queueing time

⇒ Latency kisi bhi system ya network mai delay ko kaha jaata hai jo data ko ek point se doosre point tk pohonchne mai lagta hai.
⇒ measured in ms.
⇒ Latency ↓ Performance ↑

Dated: 30th Jan 2K25 Lecture # 05 and 06

**Q#** A network with bandwidth of 10 mbps can pass only an average of 12K frames per minute with each frame carrying an avg of 10K bits. What is the throughput of this network?

GIVEN

$$\text{Frames per second} = \frac{12{,}000}{60}$$

$$\text{Throughput} = 200 \times 10{,}000 = 2 \times 10^6 \text{ Kbps} = 2 \text{ mbps}$$

Hence we can say that throughput of this channel is actually 1/5th of the Bandwidth of this channel.

---

⇒ Another type of delay other than latency are due to the structure of the system.

## ENERGY AND POWER CONSUMED BY A PROCESSOR

Dynamic

⇒ Power is totally dependent on System's clock.

$$D.E = \frac{1}{2} \times C_L \times V^2.$$

$$D.P = \frac{1}{2} \times C_L \times V^2 \times f$$

Dated: _____

**Q#** Consider a micro-processor designed to have adjustable voltage, so a 15% reduction in voltage may result in 15% reduction in Power. What would be the impact on dynamic energy and dynamic power?

a) D.E

$$\frac{E_{new}}{E_{old}} = \frac{\frac{1}{2} \times C_L \times V^2}{\frac{1}{2} \times C_L \times V^2}$$

$$\frac{E_{new}}{E_{old}} = \frac{(0.85V)^2}{V^2}$$

$$\frac{E_{new}}{E_{old}} = (0.85)^2 = 0.7225 \quad \text{[Ans]}$$

b) $D.P = \frac{1}{2} \times C_L \times V^2 \times f$

$D.P = D.E \times f$

$$\frac{P_{new}}{P_{old}} = 0.7225 \times \frac{0.85f}{f}$$

$$\frac{P_{new}}{P_{old}} = 0.6141$$

Points

⇒ Energy and Power are not same

⇒ ∴ Power is dependent on clock frequency f.

Dated: 6 Feb 2K25' Thursday Lecture # 08'

CPU Time = CPU clock cycles for a prog * clock cycle time.

$\therefore \frac{1}{f} = t$

$\therefore$ CPU Time $= \frac{\text{CPU clock cycles for a program}}{\text{clock Rate.}}$ (T)

**CPI :-**

Different machine instructions may require different number of clock cycles to execute. It measures the time needed to execute instruction.

$$CPI = \frac{\text{CPU clock cycles for a program}}{\text{Instruction count.}} = \frac{C}{Ic}$$

CPU Time = Instruction count x cycles per instruction * clock cycle time. (T)

IC :=

Ic is the size of a program. which is the number of machine instructions to be executed in a program.

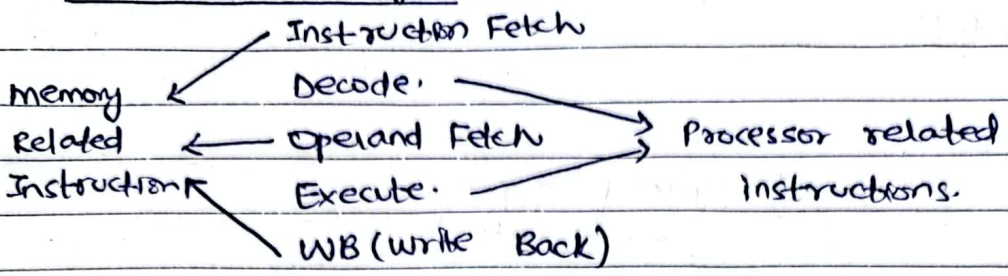
$$T = CPI \times IC \times t$$

$$\text{CPU clock cycles} = \sum_{i=1}^{n} IC_i \times CPI_i$$

$$\text{CPU Time (Avg)} = \sum_{i=1}^{n} IC_i \times CPI_i \times \text{Clock Cycle Time}$$

Dated: _____

## CPU Execution cycle.




H.W; Study different types of memory w.r.t size and cost.
Regista, RAM, Hard Disk, Cache

## LECTURE # 09.

$$Y = \frac{\text{Working dies}}{\text{Total Dies}} = \frac{900}{1000} \times 100\%.$$

$$\boxed{T = \frac{IC \times CPI}{f}}$$

**MIPS :- (million Instruction per second) :-**

The processor speed is often measured in terms of MIPS.

$$\text{MIPS rate} = \frac{IC}{T \times 10^6}$$

$$= \frac{f}{CPI \times 10^6} \qquad \because CPI = \frac{C}{IC}.$$

$$= \frac{f \times IC}{C \times 10^6} \rightarrow (1)$$

$$\boxed{T = \frac{IC}{MIPS \times 10^6}}$$

Dated:

## Throughput

The number of programs executed per unit time.

$$W = \frac{1}{T} \rightarrow T = \frac{CPI \times IC}{f}$$

$$W = \frac{f}{IC \times CPI}$$

$$\boxed{W = \frac{MIPS \times 10^6}{IC}}$$

**Q#** Consider a multicycle MIPS processor, there are 5 types of instructions:-

Load (5 cycles), store (4 cycles), R-type (4-cycles), Branch (3 cycles), Jump (3 cycles).

If a program has 50% Load instructions, 25% store instructions, 15% R-instructions, 8% branch instructions, and 2% jump instructions. Calculate effective CPI.

**Sol**

$$\text{Effective CPI} = \sum_{i=1}^{N} \frac{CPI_i \times IC_i}{IC}$$

$$= \frac{(5 \times 50) + (4 \times 25) + (4 \times 15) + (3 \times 8) + (3 \times 2)}{100}$$

$$= 4.4 \text{ Ans}$$

Dated:

Q# An instruction set has three instruction classes, A has CPI = 1, B has CPI = 2, C has CPI = 3. Two code sequences have the following ICs.

| code seq | IC for class A | B | C |
|---|---|---|---|
| 1 | 2 | 1 | 2 |
| 2 | 4 | 1 | 2 |

Calculate CPU cycles and CPI for seq 1 and 2

Amdahl's Law

To improve CPU performance, it is not necessary to consider all components of the system.