COURSE DESCRIPTION: EE-3009 Computer Architecture (CA)

COURSE DESCRIPTION FORM

INSTITUTION FAST School of Computing, National University of Computer and Emerging Sciences, Karachi

PROGRAM TO BE EVALUATED	BS-School of Computing– Spring 2025

Course Description

Course Code	EE2013
Course Title	Computer Architecture
Credit Hours	3
Prerequisites by Course(s) and Topics	DLD,COAL
Grading Policy	Absolute grading
Policy about missed assessment items in the course	Retake of missed assessment items (other than midterm/ final exam) will not be held. For a missed midterm/ final exam, an exam re-take/ pre-take application along with necessary evidence are required to be submitted to the department secretary. The examination assessment and retake committee will decide the exam re-take/ pre-take cases.
Course Plagiarism Policy	Plagiarism in project or midterm/ final exam may result in F grade in the course. Plagiarism in an assignment will result in zero marks in the **whole assignments** category.
Assessment Instruments with Weights (homework, quizzes, midterms, final, programming assignments, lab work, etc.)	

Assessment Item	**Number**	**Weight (%)**
Assignment	3	10%
Quiz	3	10%
Midterm Exam	2	30%
Final Exam	1	50%

Course Instructors	Aashir Mahboob, Kashan Hussain , Shoaib Rauf & Dr Nausheen
Lab Instructors (if any)	
Course Coordinator	Aashir Mahboob
URL (if any)	

Current Catalog Description	- Get a working knowledge of architecture of subsystems and the general - principles that affect their performance - Get knowledge about advanced architectural features that boost the performance - of computers with pipelining and superscalar architecture - Analyze the performance of systems and quantify the performance measurements - Study the major trends towards parallelism with respect to a single processor - and multicore architecture
Textbook	**Computer Architecture: A Quantitative Approach** *John L. Hennessy & David A. Patterson 6th Edition*
Reference Books	**Computer Organization & Architecture** *William Stallings Pearson, 9th Edition*

S#	CLO	Domain	Taxonomy level	PLO
1	Describe the performance evaluation criteria of computers and recognize performance of different computing systems.	Cognitive	2	1
2	Describe advanced concepts in computer architecture like multi-cycle pipeline, dynamic scheduling, dynamic branch prediction, loop unrolling, super-scalar, multi-issue and multi-core processors and identify their impact on a given machine.	Cognitive	2	1
3	Analyze existing bottlenecks in computer architecture designs and categorize potential solutions, virtual memory contribution toward performance improvement of a computing machine.	Cognitive	4	2

Program Learning Outcome (PLO)	Description
	PLO-01: Computing Knowledge: An ability to apply knowledge of mathematics, science, computing fundamentals and an engineering specialization to the solution of complex computing problems.
	PLO-02: Problem Analysis: Identify, formulate, research literature, and analyze complex computing problems, reaching substantiated conclusions using first principles of mathematics, natural sciences, and computing sciences.

	Topics to be covered				
	List of Topics	**Week**	**Chapter/ Appendix**	**Contact Hours**	**CLO(s)**
Topics covered in the course with number of lectures on each topic (Assume 16 weeks of instruction and 1 hour lecture duration)	Introduction ***(1 Lecture)*** --- Classes of Computers ***(2 Lecture)*** ---	**1**	**1**	**3**	**1**
	Performance Metrices of a system (***2 Lectures)*** --- Measuring and Reporting Performance ***(1 Lecture)*** ---	**2**	**1**	**3**	**1**
	Amdahl Law, CPU Performance Equation ***(2 Lecture)*** --- Chapter related fallacies and pitfalls ***(1 Lecture)*** ---	**3**	**1**	**3**	**1**
	Principals of ISA, internal Storage, Memory addressing ***(1.5 Lecture)*** --- Control Flow Instructions, Role of Compilers, IS encoding ***(1.5 Lecture)*** ---	**4**	**A**	**3**	**3**

	Register Allocation **(1 Lecture)** **----------** MIPS Architecture **(1 Lecture)** **----------** Instruction Usage , Chapter related fallacies and pitfalls **(1 Lecture)**	**5**	**A**	**3**	**2**
	WEEK 6	***MID -1 Exam***			
	Pipelining Basic concepts, limitations, Major Hazards of pipelining & Internal Forwarding **(3 Lectures)**	**7**	**C**	**3**	**3**
	Exception in Pipeline, Precise Exceptions & Floating-point Pipeline **(3 Lectures)**	**8**	**C**	**3**	**3**
	MIPS R-4000 Pipeline, Superscalar and VLIW architecture. **(3 Lectures)**	**9**	**C**	**3**	**2**

	Instruction Level Parallelism, data and name dependance, Loop unrolling ***(3 Lectures)***	**10**	**3**	**3**	**3**
	Week 11	***MID -2 Exam***			
	Dynamic Scheduling -Scoreboarding technique and Tomasulo's Approach **(3 Lectures)**	**12**	**3&C**	**3**	**1**
	Basics of Caches, Caches miss , hits & Organization **(3 Lectures)**	**13**	**B**	**3**	**3**
	Four memory hierarchy questions, Six basic cache optimizations ***(3 Lectures)***	**14**	**B**	**3**	**3**
	Advance Cache Optimizations, Virtual memory , DRAM optimizations (***3 Lectures)***	**15**	**B**	**3**	**3**

	Simultaneous Multithreading (SMT), Multiprocessors Thread-Level parallelism **(3 Lectures)**	16	**5**	**3**	**3**
	Total		**16**	**48**	

Laboratory Projects/Experiments Done in the Course	**None.**
Programming Assignments Done in the Course	None.

Class Time Spent (in percentage)	**Theory (%)**	**Problem Analysis (%)**	**Solution Design (%)**	**Social and Ethical Issues (%)**
	50	25	20	5

Instructor Name: Aashir Mahboob

Instructor Signature: Aashir Mahboob

Date: 16th-January-2025