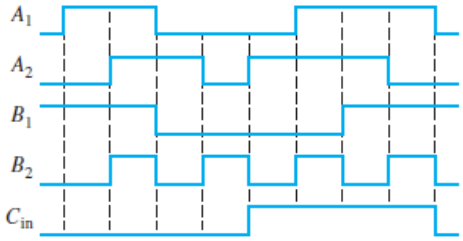
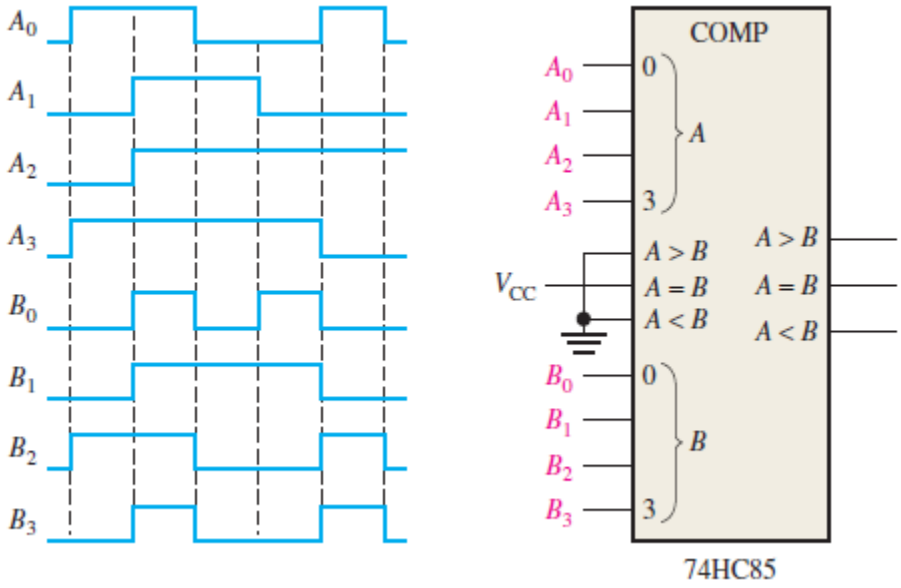
DLD Assignment -2

1. The input waveforms in Figure are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.



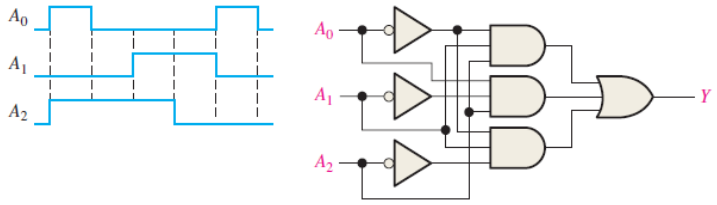
2. For the 4-bit comparator in Figure, plot each output waveform for the inputs shown. The outputs are active-HIGH.



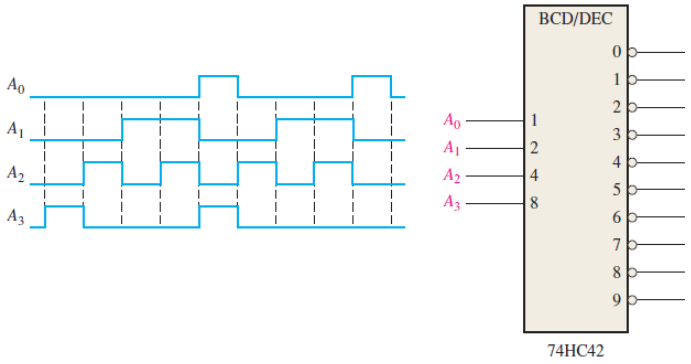
3. Show the decoding logic for each of the following codes if an active-HIGH (1) output is required: (a) 1101 (b) 1000 (c) 11011 (d) 11100

4. You wish to detect only the presence of the codes 1010, 1100, 0001, and 1011. An active-HIGH output is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be LOW.

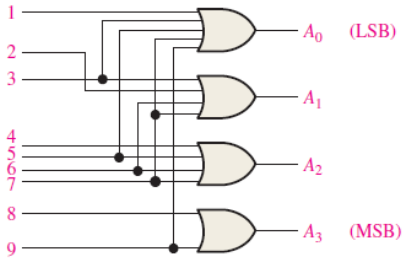
5. If the input waveforms are applied to the decoding logic as indicated in Figure 6–76, sketch the output waveform in proper relation to the inputs.



6. BCD numbers are applied sequentially to the BCD-to-decimal decoder in Figure 6–77. Draw a timing diagram, showing each output in the proper relationship with the others and with the inputs.



7. For the decimal-to-BCD encoder logic of Figure, assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD (8421) code?



8. The notation x1 x0 represents a two-bit binary number that can have any value (00, 01, 10,11); for example, when x1= 1, x0 = 0, the binary number is 10, and so on. Similarly, y1 and y0 represent another two-bit binary number. Design a logic circuit, using x1,x0,y1, and y0 inputs, whose output will be HIGH only when the two binary numbers x1 x0 and y1 y0 are opposite.

9. Write the function table for a half subtractor (input A and B, output DIFF and CARRY). From the function table, design two logic circuits that will act as half subtractor.
10. Derive an expression for a 2-bit magnitude comparator using Table.

A2	A1	B2	B1	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

11. For the multiplexer in Figure1, determine the output for the following input states: D0 = 1, D1 = 0, D2 = 0, D3 = 1,
(a) S0 = 0, S1 = 1 (b) S1 = 0, S1 = 1 (c) S0 = 1, S1 = 0

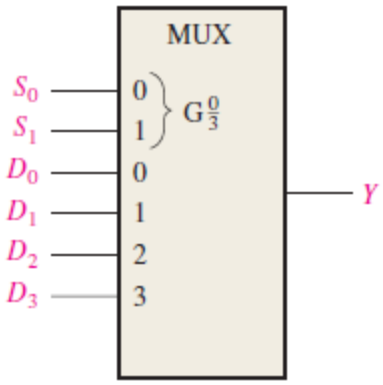


Figure1

12. If the data-select inputs to the multiplexer in the above Figure 1 are sequenced as shown by the waveforms in Figure 2, determine the output waveform with the data inputs specified in Problem 3.

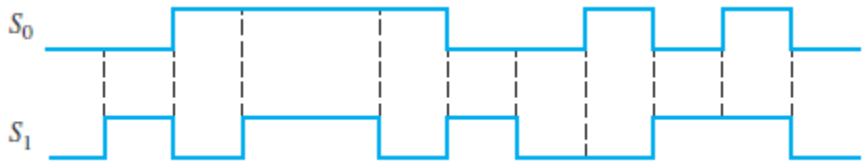
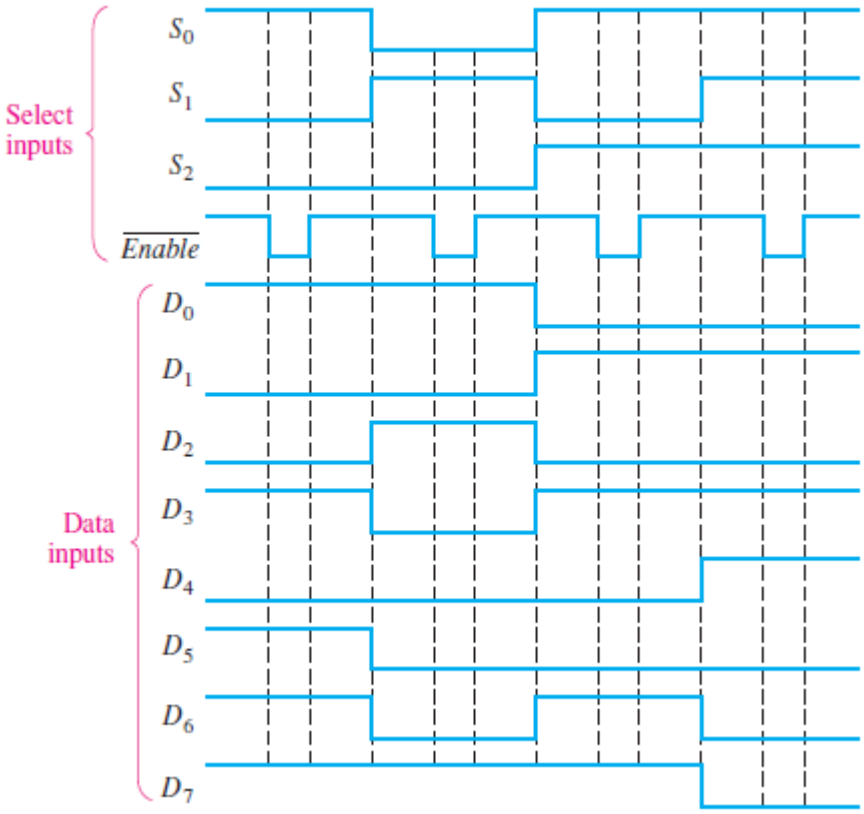


Figure2

13. The waveforms in Figure 3 are observed on the inputs of a 74HC151 8-input multiplexer. Sketch the Y output waveform.



14. Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is a serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is first in the sequence, with its LSB first, and it should appear in the first 4-bit positions of the output.
15. Implement the following Boolean function using the decoder.
    F(A, B, C,D) = Σ (1, 2, 3, 7,9,13,15)
16. Implement the logic function in the table by using a 74S151 8 input data selector/multiplexer. $X(A_3, A_2, A_1, A_0) = \sum(2,3,4,8,9,10,11,15)$
17. Implement a full adder circuit by using:
    (a)3 – to - 8 line Decoder (b) 4 X 1 Multiplexers.
18. Construct a 16 X 1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.