National University of Computer & Emerging Sciences, Karachi

Spring 2021 CS-Department

Final Examination

June 14, 2021, 9:00 AM – 12:00 noon

Course Code: EE227	Course Name: Digital Logic Design
Instructor Names: Ms. Rabia Tabassum, Mr. Behraj Khan, Mr. Syed Waqar Ahmed	
Student Roll No:	Section No:

Instructions:

- Return the question paper. The question paper consists of two pages.
- All the answers must be solved according to the sequence given in the question paper.

Time: 180 minutes.

Max Marks: 100 points

Question 1: (Digital System and Boolean algebra) [15 Points]

(a) Add the following BCD numbers: 11010110 + 10011011 [5]

(b) Convert the sequence of binary numbers from 11011_2 to 11111_2 to a Gray code sequence. [5]

(c) Determine the values of the following 32-bit single-precision floating-point binary number: [5]
1 10000001 01001001110001000000000

Question 2: (Combinational Logic Analysis) [15 Points]

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Question 2: (Combinational Logic Analysis) [15 Points]

(a) Use Karnaugh map to simplify the Boolean function. $F(A,B,C,D) = \sum(0,2,4,5,6,8,10,13,15)$ [5]

(b) Your friend Batman is staying at your apartment to solve a mystery case. He noticed the lack of security in your apartment and conditioned to work on the case only if you design and install a security system. Your apartment has 2 rooms. Each room has two windows and a door. If any two of the doors or window or main entry gate to the apartment is opened then your designed security system activates the alarm. The alarm also activates if any of the windows or the door of Batman's

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(c) Design a combinational circuit with four inputs and one output with the following conditions: [5]

(i) The output is 1 when the binary value of the inputs is less than 7. The output is 0 otherwise.

(ii) The output is 1 when the binary value of the inputs is an even number.

Question 3: (Functions of Combinational Logic) [20 Points]

(a) The waveforms in Fig 1 are applied to the 4-bit even parity generator. Determine the output parity waveform in proper relation to the inputs. [5]

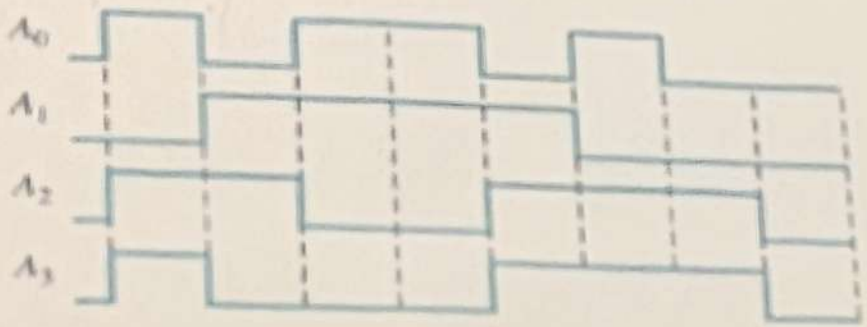

Fig-1

(b) Design a half-subtractor using basic primary gates. [5]

(c) Implement the logic function in the table by using a (74S151) 8 input data selector multiplexer

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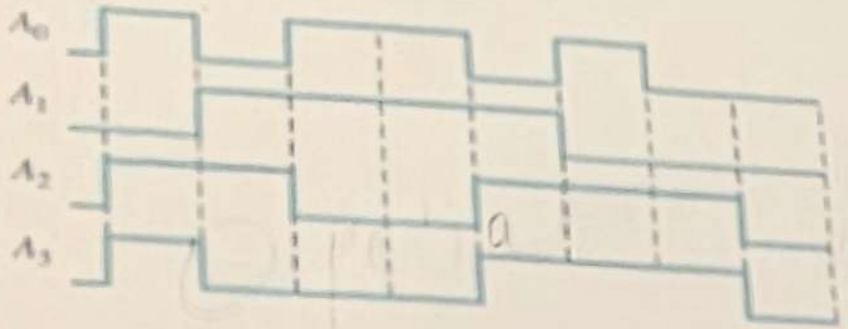

Fig-1

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$$X(A3, A2, A1, A0) = \sum(0,1,2,5,7,10,12)$$

[5]

(d) implement a full adder using 3 to 8 line decoder. [5]

Question 4: (Latches and Flip Flop)

(a) Fig 2 shown the JK inputs, clock and the Q output of a negative edge triggered JK flip-flop. Determine if the device is defective or not. Identify the defected outputs (if any) [25 Points] [5]

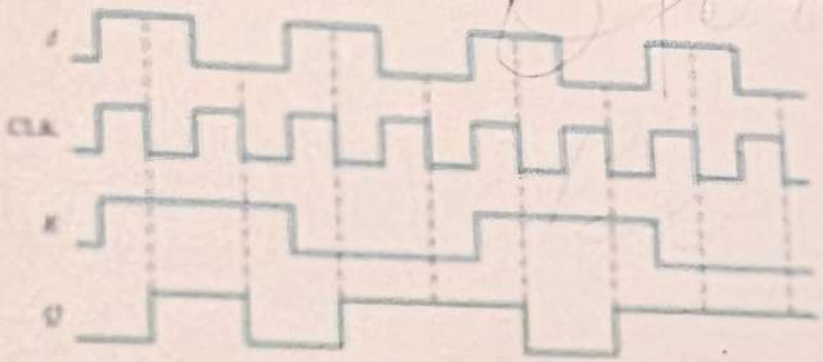


Fig-2

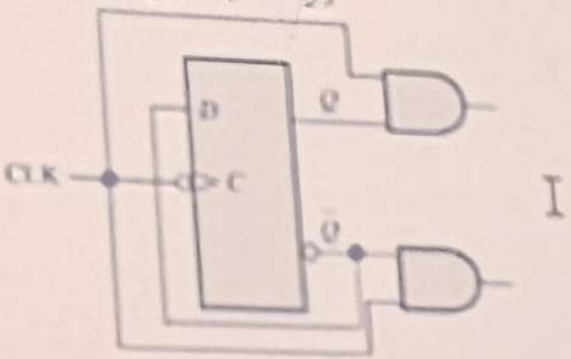


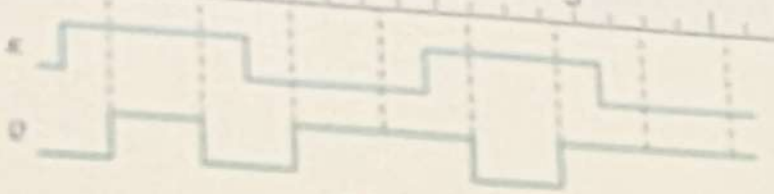
Fig-3

(b) A D flip-flop is connected such that the output Q' is feedback as input. Determine the Q output in relation to the clock. What specific function does this device perform? Also, draw the circuit diagram. [5]

(c) Design active low S-R latch , write down the truth table and draw the timing diagram as well [5]

(d) Draw the waveforms for inputs CLK, Q, Q' and the two outputs for the circuit in Fig 3. [5]

(e) For the circuit in Fig 4, develop a timing diagram for eight clock pulses, showing the Q_A and Q_B outputs in relation to the clock. [5]



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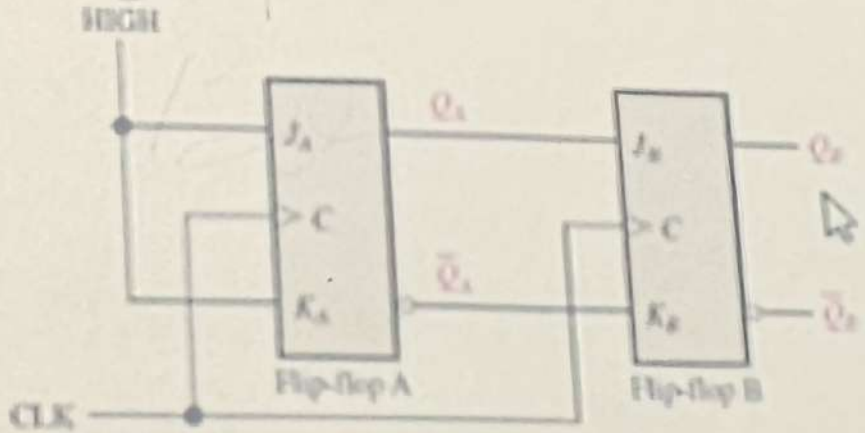

Fig-4

Question 5: (Registers and Counters) [25 Points]

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(a) Show how to connect a 4-bit asynchronous counter for each of the following moduli: (i) 13 (ii) 08 [5]

(b) If a 5-bit ring counter has an initial state 10001, determine the waveform for each Q output. [5]

(c) Determine the output sequence of the counter in Fig 5. Consider the counter initially cleared. [5]

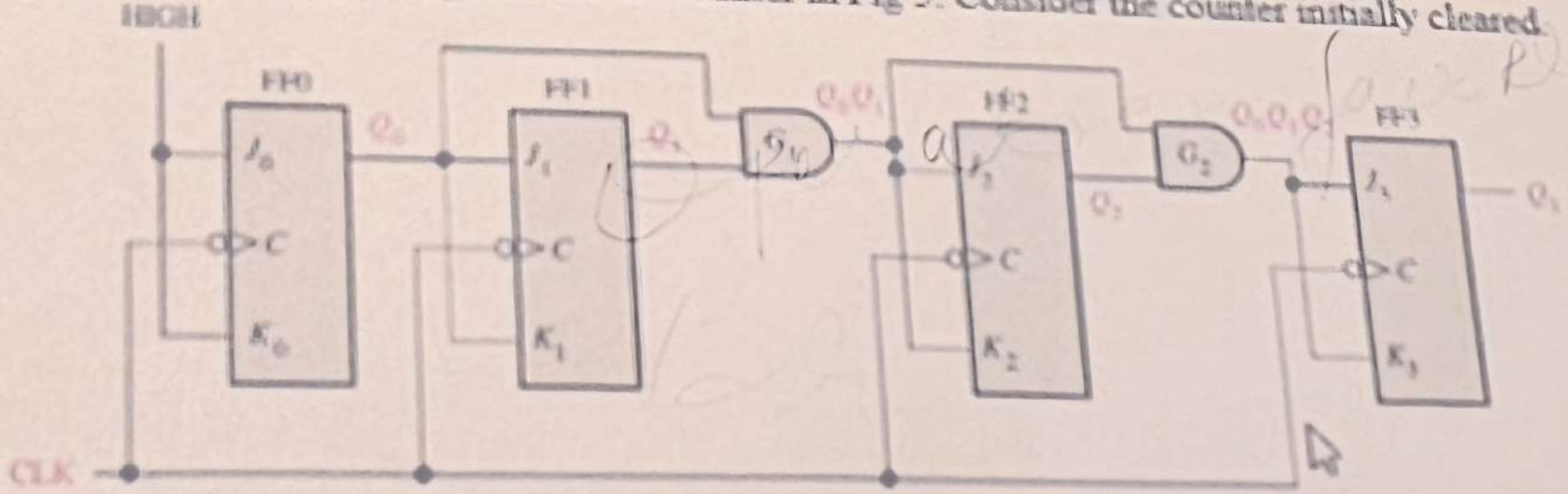

Fig-5

(d) Design an up /down counter with the binary count sequence: $001 \rightarrow 010 \rightarrow 101 \rightarrow 111 \rightarrow 001$. You may use any type of flip-flop. [10]