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Assignment :- 2

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Q.1 Input waveforms in figure are applied to a 2 bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.

A_1	B_1	C_{in}	Sum 1.	Cin/Cout	A_2	B_2	Sum 2.	Cout.
~~0~~	~~1~~	~~0~~			~~0~~	~~0~~		
1	1	0	0	1	0	0	1	0
1	1	0	0	1	1	1	1	1
0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	1	1	0
0	0	1	1	0	1	0	1	0
1	0	1	0	1	1	1	1	1
1	1	1	1	1	1	0	0	1
1	1	1	1	1	0	1	0	1
~~0~~	~~1~~	~~0~~			~~0~~	~~0~~		

Sum1:-

Sum2:-

Cout :-

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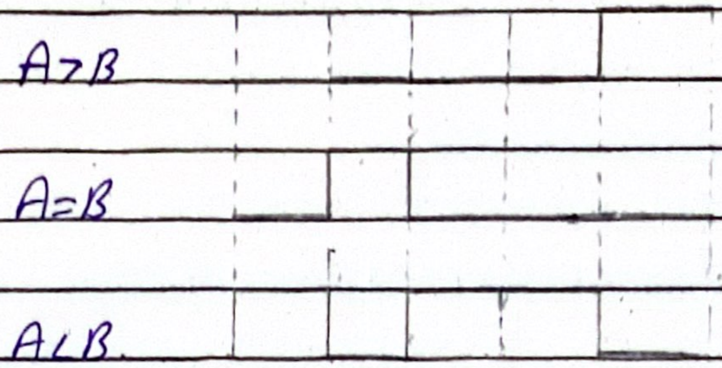
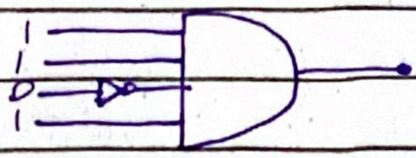
Q.2 For the 4-bit comparator in figure, plot each output waveform for the inputs shown. The outputs are active high.

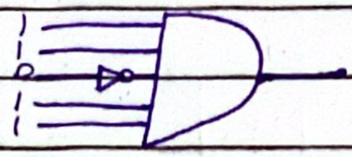


Q.3 Show the decoding logic for each of the following codes if an active-high (1) output is required:

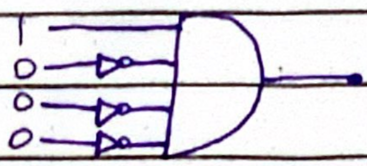
(a). 1101.



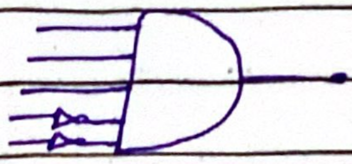
(c) 11011.



(b). 1000



(d) 11100



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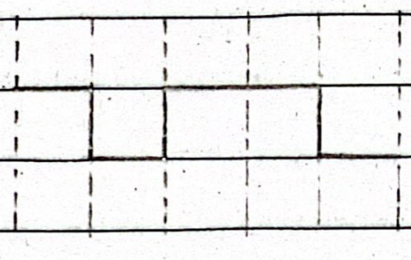
Q.4 You wish to detect only the presence of the codes 1010, 1100, 0001, and 1011. An active high input is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes ~~are~~ on the inputs. For any other code, the output must be low.

A_0A_1 \ A_2A_3	00	01	11	10
00	0	1	0	0
01	0	0	0	0
11	1	0	0	0
10	0	0	1	1

$$X = A_0\bar{A_1}A_2 + A_0A_1\bar{A_2}\bar{A_3} + \bar{A_0}\bar{A_1}\bar{A_2}A_3.$$

Q.5 If the ~~wave~~ inputs waveforms are applied to the decoding logic as indicate in figure, sketch the output waveform in proper relation to the inputs.



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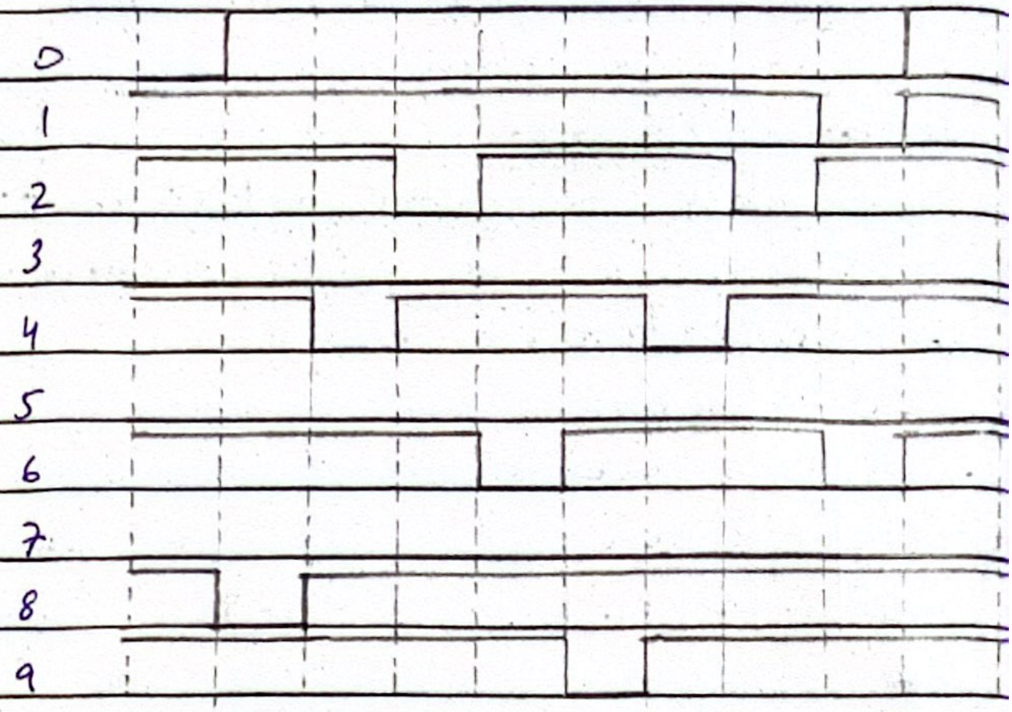
Q.6 BCD numbers are applied sequentially to the BCD-to-decimal decoder in figure. Draw a timing diagram, showing each output in a proper relationship with others and with the inputs.



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Q.7 For the decimal to BCD encoder logic of figure, assume that the 9 input and the 3 input are both high. What is the output code? Is it a valid BCD (8421) code?

$A_3A_2A_1A_0 = 1011$, which is not valid!

Q.8 The notation x1, x0 represents a two-bit binary number that can have any value (00, 01, 10, 11); for example, when x1=1, x0=0, the binary number is 10, and so on. Similarly, y_1 and y_0 represents another two-bit binary number. Design a logic circuit, using x1, x0, y_1 and y_0 inputs, whose output will be high only when the two binary numbers x1, x0, and y_1, y_0 are opposite.

x_1	x_0	y_1	y_0	X
0	0		1	1
0	1	1		1
1	0	0	1	1
1	1	0	0	1

Cancelled!
P.T.O For Truth Table

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x_1	x_0	y_1	y_0	X	
0	0	0	0	0	
0	0	0	1	0	
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	0	
0	1	1	0	1	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	1	
1	0	1	0	0	
1	0	1	1	0	
1	1	0	0	1	
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	0	

x_1x_0 \ y_1y_0	00	01	11	10
00			1	
01				1
11	1			
10		1		

$x_1 x_0 \bar{y}_1 \bar{y}_0 + x_1 \bar{x}_0 \bar{y}_1 y_0 + \bar{x}_1 \bar{x}_0 y_1 y_0 + \bar{x}_1 x_0 y_1 \bar{y}_0$

$\cancel{x_1 x_0 (\overline{y_1 + y_0}) + x_1 y_0 (\overline{x_0 + y_1}) + (\overline{x_1 + x_0}) y_1 y_0 + x_0 y_1 (\overline{x_1 + y_0})}$

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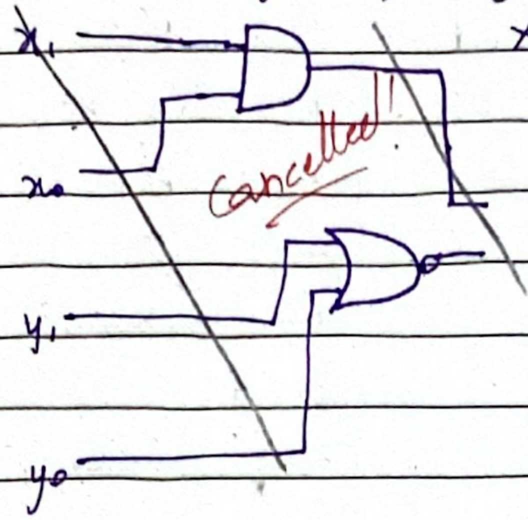
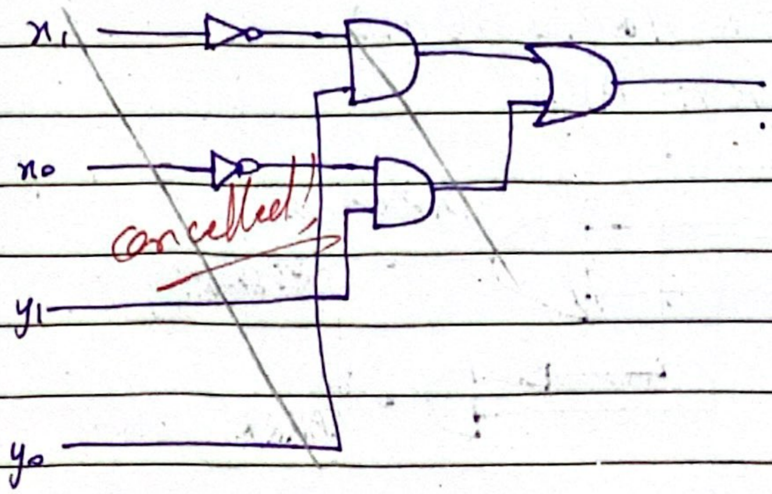
$X = x_1\bar{y}_1(x_0\bar{y}_0 + \bar{x}_0 y_0) + \bar{x}_1 y_1(\bar{x}_0 y_0 + x_0\bar{y}_0)$

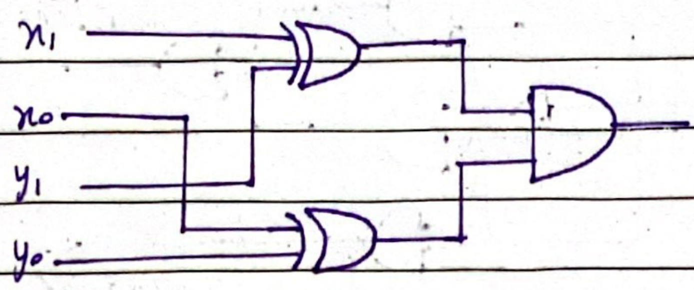


$X = x_1\bar{y}_1(x_0 \oplus y_0)$
$+ \bar{x}_1 y_1(x_0 \oplus y_0)$
$X = (x_0 \oplus y_0)(x_1\bar{y}_1 + \bar{x}_1 y_1)$
$X = (x_0 \oplus y_0)(x_1 \oplus y_1)$

$x_1 x_0 \oplus$ $(x_0 \oplus y_0)(x_1 \oplus y_1)$.

Simplified SOP:- $\cancel{x_1' y_0 + x_0' y_1}$.





~~Hadi~~

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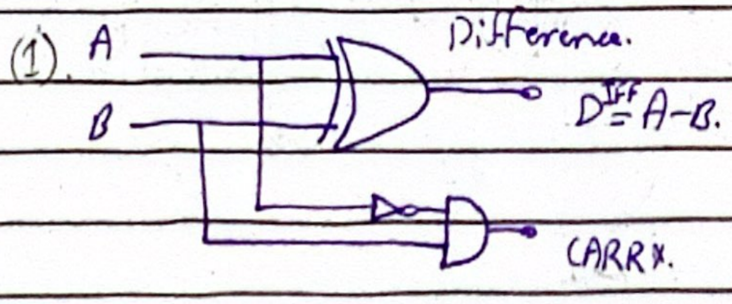
Q.9 Write the function table for a half subtractor (input A and B, output DIFF and (CARRY). From the function table, design two logic circuits that ~~will~~ ~~act~~ act as half subtractor.

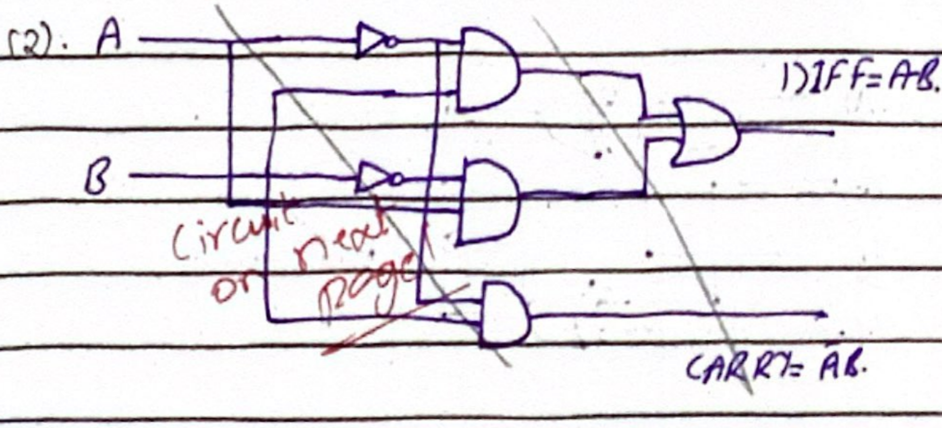
A	B	DIFF ~~Difference~~	CARRY.
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

DIFF:- $A \oplus B = \bar{A}B + A\bar{B}$.
CARRY:- $\bar{A}B$.

(1).



(2).



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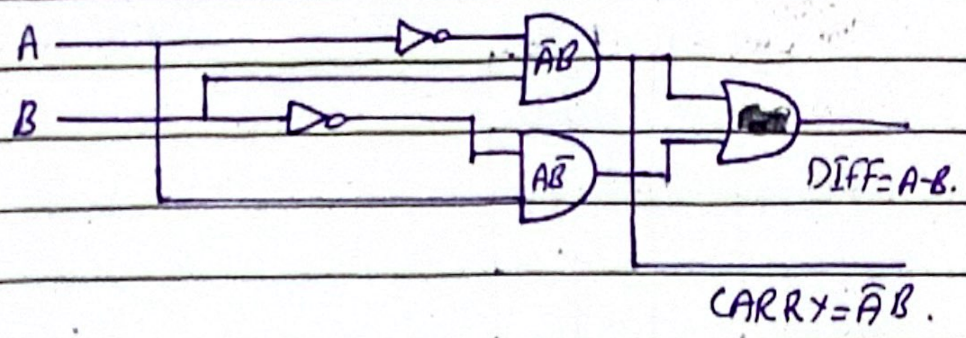
(2).



Q.10 Derive an expression for a 2-bit magnitude comparator using Table.

A_2	A_1	B_2	B_1	A>B	A<B	A=B.
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

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A<B.

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00		1	1	1
01			1	1
11				
10			1	

$\Rightarrow \bar{A}_1B_1 + \bar{A}_1\bar{A}_0B_0 + \bar{A}_0B_1B_0$

$\Rightarrow \cancel{\bar{A}(B_1 + \bar{A}_1B_0(\bar{A}_0 + B_1))}.\ \bar{A}_1B_1 + \bar{A}_0B_0(\bar{A}_1 + B_1).$

A>B.

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00				
01	1			
11	1	1		1
10	1	1		

$\Rightarrow A_1\bar{B}_1 + A_0\bar{B}_0\bar{B}_1 + A_1A_0\bar{B}_0$

$\Rightarrow A_1\bar{B}_1 + A_0\bar{B}_0(\bar{B}_1 + A_1).$

A=B.

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00	1			
01		1		
11			1	
10				1

$\Rightarrow \bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0\bar{B}_1B_0$

$+ A_1\bar{A}_0B_1\bar{B}_0 + A_1A_0B_1B_0$

$\Rightarrow \bar{A}_1\bar{B}_1(\bar{A}_0\bar{B}_0 + A_0B_0)$

$+ A_1B_1(\bar{A}_0\bar{B}_0 + A_0B_0).$

$\Rightarrow \bar{A}_1\bar{B}_1(\overline{A_0 \oplus B_0}) + A_1B_1(\overline{A_0 \oplus B_0})$

$\Rightarrow (\bar{A}_1\bar{B}_1 + A_1B_1)(\overline{A_0 \oplus B_0}) \Rightarrow (\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})$

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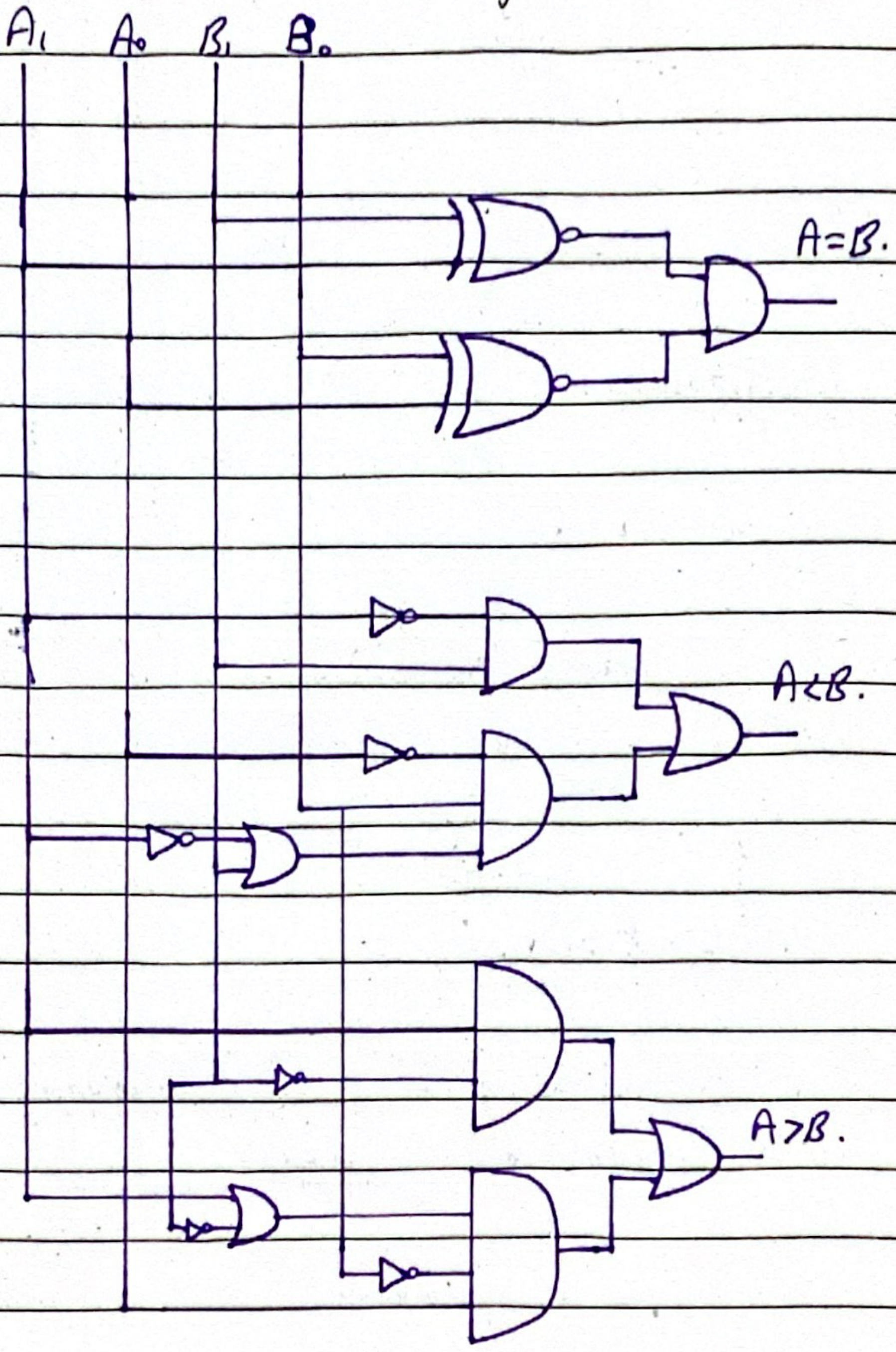
Circuit Diagram.



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Q.11 For the multiplexer in Figure 1. determine the output for the following input states: $D_0 = 1, D_1 = 0, D_2 = 0, D_3 = 1$.

(a) $S_0 = 0, S_1 = 1$.

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Output $= D_2$.

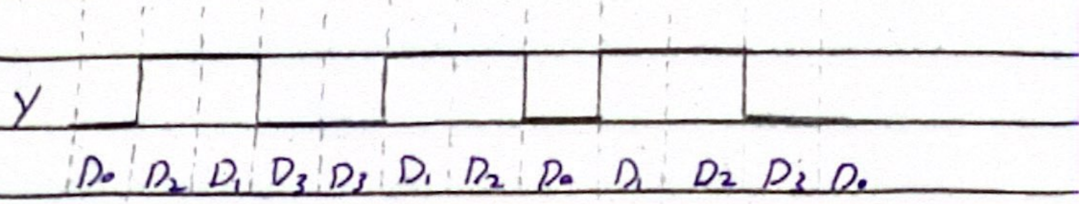
(b). $S_1 = 0, S_0 = 1$.

Type Error in Question.

(c) $S_0 = 1, S_1 = 0$.

Output $= D_1$.

Q.12 If the data inputs to the multiplexer in the above Figure 1 are sequenced as shown by the wave form in Figure 2, determine the output waveform with the data inputs specified.



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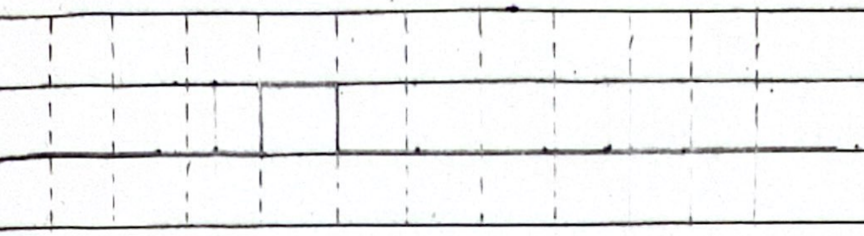
Q.13 The waveforms in figure are observed on the inputs of a 74HC151-8-input multiplexer. Sketch the y-output waveform.



Q.14 Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is the first in sequence, with its LSB first, and it should appear in the first 4-bits positions of the output.

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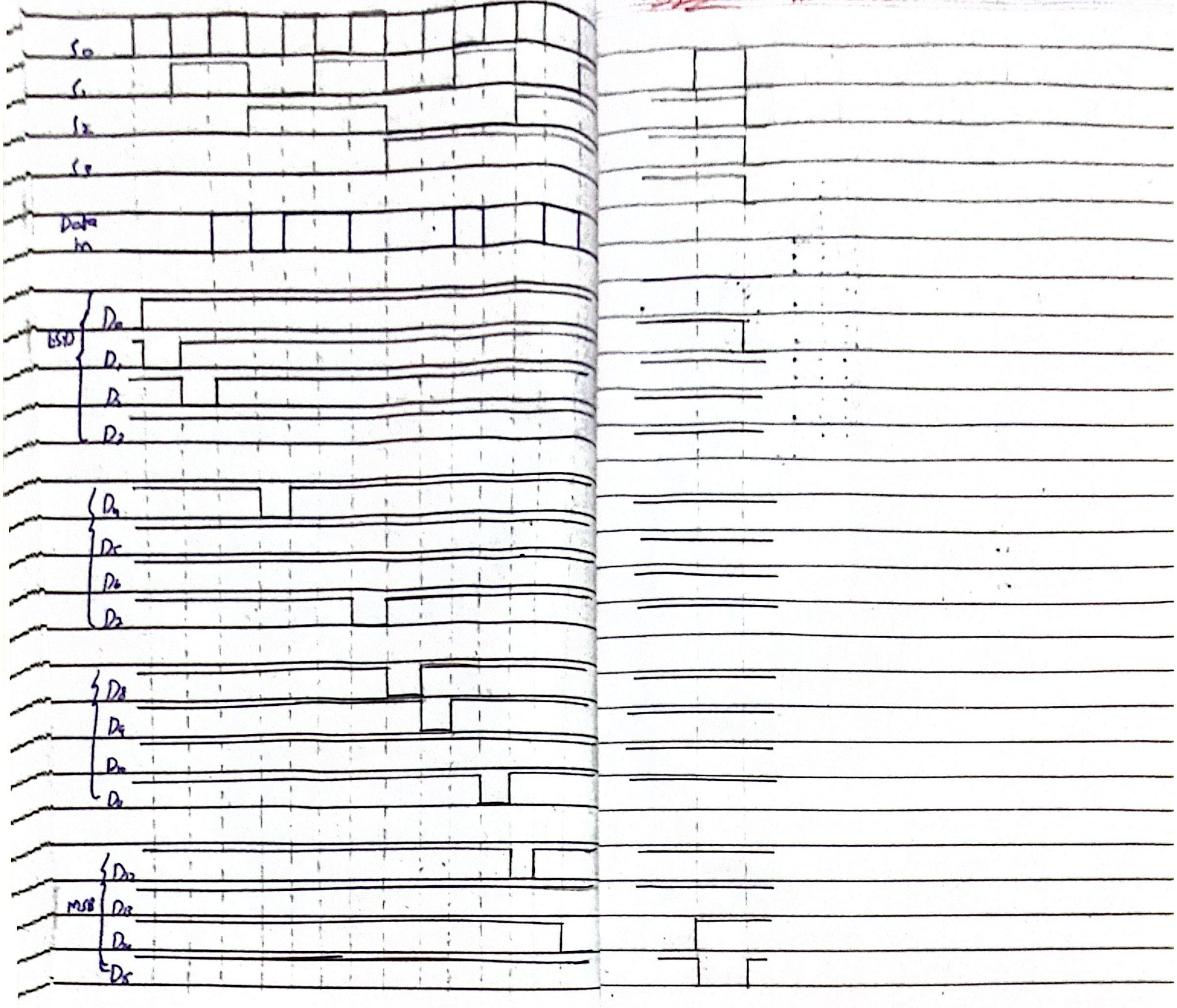

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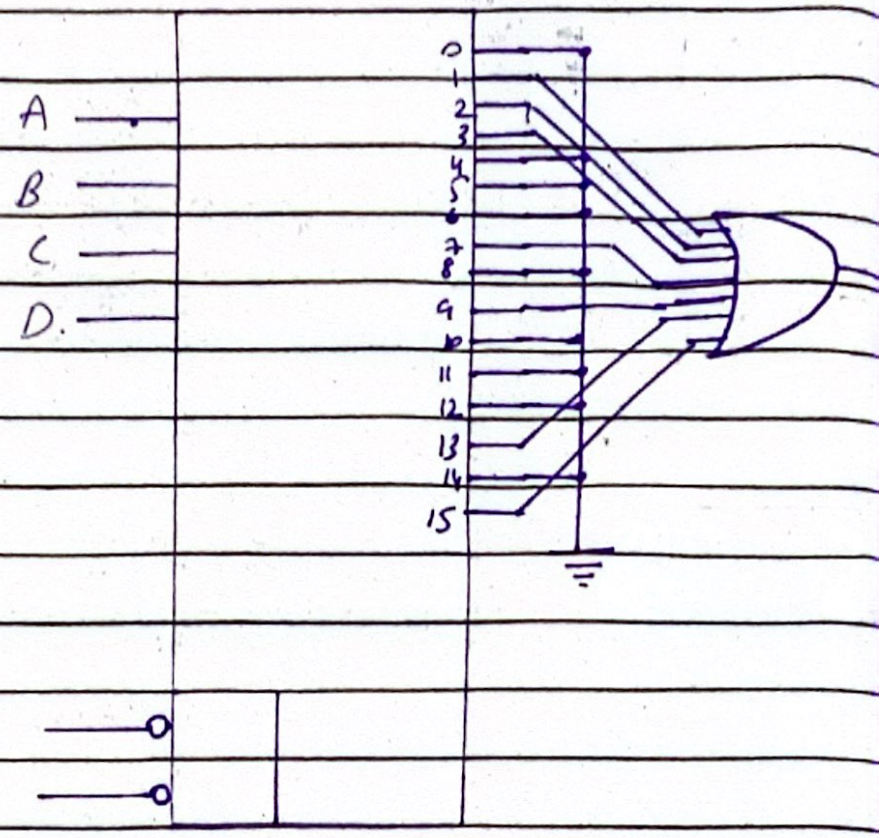
Q.15 Implement the following Boolean function using the decoder.

$F(A,B,C,D) = \Sigma(1,2,3,7,9,13,15)$



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Q.16 Implement the logic function in the table by using a 74S151 8 input data selector/multiplexer. $X(A_3, A_2, A_1, A_0) = \Sigma(2,3,4,8,9,10,11,15)$.

	A_3	A_2	A_1	A_0	X	
0	0	0	0	0	0	X=0.
	0	0	0	1	0	
1	0	0	1	0	1	X=1.
	0	0	1	1	1	
2	0	1	0	0	1	$X=\bar{A_0}$
	0	1	0	1	0	
3	0	1	1	0	0	X=0.
	0	1	1	1	0	
4	1	0	0	0	1	X=1
	1	0	0	1	1	
5	1	0	1	0	1	X=1
	1	0	1	1	1	
6	1	1	0	0	0	X=0.
	1	1	0	1	0	
7	1	1	1	0	0	$X=A_0$.
	1	1	1	1	1	

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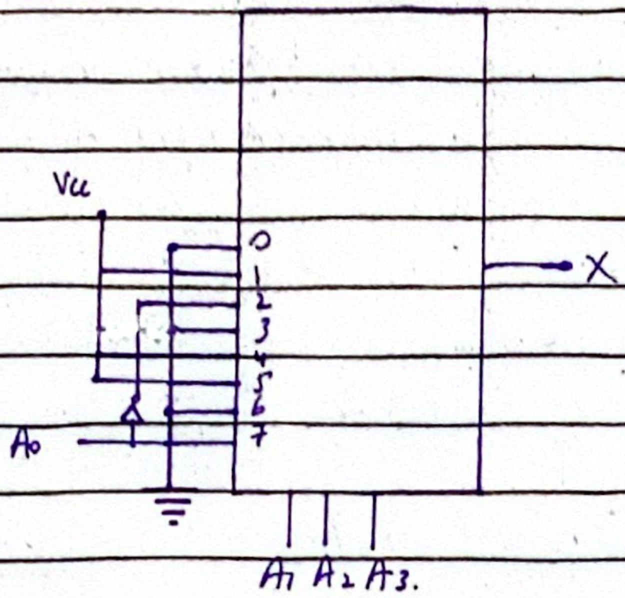

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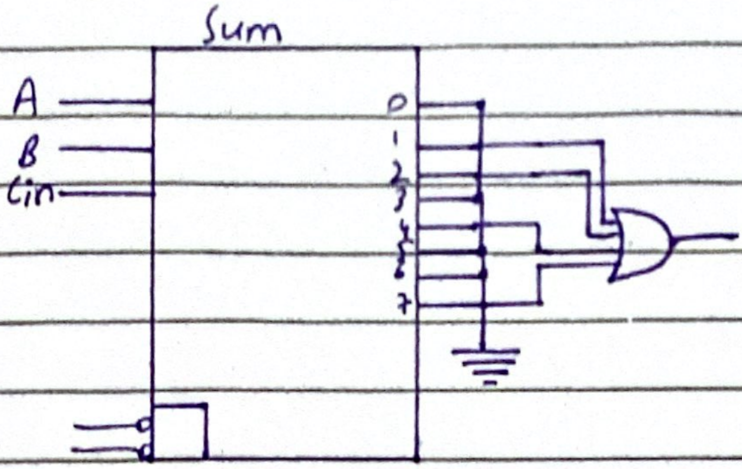
Q.17. Implement a full adder circuit by using:

(a). 3-to-8 line decoder.

A	B	Cin	Sum	Cout.
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



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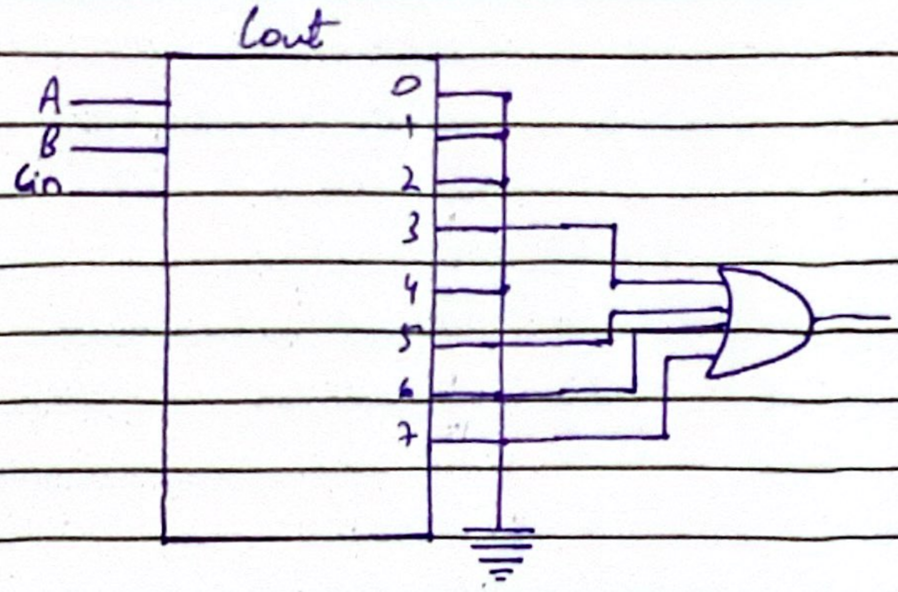

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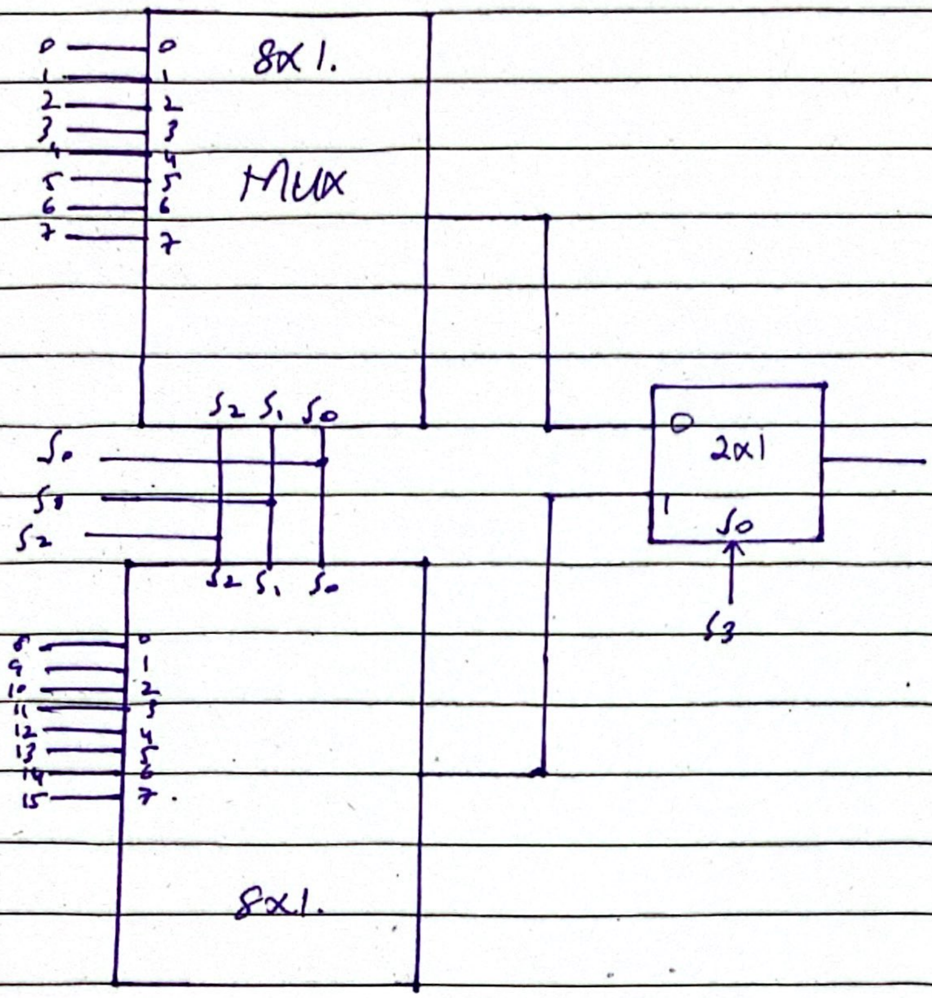
2.18 Construct a 16x1 multiplexer with two 8x1 and 2x1 multiplexers. Use block diagram.



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