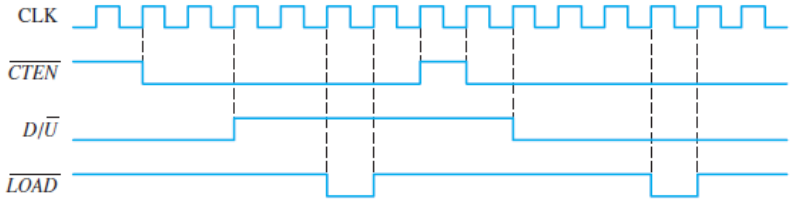
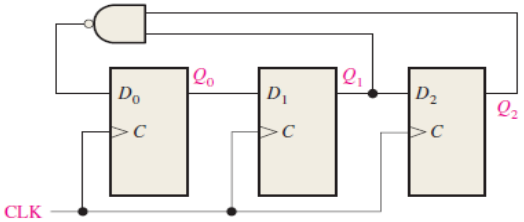
(Practice Questions)

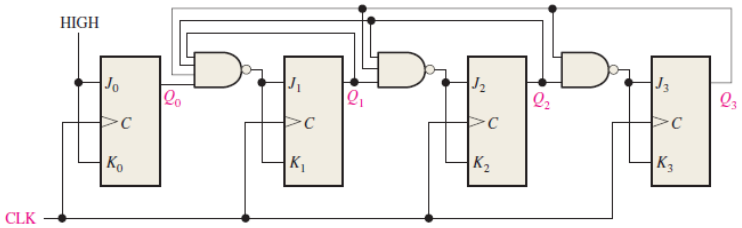
1. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP mode and when it is in the DOWN mode. Assume positive edge-triggering. 0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0
2. Develop the Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure. A binary 0 is on the data inputs. Start with a count of 0000.



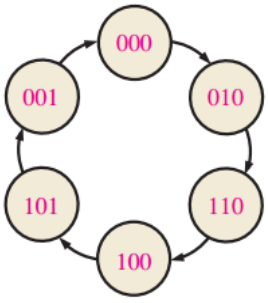
3. Repeat above Problem if the CTEN is inverted with the other inputs the same.
4. Determine the sequence of the counter in Figure.



5. Determine the sequence of the counter in Figure 9–74. Begin with the counter cleared.



6. Design a counter to produce the following sequence. Use J-K flip-flops. 00, 10, 01, 11, 00, ….
7. Design a counter to produce the following binary sequence. Use J-K flip-flops. 1, 4, 2, 5, 1, 6, 2, 1, ….
8. Design a counter to produce the following binary sequence. Use J-K flip-flops. 0, 9, 2, 8, 1, 5, 3, 7, 4, 5, 0, …
9. Design a counter by using D -flip flop only with the irregular binary count sequence shown in the state diagram of Fig. Include Next-state table, transition table, Karnaugh maps and final circuit.



10. If a 5-bit ring counter has an initial state 10101, determine the waveform for each *Q* output
11. Design a modulus-10 Johnson counter using J K flip flop. Write the sequence in tabular form.

1. The sequence 1011 is applied to the input of a 4-bit serial shift register that is initially cleared.
   What is the state of the shift register after three clock pulses?
2. If a 10-bit ring counter has an initial state 0101001111, determine the waveform for each *Q* output.
3. How many states are there in an 8-bit Johnson counter sequence? Write down all sequence.

7. What is the state of the register in Figure 8–49 after each clock pulse if it starts in the 101001111000 state?

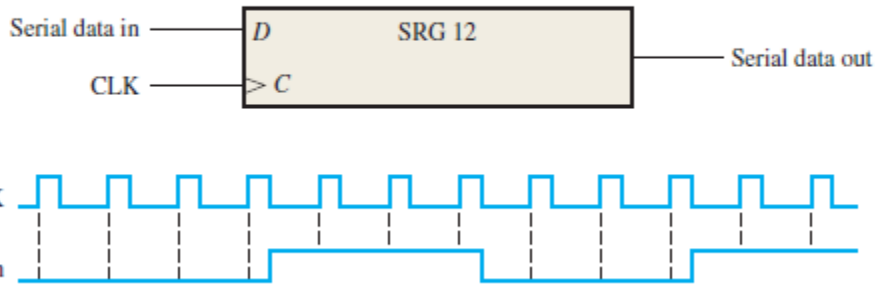
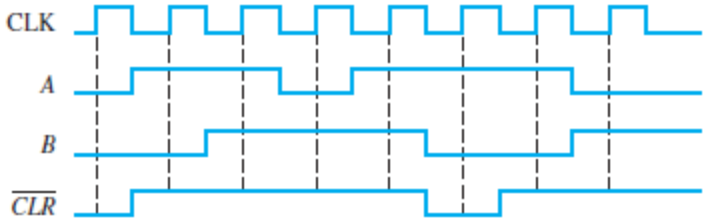
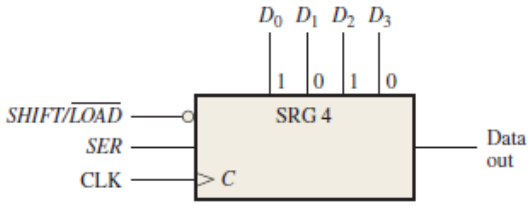


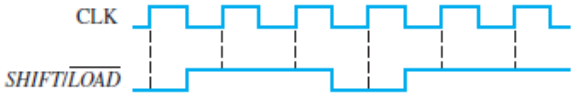
FIGURE 8–49

13. Develop the Q_0 through Q_7 outputs for a 74HC164 shift register with the input waveforms shown in Figure 8–53.



14. The shift register in Figure 8–54(a) has *SHIFT*/$\overline{LOAD}$ and CLK inputs as shown in part (b). The serial data input (*SER*) is a 0. The parallel data inputs are $D_0 = 1$, $D_1 = 0$, $D_2 = 1$, and $D_3 = 0$ as shown. Develop the data-output waveform in relation to the inputs.





26. Draw the logic diagram for a modulus-18 Johnson counter. Show the timing diagram and write the sequence in tabular form.

27. For the ring counter in Figure 8–60, show the waveforms for each flip-flop output with respect to the clock. Assume that FF0 is initially SET and that the rest are RESET. Show at least ten clock pulses.