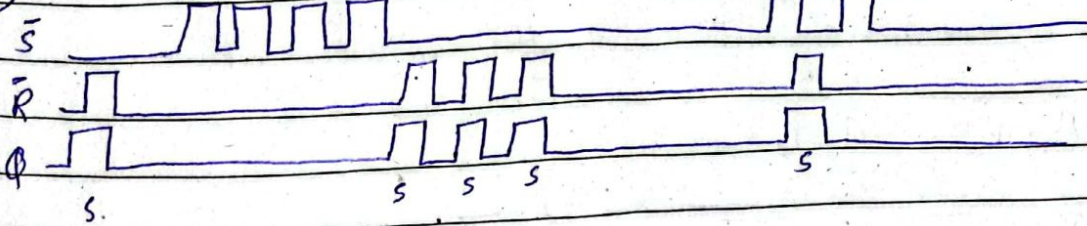


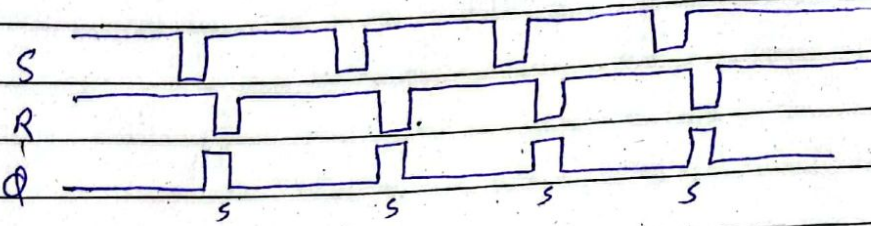
Assignment 3

Date: _____

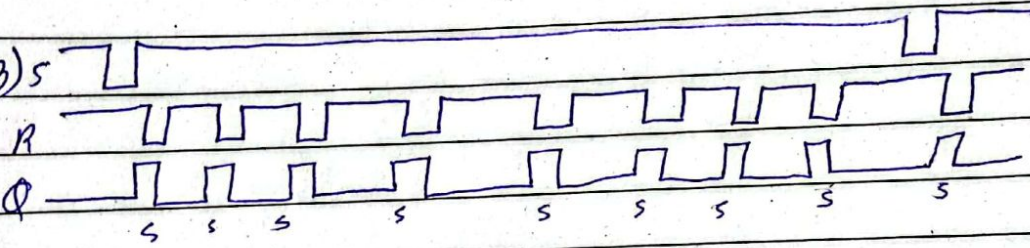
Q1)



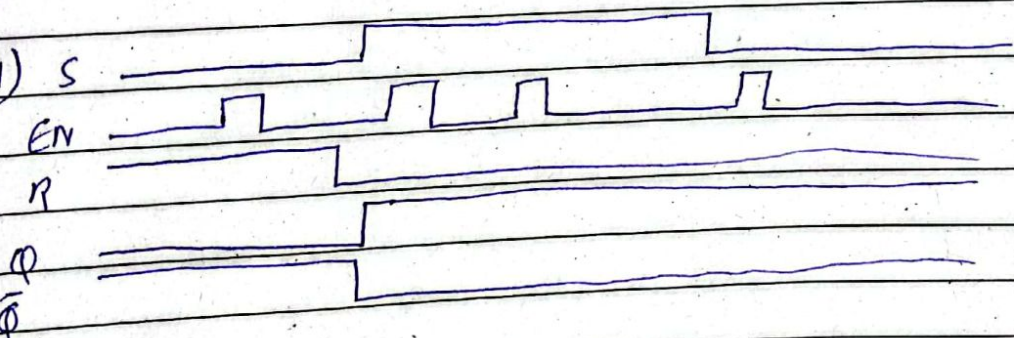
Q2)



Q3)



Q4)



Q5)

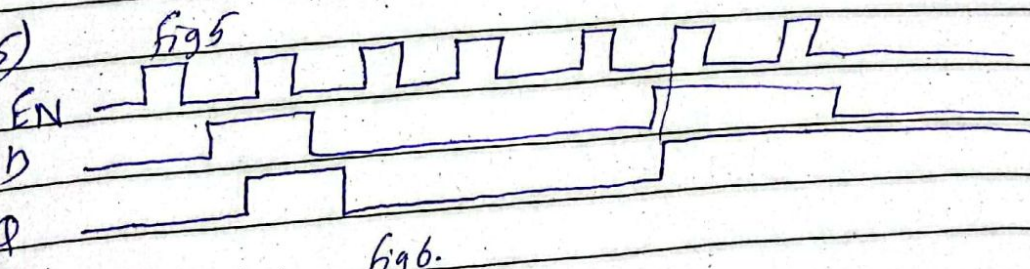
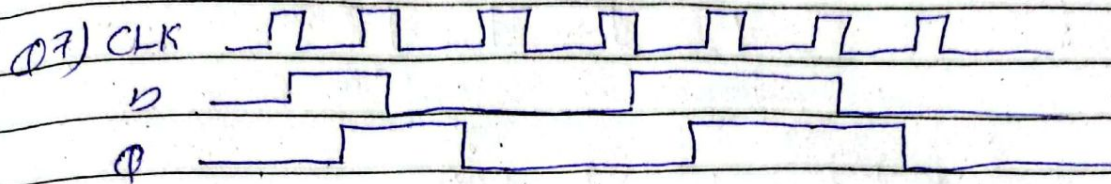
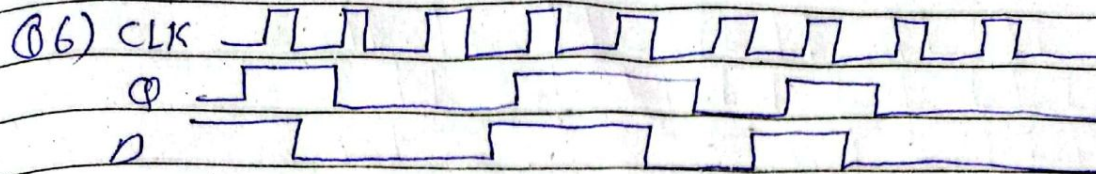


fig6.

EN

D

Q



Q8) *fig 9.*

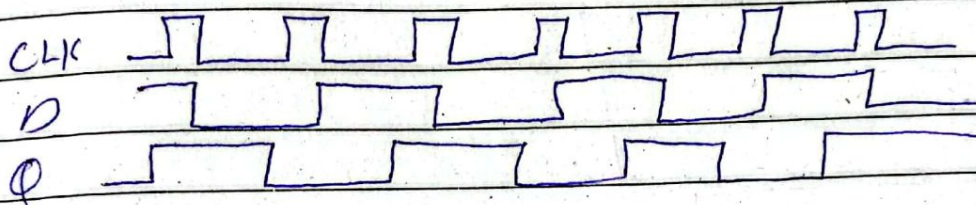
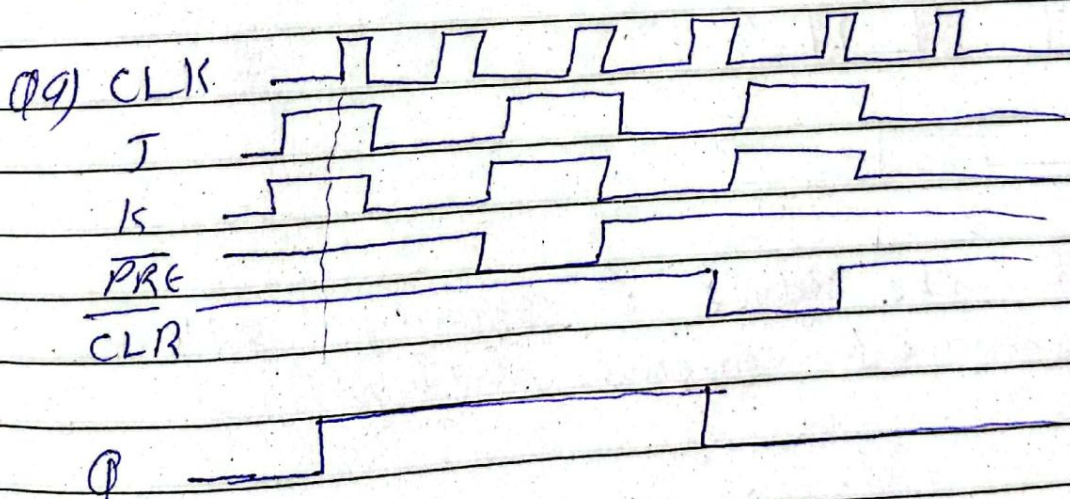
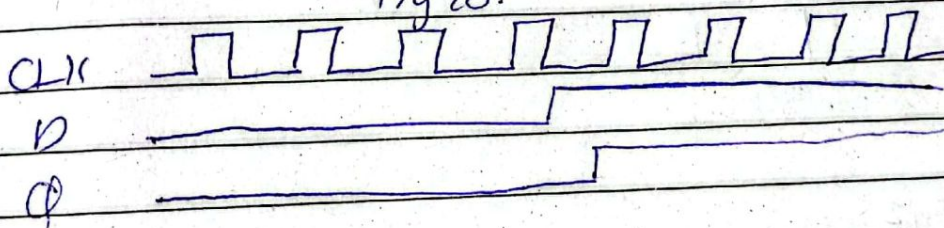
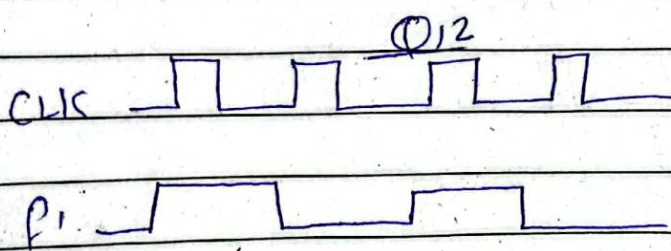
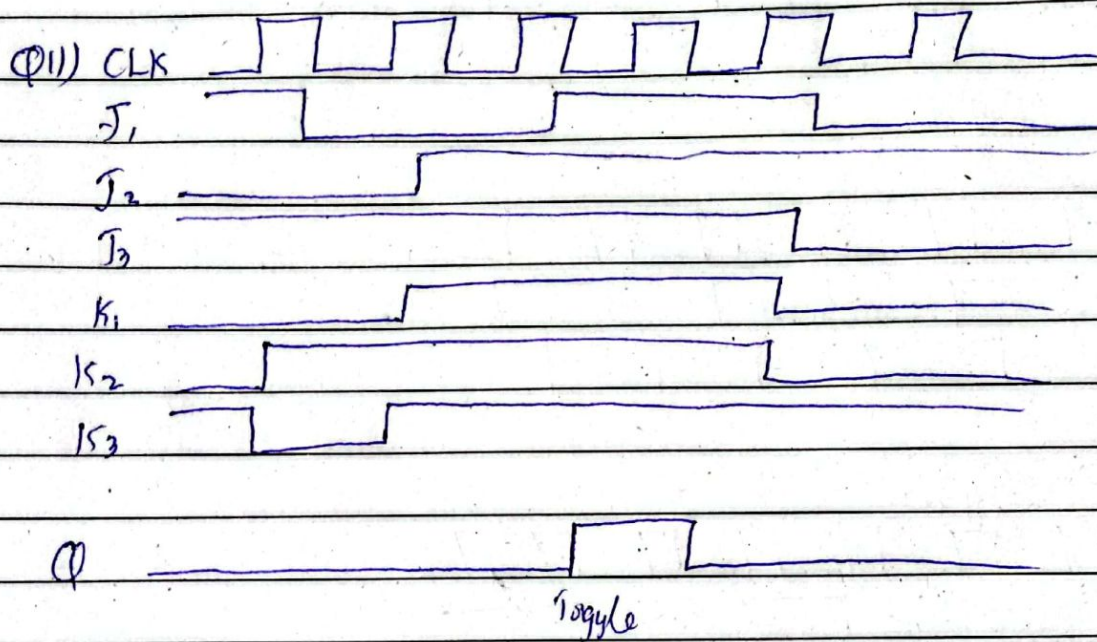
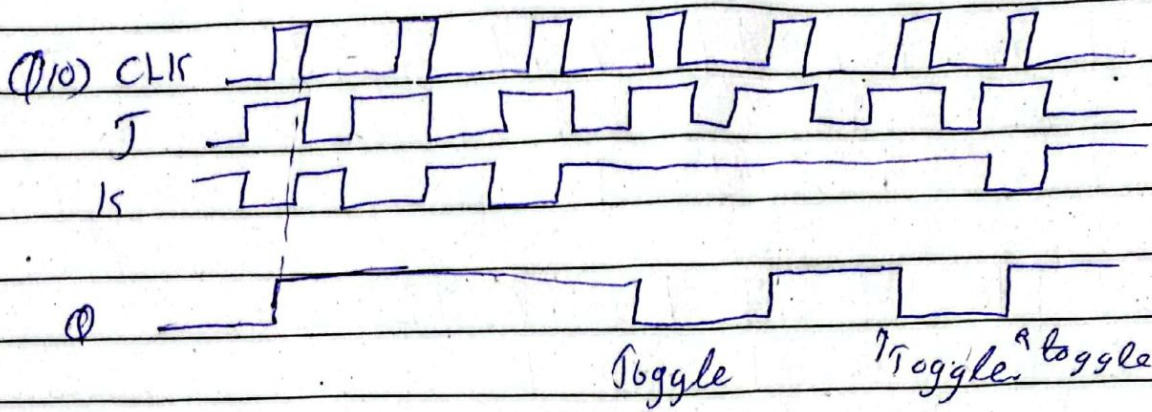


fig 10.





This circuit can be reduce the frequency of CLK as $\frac{f}{2}$, as arrangement comprises of 1 flip flop.

$$\therefore f_1 = f/2$$

Date: _____

Q13

