MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering

6.331 Advanced Circuit Techniques

Laboratory 2
Power Converters

Issued : October 13, 2011
Due : Thursday, October 27, 2011

Design, build, and demonstrate a switching power supply that meets the following specs. (You may choose to build either the boost or flyback topology.)

Specifications

- Output voltage: for the boost 20 V, for the flyback -10 V
- Steady state error: Zero (use an integrator in the loop).
- Output voltage ripple: $\leq$ 200 mVpp (peak-to-peak)
- Input voltage range: 8 V $\leq V_{in} \leq$ 16 V
- Input ripple current (calculated): $\leq$10 mA rms
- Output power: 5 watts
- Small signal bandwidth: $\geq$ 5 kHz
- Small signal step overshoot: $\leq$ 10%

Lab Hints

Build your converter in stages rather than attempting to construct and test the entire loop in one smoke-producing flip of the switch.

1. Build the switching section
    - use ceramic capacitors for the main filtering caps in your converter. Use electrolytics only for damping legs.
    - drive the switch with a function generator (D = 0.5 or whatever)
    - start with a small input voltage (V_{in} = 0.5 V or so)
    - if the waveforms look ok, gradually increase V_{in}
    - use the function generator's symmetry control to vary D, and convince yourself that the converter is operating correctly.
2. Build the controller section

- test the controller section using "fake" inputs
- use lab kit supplies to power controller circuitry (not V_{in} supply)
- verify proper operation before attempting to close the loop

3. Consider start-up details before closing the loop.
   - soft-start
   - current-limit
   - duty-cycle limit
4. Pray, sacrifice a token 3904, then power up the closed-loop system

If you elect to use a fixed-frequency PWM technique, the following circuit may be of interest. (Note that this circuit is intended to drive a N-channel FET referenced to ground. It is not difficult to modify it for use with a P-channel FET referenced to +V.)

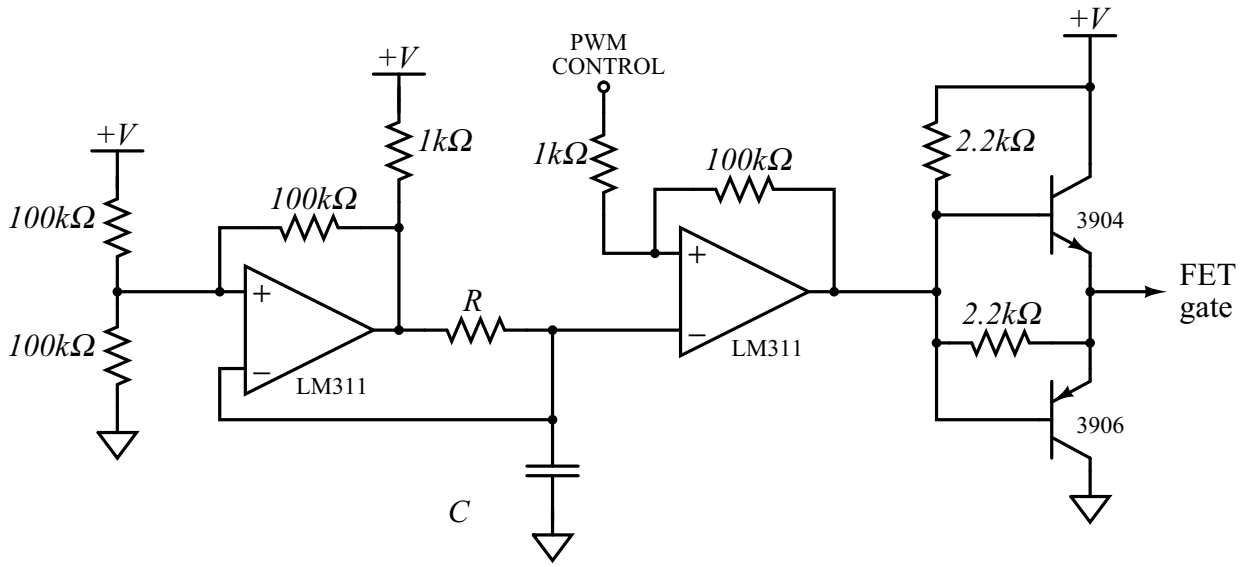

Figure 1: Fixed Frequency PWM Controller

The FET switches used for this lab may be obtained fron the instrument desk. Use the IRFD110 for a N-channel switch, the IRFD9110 for a P-channel switch, and a 1N5818 for the Schottky diode switch. The FET devices are packaged in a 4-pin DIP with the following pinout:

Figure 2: FET pinout

You must wind your own inductors for use in this lab. The toroidal cores for winding these inductors are available from the instrument desk. A partial data sheet for the particular core we are using as well as a design example are included in this handout to aid you in designing your inductors.

Core winding example

Suppose we want a 100 μH inductor which has the capability of supporting peak currents of 0.5 amps. First determine the number of turns required:

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{100\ \mu\text{H}}{52\ \text{nH/turn}^2}} = 44\ \text{turns}$$

Next, decide what size wire to use. The table claims that 43T of #25 wire will fit on the core. This is in fact not true. The manufacturer's table assumes a "unity winding factor", which means that no wasted space has been allotted for insulation thickness or air spaces between adjacent turns. In practice, 44T of #26 wire won't fit, #27 wire would probably work OK. In the lab we only have even wire sizes, so we decide to wind the core with 44T of #28 wire.

We can now estimate the length of wire required and the DC resistance of the finished inductor. If we assume a mean turn length of about 0.05ft, the total length of the winding is 2.2 feet. Adding a little extra for leads and some error margin results in an estimated winding length of 3 feet. #28 wire has a resistance of 65 mΩ/ft, thus the DC resistance of the inductor is approximately 0.2Ω. For a DC current of 0.5 amps, the power dissipation is 50 mWatts, which is no problem.

The permeability of the core (and thus the inductance) will decrease as the inductor current increases. For a DC current of 0.5 amps, the magnetizing force on the core is:

$$H = 0.704NI = 0.704(44)(0.5) = 15.5\ \text{Oe}$$

The graph shows that our inductance will drop to about 93% of the zero bias inductance value. This small variation is not really a problen for our purposes. If the minimum inductance value were critical, an extra turn or two would be required.