**MASSACHUSETTS INSTITUTE OF TECHNOLOGY**
Department of Electrical Engineering

# 6.331 Advanced Circuit Techniques

Fall Term 2011 — Issued : October 6, 2011
Problem Set 4 — Due : Thursday, October 13, 2011

---

**Problem 1** The flyback converter shown in Figure 4.1 is operating in steady state with a constant frequency PWM-type switch drive at a switching frequency of 100kHz.

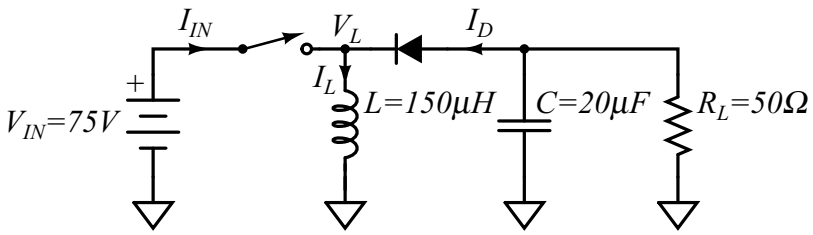


Figure 4.1: Flyback Converter

**A.** Determine the relationship between the output voltage $V_O$, the input voltage $V_I$, and the duty cycle ($D$) of the switch drive. Explain why this topology is sometimes called a "buck-boost" or "up-down" converter.

**B.** Assume that the duty cycle of the switch drive is $D = 0.4$. Determine the average value of $i_{in}$, the average value of $v_{out}$, and the peak-to-peak magnitude of the output voltage ripple. Sketch $i_L$ and $v_L$ for a switching cycle.

**C.** Determine the transfer function which relates the incremental changes in output voltage to a small perturbation in $D$. Comment on the nature of this transfer function.

**D.** Assume the on resistance of the switch is $R_{on} = 1\Omega$, and the forward voltage drop of the diode is $0.35\text{V} + 0.1\Omega i_D$. Estimate the power dissipation in the switch and the diode.

**Problem 2** The buck converter shown in Figure 4.2 utilizes a hysteresis controller to control the average value of the current flowing in the inductor. The characteristics of the hysteresis controller are shown in Figure 4.3.

**A.** Determine the width of the hysteresis band which results in an operating frequency of 250 kHz when $v_{out} = 5$ V. (Assume continuous conduction.)

**B.** For the same width hysteresis band as found in part A, what is the operating frequency for $v_{out} = 7.5$ V? (Note that $I_{set}$ must now be 1.5 amps.) For $v_{out} = 2.5$ V? ($I_{set} = 0.5$ amps.) What happens if $v_{out}$ is less than 2.5 V? ($I_{set} < 0.5$ A).

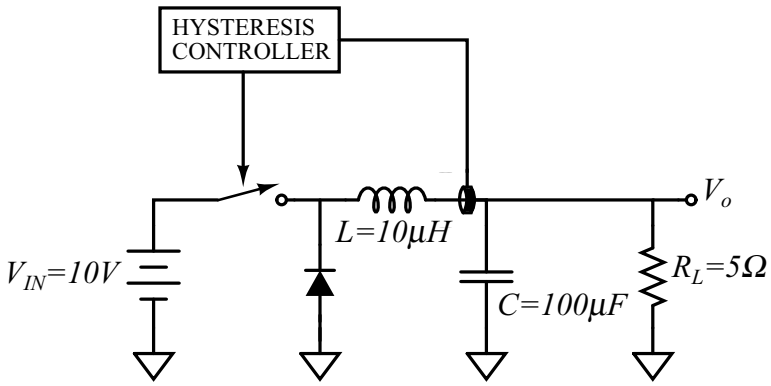


Figure 4.2: Buck Converter with Hysteresis Control of Inductor Current

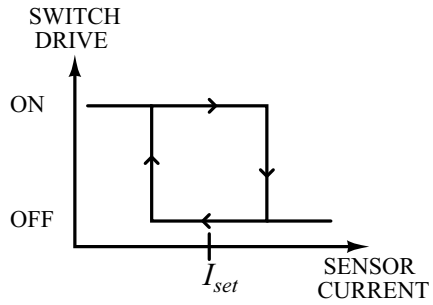


Figure 4.3: Hysteresis Controller Characteristics

**C.** Find the transfer function for the incremental changes in the average output voltage which result from a small perturbation in the value of $I_{set}$. Find a suitable compensator transfer function $G(s)$ which will result in a closed loop system with zero steady-state error, a crossover frequency of $10^5$ rad/sec, and a phase margin greater than 50°. (Don't forget to include a reasonable approximation for the dynamics associated with the inner current control loop.)

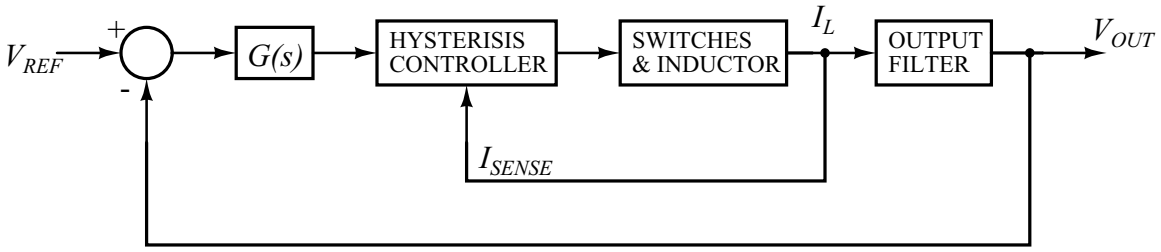


Figure 4.4: Block Diagram of Closed Loop

**D.** The output filter capacitor used in the converter will have a small but non-zero effective series resistance (or ESR). What happens to the response of closed loop system of part C when the capacitor has an ESR of 0.1Ω? Redesign the compensator so that the stability and error specifications from part C are met, and the crossover frequency specification is met or exceeded, for any value of capacitor ESR between 0 and 0.1Ω.

**Problem 3** This problem examines the switching performance of a common base amplifier. The transistor parameters are $\beta_F = 100$, $\beta_R = 5$, $\tau_F = 0.5$ ns, $\tau_R = 1$ ns, and $\tau_S = 7.55$ ns. Ignore the effects of the space charge layers. The transistor is connected as shown in Figure 4.5.

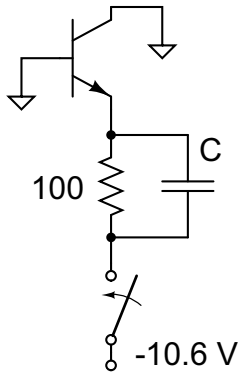


Figure 4.5: Switched-emitter common base amplifier

**A.** Assume that $C = 0$ and $q_F = q_R = 0$ for $t < 0$. The switch is closed at time $t = 0$. Determine equations that describe the growth of $q_F$ and $i_C$ as functions of time.

**B.** The test described above is repeated with capacitor $C$ included. What value of $C$ minimizes the time required for the transistor to reach steady-state values of $q_F$ and $i_C$?

Now suppose the circuit is changed to Figure 4.6 (you may assume that $V_{\text{CEsat}}$ for the transistor is zero).

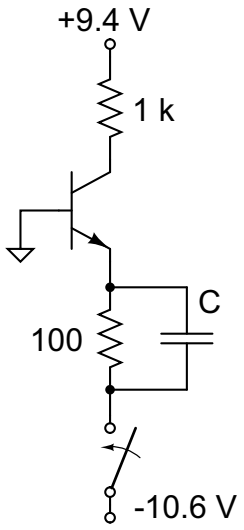


Figure 4.6: Switched-emitter common base amplifier

**C.** Again assume $C = 0$ and $q_F = q_R = 0$ for $t < 0$ and that the switch is closed at time $t = 0$. How long does the transistor remain in the forward-active region?

**D.** The switch is kept closed until the transistor reaches steady state in saturation. What are the values of $q_F$, $q_R$, $q_{B0}$, and $q_S$ in the steady state? (Recall that $q_{B0}$ is the base charge required to get to the edge of saturation.)

**E.** The test described in part C is repeated with capacitor $C$ included. What value of $C$ minimizes the time required to reach steady-state saturation?

**F.** Once steady-state saturation has been reached, the switch is opened. What is the value of $i_B$ immediately after the switch is opened?

**G.** How long after the switch is opened does the transistor remain in saturation?

**H.** Sketch the general form of the base charge distribution shortly after the switch is opened (part F) and at the instant the transistor enters the forward active region (following the time determined in part G).