MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering

6.331 Advanced Circuit Techniques

Fall Term 2011 — Issued : Thursday, September 8, 2011
Problem Set 2 — Due : Thursday, September 15, 2011

Problem 1 Consider the four-diode-switch sample and hold circuit:

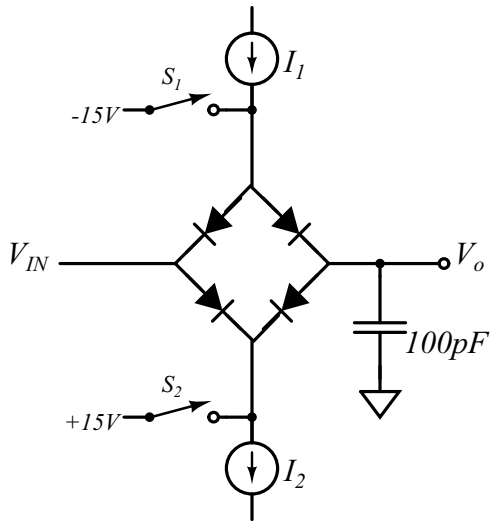

Figure 3.1: Four Diode Switch Circuit

In the sample mode, switches S_1 and S_2 are open, thus allowing the currents I_1 and I_2 to bias the diodes in the usual manner. In the hold mode, S_1 and S_2 are closed. Thus the diodes are reverse biased, insuring a rapid turn-off. This problem investigates the various sources of error inherent in this design. For each source of error, indicate whether it results in an offset error or a scale factor error.

(a) Let $I_1 = 10$ mA, $I_2 = 9$ mA. What is the maximum slew rate of the hold capacitor voltage in both the positive and negative directions? If the circuit is in equilibrium in the sample mode, what is the error caused by the given current imbalance? Use the diode model:

$$i_D = I_S e^{qv_D/kT} \qquad I_S = 10^{-13}\text{A}$$

(b) Assume that $I_1 = I_2 = 10$ mA. How long does it take for this circuit to slew 10 volts? Sample mode is ended when S_1 and S_2 close. If the switches don't close simultaneously, an error is introduced. Evaluate this error for the case in which S_1 closes 1 ns late.

(c) Assume that each diode is shunted by 10pF of stray capacitance. There will be charge dumped through this capacitance when the switches close. Evaluate the effects of this charge dump. Assume that all of the stray capacitances are equal, but the equilibrium output level was +5 V just before the switches were closed.

(d) Assume that $I_1 = I_2 = 10$ mA, and the circuit is in equilibrium in the sample mode. Consider the circuit's response to small changes in v_i. Use an incremental diode model. This analysis is valid as long as $|v_o - v_i|$ is on the order of kT/q. Compute the response to a step change in v_i. What is the 0.1% settling time? What is the response if v_i is a ramp?

Problem 2 The real part of the input impedance of a capacitively loaded emitter follower can be negative. Demonstrate this possibility by calculating the incremental input impedance for the connection shown.

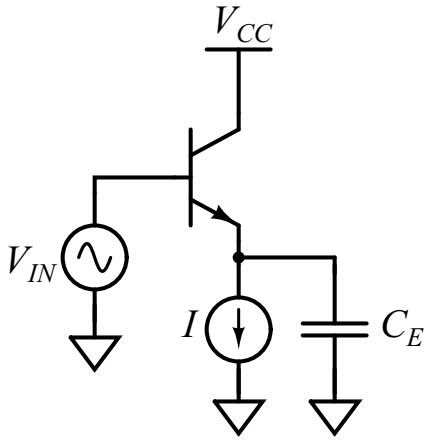

Figure 2.2: Capacitively Loaded Emitter Follower Circuit

Use a simplified incremental model for the transistor, including only r_π, c_π, and g_m.

Also show that for sufficiently large values of C_E, the real part of the input resistance will be positive at all frequencies, and determine the critical value for C_E in terms of transistor parameters.

Sketch plots of the magnitude and phase of Z_{in} for the two cases where C_E is larger and smaller than the critical value determined above.

Problem 3 Consider the problem of minimizing the additive error of a very fast sampler with a long hold time by "ganging-up" a series of sample and holds. For example using a τ_H/τ_S quotient of ten, the first sampler has a sample time of one nanosecond and a hold time of 10ns, the second sampler has $\tau_S = 10$ns and $\tau_H = 100$ns, etc.

Assume that the error of each stage is dominated by hold-time droop, and that it is proportional to the τ_H/τ_S quotient of each stage.

Assume we want a sample time of one nanosecond and a hold time of one second. What is the optimum τ_H/τ_S quotient? How many sample and holds will we need?