MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering

6.331 Advanced Circuit Techniques

Fall Term 2011 — Issued : November 10, 2011
Problem Set 5 — Due : Thursday, November 17, 2011

Phase Locked Loops This problem set illustrates many of the important concepts involved in the design of phase locked loops.

Problem 1 Figure 6.1 illustrates a linearized block diagram for a phase locked loop (PLL). Notice that some of the variables represent a phase (the derivative of phase is frequency), and some of the variables represent voltages. The scale factor for the phase detector is K_D volts/rad. The frequency output from the voltage controlled oscillator (VCO) is

$$\omega_o = \omega_c + K_O V_i$$

thus K_O has units of rad/v-sec.

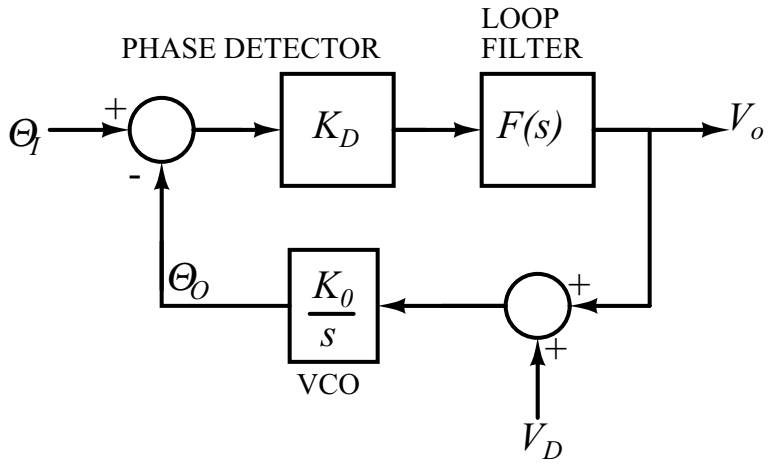

Figure 6.1: PLL block diagram

A. First Order Loop: Assume that the PLL is locked onto an input frequency ω_1 rad/sec away from the VCO center frequency. Let $F(s) = 1$, so the loop transmission will be first order. What is the steady state phase error?

Assume that the phase detector will only function properly over the range $-\pi < \theta_e < +\pi$. How does this limit the operating frequency range (the lock range) of the PLL? If v_D is a constant voltage, what is the lock range?

Sketch a Bode plot of $H(s) = \theta_O(s)/\theta_I(s)$. What is the relationship between the steady state error and the loop bandwidth (i.e. the bandwidth of $H(s)$)?

B. Second Order Loop: Assume that the loop is locked onto an input frequency of ω_1 rad/sec. Let $F(s) = 1/\tau s$. Is this loop stable?

Perhaps a better candidate for $F(s)$ is $(\tau_2 s + 1)/\tau_1 s$. Sketch a Bode plot of the loop transmission. How do you choose τ_1 and τ_2 so that the loop will have a phase margin of 45°? What is the steady state phase error? What is the lock range?

C. Higher Order Loops: Sometimes it is desirable to track linear FM (the input is a ramp in frequency). What does this suggest about the required $F(s)$?

D. Multiplier Phase Detectors: An analog multiplier can be used to implement a phase detector. Assume that the input is $A \sin \omega t$ and the VCO output is $B \sin(\omega t + \theta_e)$.

What is the phase detector output? Assume that the loop will filter out all of the high frequency components. Sketch the output voltage versus the phase error. What is the scale factor of the phase detector?

The multiplier phase detector is used in conjunction with a second order PLL as in part B. Explain how the magnitude of the input signal affects the loop bandwidth and stability.

Let $F(s) = (\tau s+1)^2/s^2$. Assume that the loop is stable for sufficiently large input amplitudes. Use root locus techniques to demonstrate the effects of reducing the input signal amplitude.

E. Finite State Machine Phase Detector :

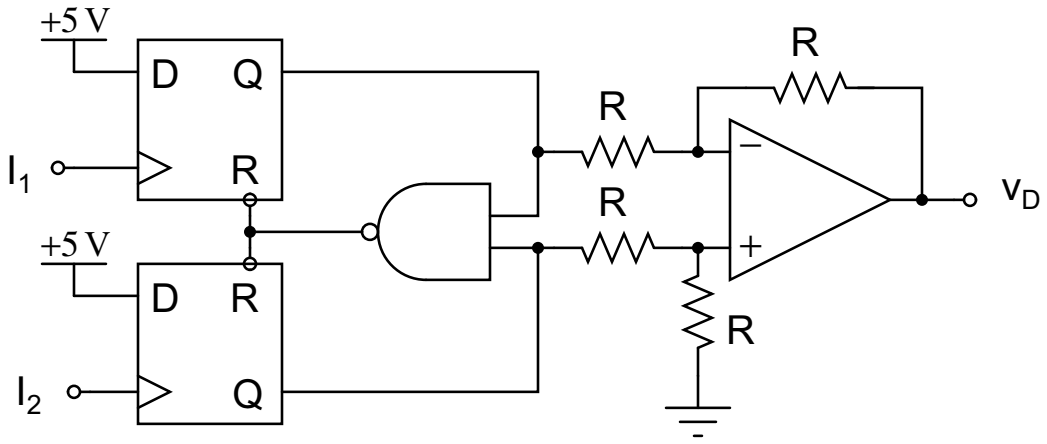

Figure 6.2: FSM phase detector

This circuit uses two "D" flip flops and a NAND gate. Assume that a Logic 1 is +5 V, and a logic 0 is 0 V. For a "D" flip flop, the Q output is set equal to the D input on the rising edge of the clock input, and is set equal to 0 when the reset input is 0.

Assume that I_1 and I_2 are 5 volt square waves of frequency ω_0. Relate the average value of v_{out} to the phase difference between I_1 and I_2. What is K_D? What is the maximum allowable range of phase shift?

If this phase detector is used in a PLL, which input (I_1 or I_2) should be connected to the VCO output? (Assume that the VCO output frequency increases when the average value of vout increases.)

F. Many State Machine Phase Detector :

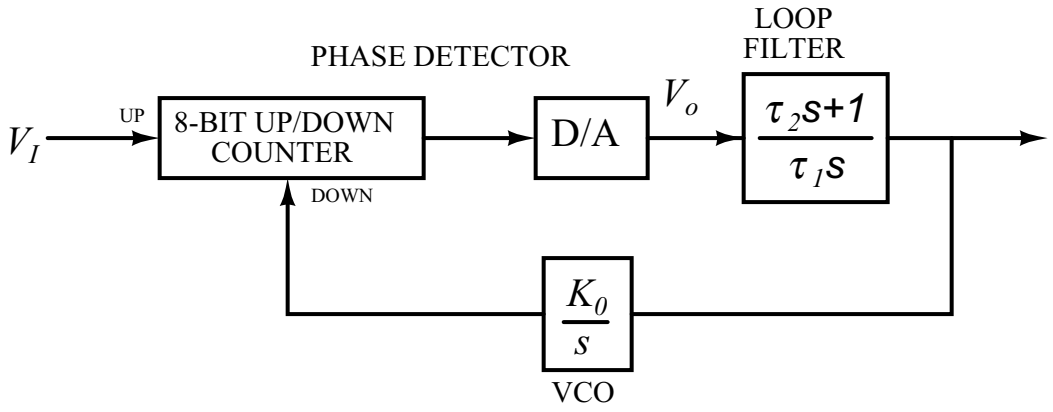

Figure 6.3: Alternative Digital Phase Detector

This circuit employs an 8-bit up/down counter and a D/A converter. Assume that the VCO output and the input are both square waves. The counter increments for each input pulse and decrements for each VCO pulse. The range of v_O is ± 10 volts.

When the loop is locked, what is the average value of v_O? What is K_D? What is the allowed range of phase error?

G. Noise: Digital phase detectors may be useful even if the input signal is not a square wave. Typically, a comparator is used to detect each zero-crossing of the input signal, thus 'squaring up' the input. Assume that the input is processed by an infinite gain comparator.

(Answer the following questions qualitatively.) Describe the operation of the digital phase detector if the input is a sine wave plus noise. How does this affect the loop behavior? How can this situation be improved if the noise is small compared to the signal? Would a multiplier phase detector perform better in a noisy enviornment?

H. Spectral Purity: Consider the effects of an inferior VCO. Specifically, assume that the VCO has a certain amount of phase jitter. This can be modelled by injecting a disturbance at the point labelled v_D in the diagram of Figure 6.1 and then assuming that the VCO is "clean". What is the output jitter θ_O if the loop is locked to a clean input signal? Consider the transfer function $\theta_O(s)/v_D(s)$. How is the output jitter related to the loop bandwidth and gain?

Problem 2 Consider the PLL shown below:

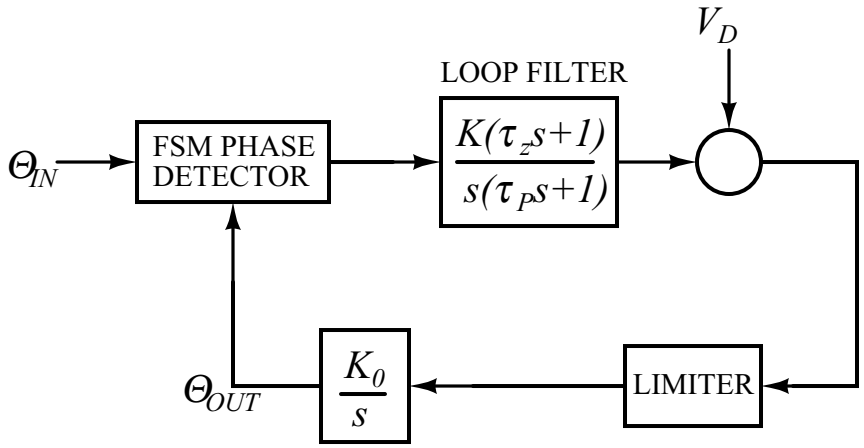

Figure 6.4: PLL block diagram

The FSM phase detector is the same as the one examined in problem 1E (see Figure 6.2). The limiter "clips" its input signal such that its output lies within the range 2 V≤output≤10 V. The VCO has a transfer function of K_O/s.

A. VCO: Assume the VCO operates as $\omega_o = K_O V_i$. Determine K_O, such that the maximum VCO output frequency is 50 kHz. What is the lock range of the PLL? With no signal supplied to the input, what is the VCO frequency?

B. Loop Filter: Consider a loop filter of the form

$$F(s) = \frac{K(\tau_Z s + 1)}{s(\tau_P s + 1)}$$

Let $\tau_P = 2$ ms (a pole at 500 rad/sec). Choose values for K and τ_Z such that the loop has a crossover frequency of 100 rad/sec and a phase margin of 45°. (Keep these values for the remainder of the problem.)

C. Aquisition Time: Assume that the loop is initially in equilibrium and locked to an input signal at the low end of the lock range. The input frequency is then changed (in a step-like manner) to a frequency at the high end of the lock range. Approximately how long does it take for the loop to acquire lock after the step change?

D. Loop Dynamics: A convenient way to measure the dynamic characteristics of the loop is to inject a small disturbance v_D and observe the effects at the VCO input. If you assume that the loop is sufficiently "second order-like," you can use Figure 4.26 in Operational Amplifiers to estimate the risetime and peak overshoot of the loop. Based upon this approximation, what values do you estimate for the risetime and peak overshoot for this loop?