Sujatha Kashyap, Ph.D.

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Summary

20+ years of experience in the US technology industry, spanning engineering roles to engineering management and business roles across Fortune 100 companies, startups and research labs. Extensive experience across the entire silicon lifecycle - design, validation, verification, bring-up and post-silicon benchmarking for enterprise and consumer chips, including working with external vendors and troubleshooting customer installations. Relocated to Bangalore for family reasons.

Experience

(Relevant experience first)

SEP 2021 - OCT 2022

Meta (Facebook), Austin, TX
Engineering Manager,
AR SoC Performance, Reality Labs

Supported a team of engineers responsible for end-to-end system modeling, SoC architecture exploration, use case PnP (power and performance) analysis, micro-architecture modeling, and PnP verification of custom SoCs for AR/VR. The chips were designed and manufactured in partnership with Samsung Foundry.

MAY 2016 - JAN 2019

IBM, Austin, TX
Program Director, Power Processor Performance (2018- 2019)

Led a team of 90 engineers across the US, Canada, India and China responsible for three major deliverables:

(1) Design guidance for the IBM chips and systems roadmap, for both accelerated and non-accelerated systems, based on workload analysis, performance modeling and competitive analysis.

(2) Software stack optimization, including operating systems, middleware and key ISV applications. Compiler and library optimization to ensure peak performance on POWER chips and systems, including GPU-enabled systems.

(3) Performance engineering and collateral for new releases of POWER chips and systems, including certification for key ISV applications such as SAP HANA.

Manager, IBM Austin Research Lab (2016- 2018)

Led the design and implementation of a Science for Social Good project called Simpler Voice - a mobile app targeted at enabling low-literacy adults to understand complex written instructions by transforming them into simpler messages with accompanying illustrative images using deep learning techniques for natural language understanding and narrative summarization, and generative adversarial networks for image generation.

Publications:

1) Can AI Solve Poverty? Communications of the ACM, Sep 5 2017, https://cacm.acm.org/news/220776-can-ai-solve-poverty/fulltext

2) SimplerVoice: Overcoming Illiteracy. Minh N.B. Nguyen, Samuel Thomas, Anne E. Gattiker, Sujatha Kashyap, Kush R. Varshney, Neural Information Processing Systems (NIPS) - Women in Machine Learning Workshop

3) SimplerVoice: A Key Message & Visual Description Generator System for Illiteracy. Minh N. B. Nguyen, Samuel Thomas, Kush R. Varshney, Sujatha Kashyap, and Anne E. Gattiker. Data for Good Exchange, New York, NY, September 2018.

JAN 2001 - MAY 2014

IBM, Austin, TX

Staff Engineer (Band 7) to Senior Technical Staff Member (Band 10),
Power Processor Design and Performance

A varied technical career touching all aspects of chip and system engineering, from writing VHDL to full-stack performance optimization. Key highlights:

Chief Performance Architect, POWER9 chips and systems

Led a cross-organizational team of performance modeling engineers and workload specialists to collaborate with chip and system architects in designing the POWER9 family of chips and systems, including GPU-enabled systems.

Chief Performance Architect, SAP HANA on POWER

Led the SAP HANA port to the POWER architecture, delivering 2x performance per core compared to x86 systems. This result convinced SAP executives to add POWER as a HANA-certified platform, which has since resulted in over $500M of revenue for IBM.

Hardware Architect, POWER8 Processor

Led the pre-silicon performance verification of key differentiating features on the POWER8 system-on-a-chip, including the Coherent-Attached Processor Interface, virtualization assists, and on-chip hardware accelerators. Designed and implemented key functions on the memory buffer chip for POWER8-based systems.

(Other experience)

MAR 2019 - DEC 2019

CS-DISCO, Austin, TX

Chief Performance Architect

One of Austin's hottest startups, DISCO provides a cloud-based e-discovery solution for legal firms. Its competitive advantage is blazing speed, powered by a highly distributed cloud-native architectureAs Chief Performance Architect, I was responsible for meeting key performance targets for DISCO, and working with various engineering teams to speed up the platform to provide a wait-free "magical" user experience.

NOV 2014 - JAN 2016

Robin.io (a Rakuten Symphony Company), San Francisco Bay Area
VP of Products

Led the product and technology strategy for this seed stage Silicon Valley startup aimed at automating large-scale Big Data deployments in the cloud by creating virtual clusters using containerization, orchestration, and software defined storage and networking. Led the proof of concept that led to its first Fortune 50 customer acquisition, and a successful Series A funding round of $22M. The company was subsequently acquired by Rakuten Symphony.

Education

2002-2008

University of Texas at Austin, Austin, TX - *Ph.D., Computer Engineering*

Dissertation: Applications of Lattice Theory to Model Checking Distributed Systems

1998-2000

Texas A&M University, College Station, TX - *M.S., Computer Science*

1994-1998

NIT-K (formerly KREC), Surathkal, Karnataka, India - *B. Tech., Computer Engineering*

Patents

32 issued US patents spanning hardware architecture, operating systems, software architecture and AI.

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