# Shivraj Thakare


## CONTACT ME AT

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LinkedIn


Senior Director, bringing substantial experience in managing Analog IP and subsystem integration. Desire is to obtain a **leadership roles in Analog IP, Subsystem design services, SOC/Logic Design, Physical Design Engineering, and Post-Si Engineering**. Proven track record in developing and launching next-generation memory technology for leading tech companies.

## EDUCATION

- M. Tech. (Microelectronics), IIT Kanpur, India March 1998.
- B. Tech. (Electronics), SGGS college, Nanded MH, India June 1994.

## CORE COMPETENCIES

### Analog IP Management Skills

- Analog IP Portfolio Management
- Analog Design and Validation
- IP subsystem hardening
- Post-Si and Post Launch Support
- Memory Technology Development
- IP Function Team Management (Analog, LAY, Logic, and PD)
- IP Market Trend Analysis
- IP Quality Management

### Organizational Skills

- Customer and Supplier Engagement
- Strategic Hiring and Retention
- Team Building, Mentoring & Leadership
- Recruitments & Trainings
- Performance Management
- Cross-Functional Collaboration

## PROFILE SUMMARY

- Strategic Professional, **presenting decades of experience in India and US in Analog IP and Sub-system Design Services Management**, Physical Design and Logic Design/Verification, showcasing a diverse range of experiences.
- Currently **spearheading the development & launch of cutting-edge DDR Phy memory technology for Intel server products,** showcasing expertise in managing large analog and design services teams and overseeing all functions related to analog Ips and Subsystem.
- **Possess expert knowledge and hands-on experience in:**
  - **Analog IP Management**: Overseeing the entire lifecycle of Analog IP projects and ensuring technical excellence and innovation in design and implementation; acting as a primary liaison with stakeholders, ensuring high-quality analog IP solutions for multiple analog IP(s) such as DDR, HBM, PCI, SATA, MIPI and VR.
  - **Physical Design Engineering:** Overseeing implementation of complex Analog IP and Memory Subsystem Digital Partitions and collaborating with various cross-functional teams, including Analog, logic and SOC Teams. The ownership extends into the IP subsystem design services for testChip. I owned the subsystem delivery to testChip and SOC team
  - **SOC/Logic Design and Verification**: Overseeing the Logic design & verification of complex Analog IP and subsystem design, ensuring design meets all functional requirements
  - **Post-Silicon Engineering**: Providing strategic leadership & technical oversight for the IP post-silicon validation, characterization, and bring-up of Analog IPs. Ensuring that IP meets design specifications.
- Adept at **strategic hiring, organizational management, and team leadership**, with a keen eye for building and nurturing large analog teams.
- Recognized for exceptional skills in **Analog Design and Validation, Physical Design, IP subsystem hardening, Post-Si Validation & Logic Validation**
- **Differentiators & Success Levers:** result-oriented professional with established skills in people management, relationship building, networking, coaching & mentoring, negotiation, critical thinking, mindfulness and leadership acumen

## WORK EXPERIENCE

**Mr'24 – Till Date: Senior Director, Analog IP and Subsystem Engineering, Intel Bangalore**

**2017 – 2023: Engineering Director, Analog IP Engineering, Intel Bangalore**

- Leading the innovation rollout of cutting-edge DDR Phy and proprietary memory solutions for Intel's server product line, managing the DDR IP portfolio, hardening of the IP subsystem to test chip and SOC.
- Partnering with the memory technology ecosystem and developing DDR and MRDIMM Phy subsystem through test vehicle to validate the DDR Phy architecture and memory ecosystem.
- Oversaw the execution of Analog IPs (DDR/MRDIMM/HBM) on multiple process nodes for Intel datacenter and graphics products. The work extends into the IP subsystem integration and delivery to TestChip
- Established and led linear IP analog teams (VR, BGR) from inception to 50 DE(s), delivering linear IPs for server applications.
- Led the Analog Team to design cutting-edge analog blocks for analog IPs, such as Die-2-Die, HBM, VR, and Sensors, driving innovation and product differentiation.

**2011 – 2017: Serdes IP team Manager, Intel Bangalore**

- Successfully led the transformation of the IP team from Parallel IO to serial IO.
- Managed SATA3 IP development on 14nm for Intel Micro-Server product.
- Directed the team's new charter of porting the Serial IO Phy from Intel to TSMC process for system interconnect (UPI). This work includes the FAB and TC engagement.
- Steered the IP team to develop the Display Port (DP) Phy. Lead the Display Phy development (DP, eDP, HDMI) on multiple process nodes for Intel Client products.
- Inspired team to develop the MIPI/EDP/DP combo Phy.
- End to end ownership of SATA/UPI/DP Phy from Spec definition to IP execution to Post-Si support to productization of IPs

**2007 – 2011: DDR Memory IP, Tech Lead, Intel Bangalore**

- Relocated to Intel India, led the DDR3 IP Post-Si EV team.
- Led E2E post-SI VAL of DDR3 IP including circuit and margin, post-Si debug, and post-launch support on Intel Client product.
- Solved multiple problems at external customer (OEM) side and provided the solution on client program
- Managed the analog design & execution on next generation DDR3 IP for client products.

**2004 – 2007: Memory Phy IO Design Engineer, Intel Folsom, CA, USA**

- Participated in DDR2 IP for Intel client products and owned analog building blocks (TX, clocking & Compensation) design, validation, mask design supervision, and post-layout performance closure.
- Managed the post-SI debug and circuit characterization.
- Monitored DDR2 Phy execution, coordinating across functions like logic design, circuit design, and physical design.

**2000 – 2004: Physical Design Engineer, SUN Microsystems, Sunnyvale, CA, USA**

- Owned several partitions, from RTL to GDS of multiple digital blocks in the data cache unit of ultra-spark5, including design of the PD flow from synthesis to GDS in consultation with DA team, owning several partitions from RTL to GDS, providing feedback on timing to RTL, and meeting the milestone of partitions.

**1998 – 2000: SRAM Design Engineer, Alliance Semiconductor, Bangalore**

- Led analog building block design for the embedded SRAMs as well as CAM memories on 130nm technology.