Bahria University,
Karachi Campus

LAB EXPERIMENT NO.
12

LIST OF TASKS

TASK NO	OBJECTIVE
01	Implement 8 – 3 line encoder and 3 – 8 line decoder on Multisim.
02	Implement 2 to 4 lines decoder with an active low enable and active low outputs on Multisim by making use of NAND gates and inverters. The line of reasoning should be that: - All outputs will be high if enable pin is high i.e. the IC will be disabled. - Chip will be enabled only when enable is low. - Once the chip is enabled, output corresponding to the address pins will be low and the rest of all outputs will be high.
03	Implement an encoder circuit in Multisim based on the following table for encoding numbers.

Number	0	1	2	3	4	5	6	7
Encoded to	4	6	3	0	2	7	1	5

Submitted On:
Date: 17/12/2025

Task No. 01:

"**Implement 8 – 3 line encoder and 3 – 8 line decoder on Multisim.**"
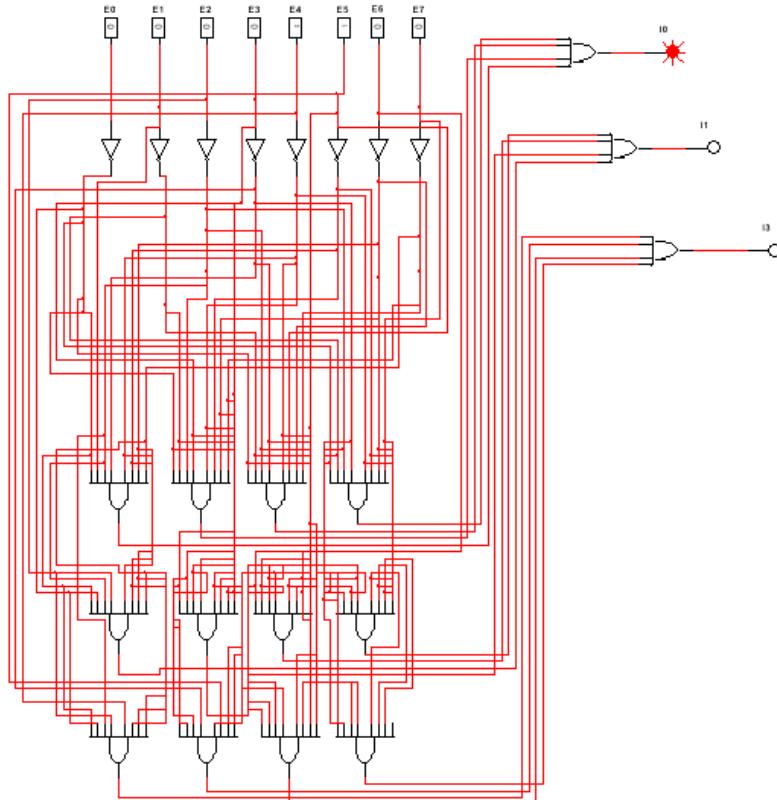
Solution:

3-8 Line Encoder:

E7	E6	E5	E4	E3	E2	E1	E0	I2	I1	I0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$I0 = E_7'E_6'E_5'E_4'E_3'E_2'E_1E_0' + E_7'E_6'E_5'E_4'E_3E_2'E_1'E_0' + E_7'E_6'E_5E_4'E_3'E_2'E_1'E_0' + E_7E_6'E_5'E_4'E_3'E_2'E_1'E_0'$

$I_1 = E_7'E_6'E_5'E_4'E_3'E_2E_1'E_0' + E_7'E_6'E_5'E_4'E_3E_2'E_1'E_0' + E_7'E_6E_5'E_4'E_3'E_2'E_1'E_0' + E_7E_6'E_5'E_4'E_3'E_2'E_1'E_0'$

$I_2 = E_7'E_6'E_5'E_4E_3'E_2'E_1'E_0' + E_7'E_6'E_5E_4'E_3'E_2'E_1'E_0' + E_7'E_6E_5'E_4'E_3'E_2'E_1'E_0' + E_7E_6'E_5'E_4'E_3'E_2'E_1'E_0'$

3-8 Line Decoder:

I2	I1	I0	E7	E6	E5	E4	E3	E2	E1	E0
0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	1	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0

$$E_0 = I_2'I_1'I_0'$$

$$E_1 = I_2'I_1'I_0$$

$$E_2 = I_2'I_1I_0'$$
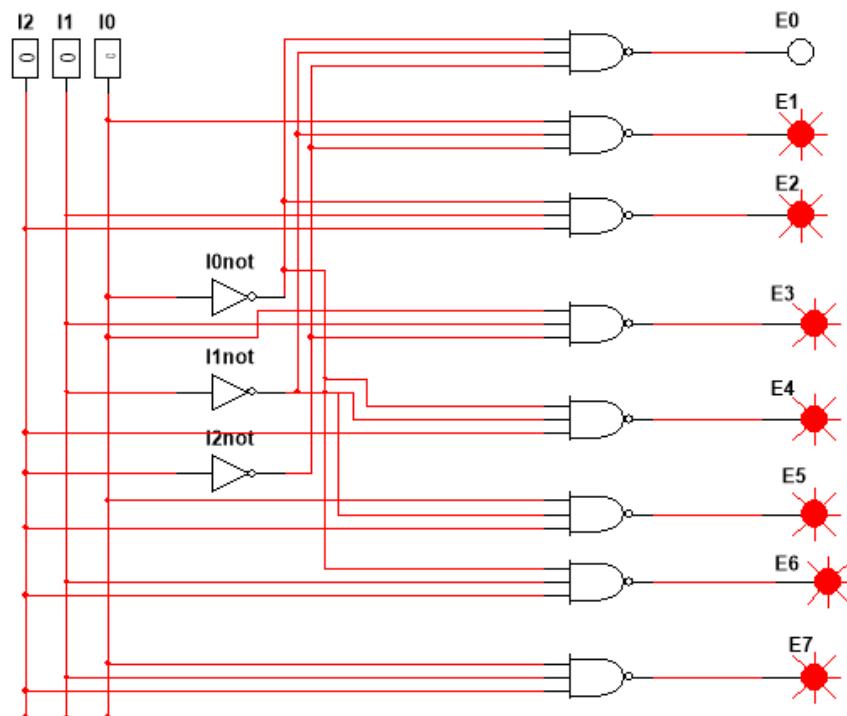
$$E_3 = I_2'I_1I_0$$

$$E_4 = I_2I_1'I_0'$$

$$E_5 = I_2I_1'I_0$$

$$E_6 = I_2I_1I_0'$$

$$E_7 = I_2I_1I_0$$

Task No. 02:

Implement 2 to 4 lines decoder with an active low enable and active low outputs on Multisim by making use of NAND gates and inverters. The line of reasoning should be that:

- **All outputs will be high if enable pin is high i.e. the IC will be disabled.**

- **Chip will be enabled only when enable is low.**

- **Once the chip is enabled, output corresponding to the address pins will be low and the rest of all outputs will be high.**

Solution:

8-3 Line Encoder:
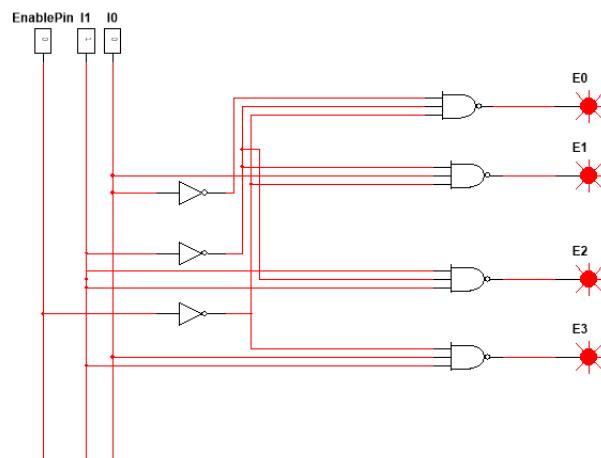
Enable Pin	I1	I0	E3	E2	E1	E0
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

$$E_0 = (I_1'I_0')'$$

$$E_1 = (I_1'I_0)'$$

$$E_2 = (I_1I_0')'$$

$$E_3 = (I_1I_0)'$$

8-3 Line Decoder:

A7	A6	A5	A4	A3	A2
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	0
1	0	0	0	0	0

A1	A0	I2	I1	I0
0	1	1	0	0
1	0	1	1	0
0	0	0	1	1
0	0	0	0	0
0	0	0	1	0
0	0	1	1	1
0	0	0	0	1
0	0	1	0	1

$I2 = A7'A6'A5'A4'A3'A2'A1'A0 + A7'A6'A5'A4'A3'A2'A1\ A0' + A7'A6'A5\ A4'A3'A2'A1'A0' + A7\ A6'A5'A4'A3'A2'A1'A0'$

$I1 = A7'A6'A5'A4'A3'A2\ A1'A0' + A7'A6'A5'A4'A3'A2'A1\ A0' + A7'A6'A5'\ A4\ A3'A2'A1'A0' + A7'A6'A5\ A4'A3'A2'A1'A0'$

$I0 = A7'A6'A5'A4'A3'A2\ A1'A0' + A7'A6\ A5'A4'A3'A2'A1'\ A0' + A7'A6'A5\ A4'A3'A2'A1'A0' + A7\ A6'A5'A4'A3'A2'A1'A0'$