Bahria University,

Karachi Campus

LAB EXPERIMENT NO.

09

LIST OF TASKS

TASK NO	OBJECTIVE
1.	Verify the functionality of NOT, AND, OR, XOR, NAND, NOR, and XNOR Gates using MultiSim by designing the gates and creating their associated Truth Tables. Attach circuit snapshots and Truth Table illustrations for verification.
2.	Implement the following equations on MultiSim and verify through Truth Table. (Attach the circuit snapshots) a. (AB) (A + C) b. AB + BC (B+C) c. ABC' + AB'C + A'BC d. (A' + B + C) (A + B' + C) (A + B + C') e. A' (A + B) + B' (A' + B')

Submitted On:

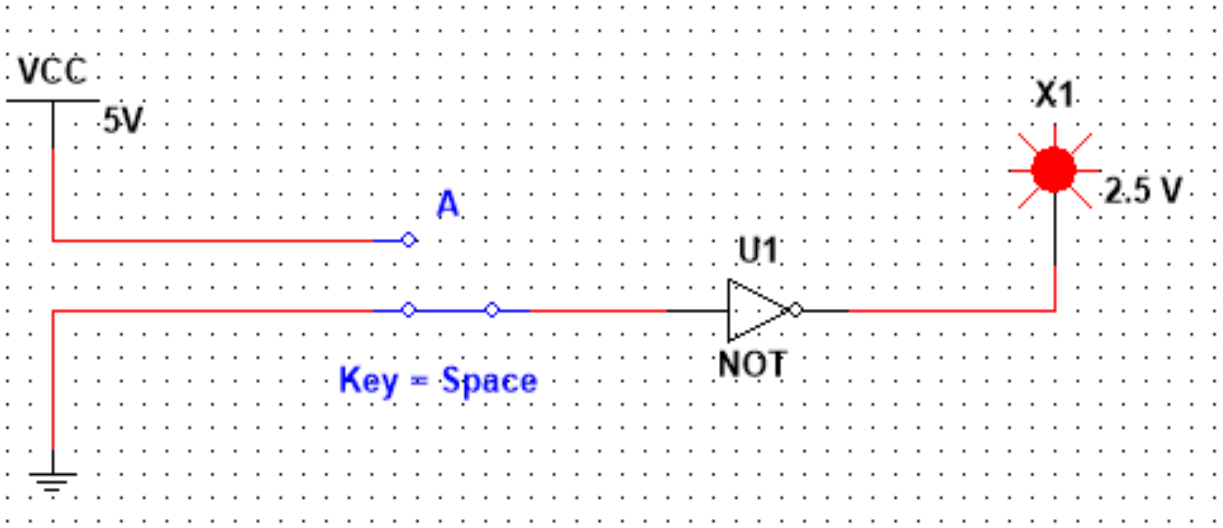
Date: 21/11/2025

Task No. 01:

"Verify the functionality of NOT, AND, OR, XOR, NAND, NOR, and XNOR Gates using MultiSim by designing the gates and creating their associated Truth Tables. Attach circuit snapshots and Truth Table illustrations for verification."

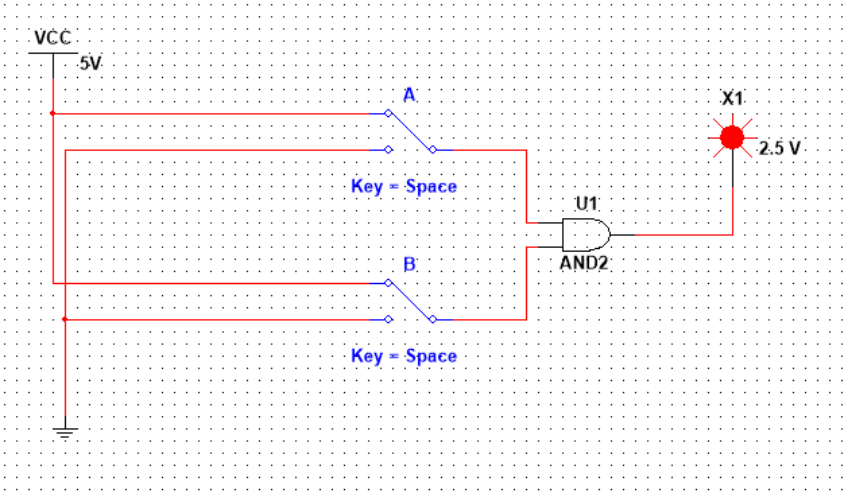
Circuit Snapshots:

Not gate:



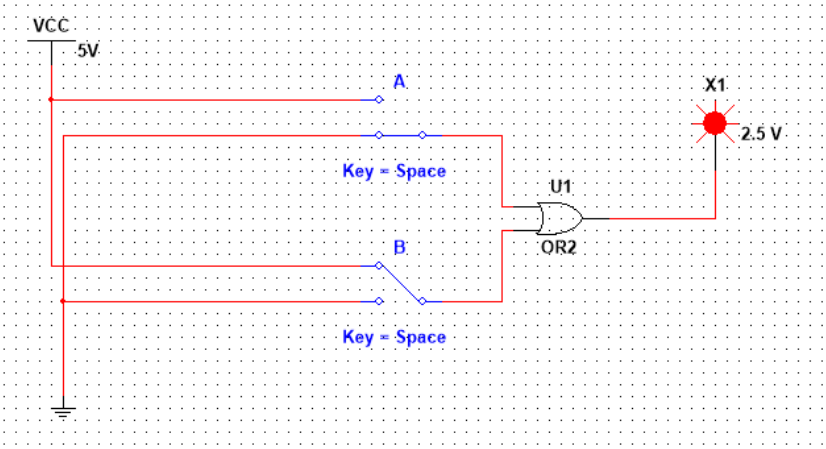
A	not A
0	1
1	0

AND gate:



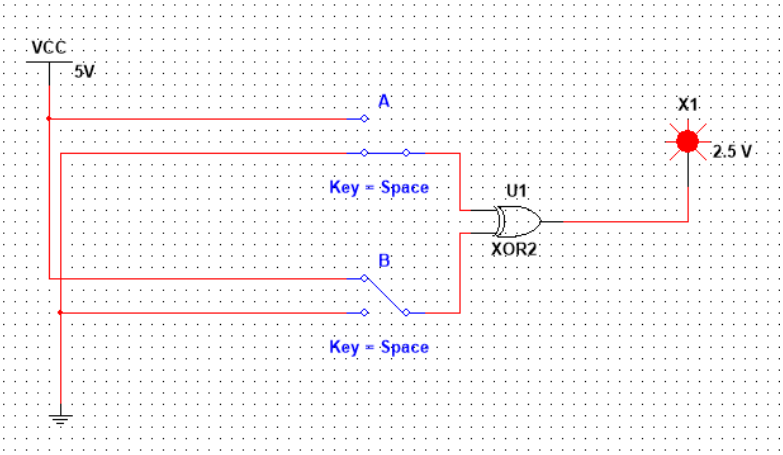
A	B	A and B
0	0	0
0	1	0
1	0	0
1	1	1

OR gate:



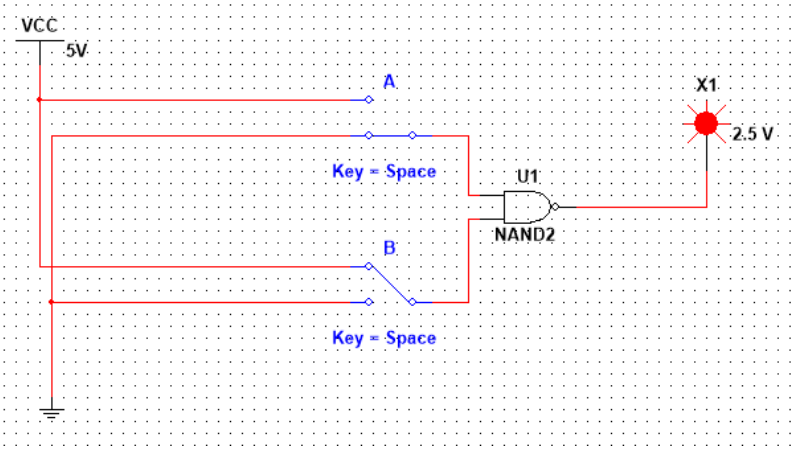
A	B	A or B
0	0	0
0	1	1
1	0	1
1	1	1

XOR gate:



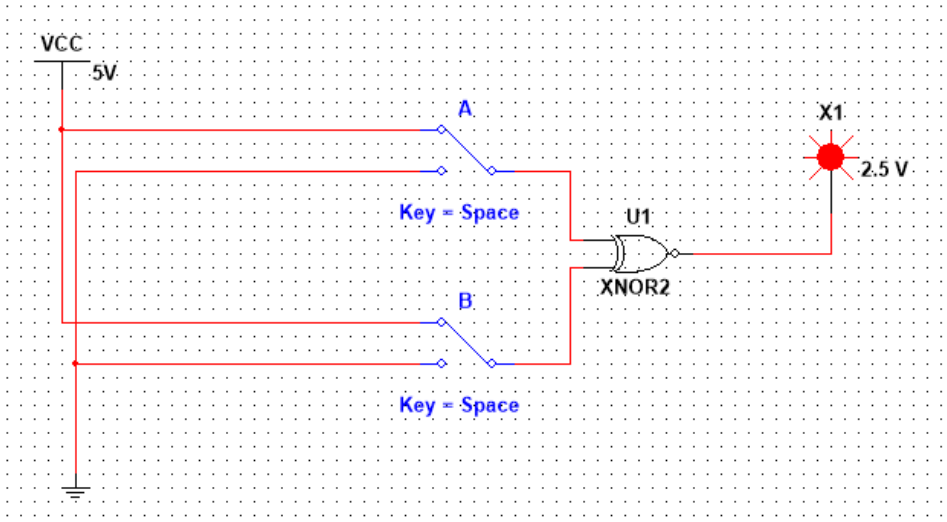
A	B	A xor B
0	0	0
0	1	1
1	0	1
1	1	0

NAND gate:



A	B	A nand B
0	0	1
0	1	1
1	0	1
1	1	0

XNOR gate:



A	B	A nor B
0	0	1
0	1	0
1	0	0
1	1	0

Task No. 02:

Implement the following equations on MultiSim and verify through Truth Table. (Attach the circuit snapshots)

a) **(AB) (A + C)**

b) **AB + BC (B+C)**

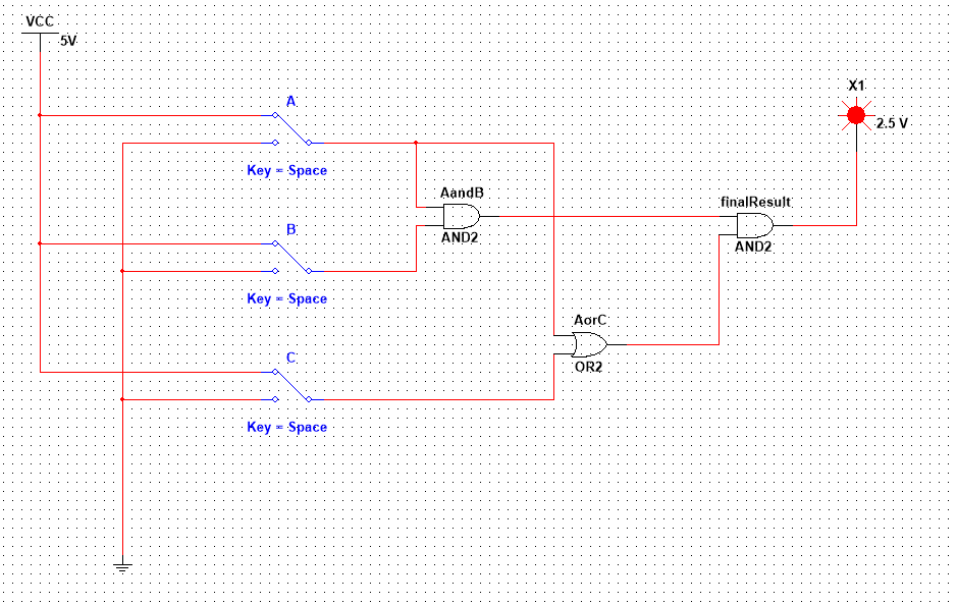
c) **ABC' + AB'C + A'BC**

d) **(A' + B + C) (A + B' + C) (A + B + C')**

e) **A' (A + B) + B' (A' + B')**

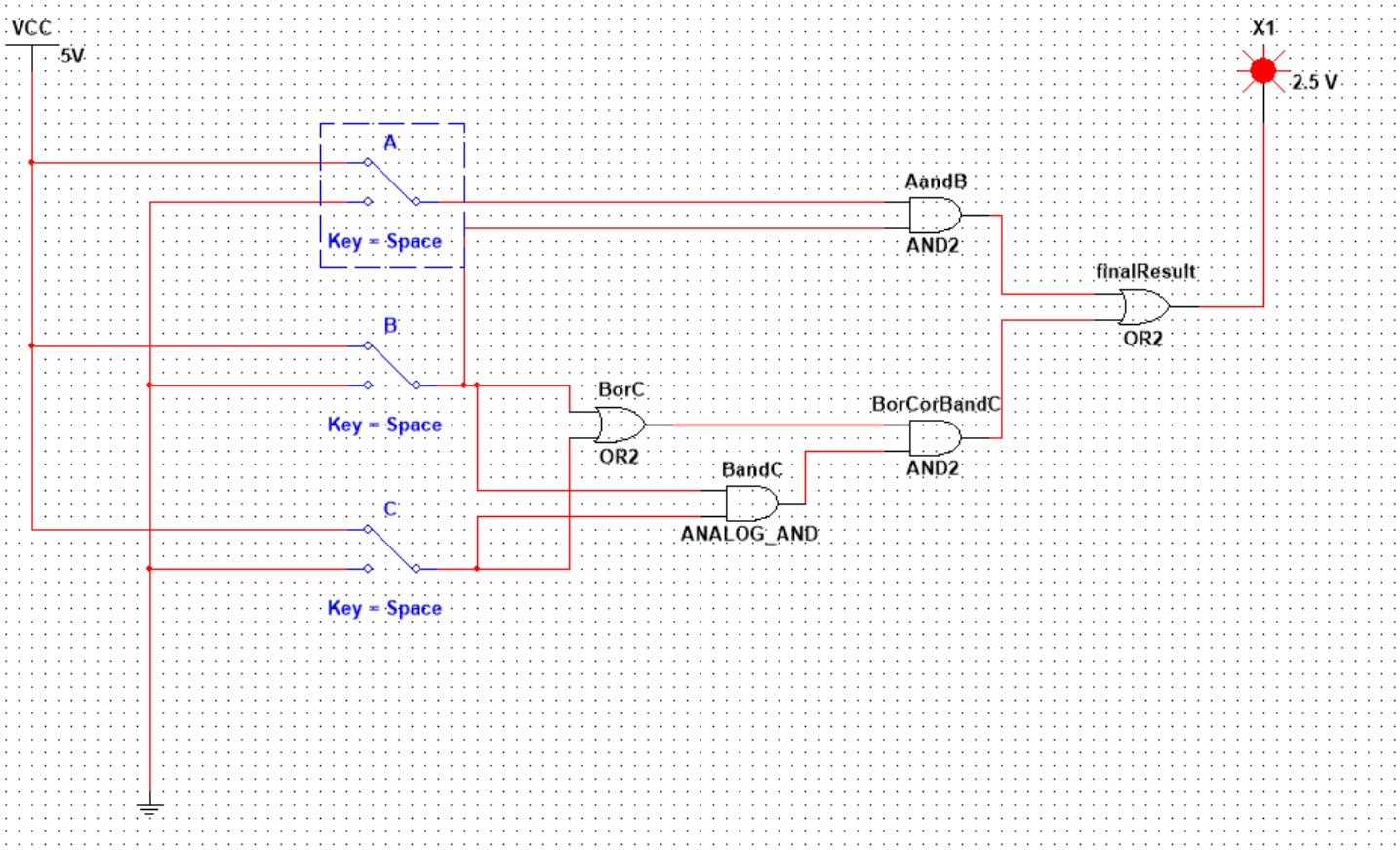
Circuit Snapshots:

(AB)(A+C):



A	B	C	A+C	AB	(AB)(A+C)
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	1

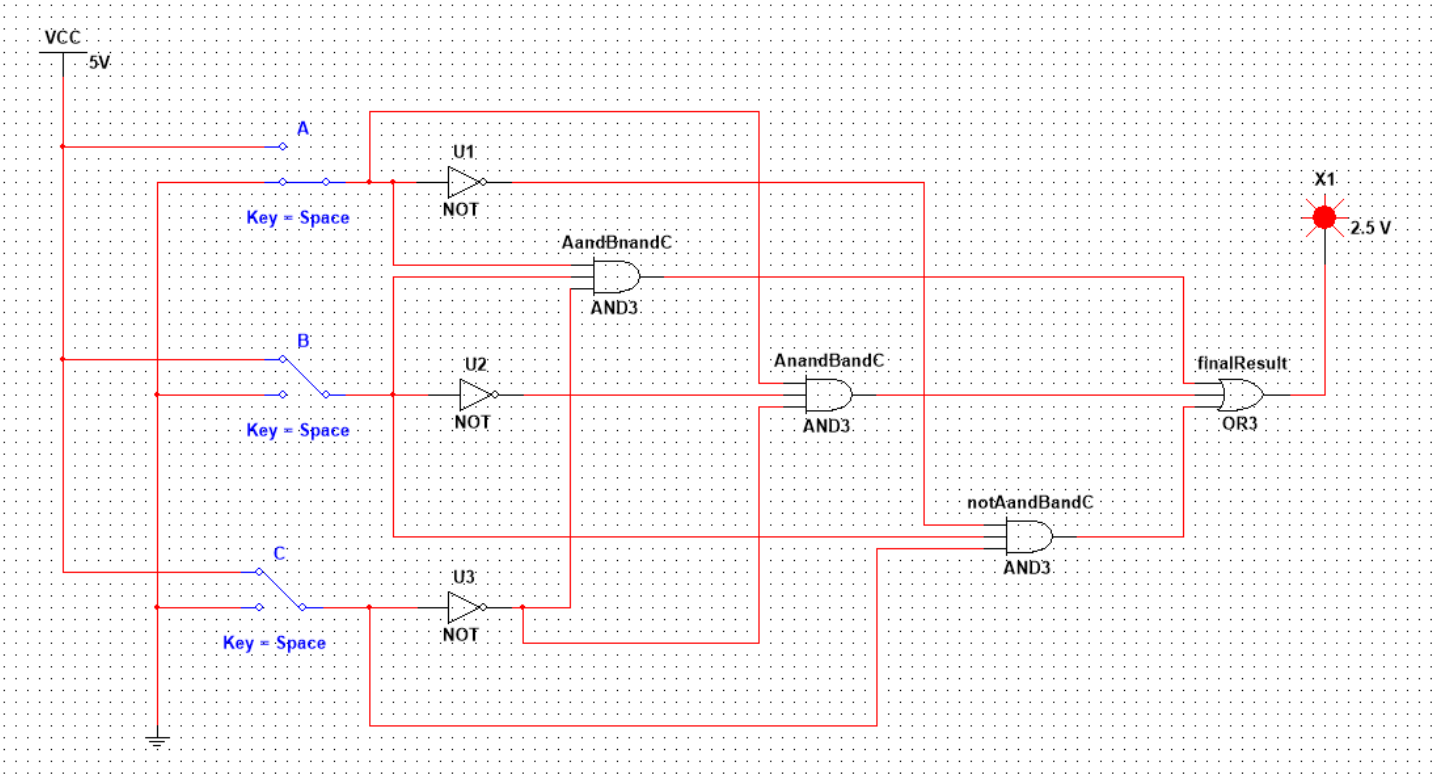
AB+BC(B+C):



A	B	C	B+C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

BC	BC(B+C)	AB	AB+BC(B+C)
0	0	0	0
0	0	0	0
0	0	0	0
1	1	0	1
0	0	0	0
0	0	0	0
0	0	1	1
1	1	1	1

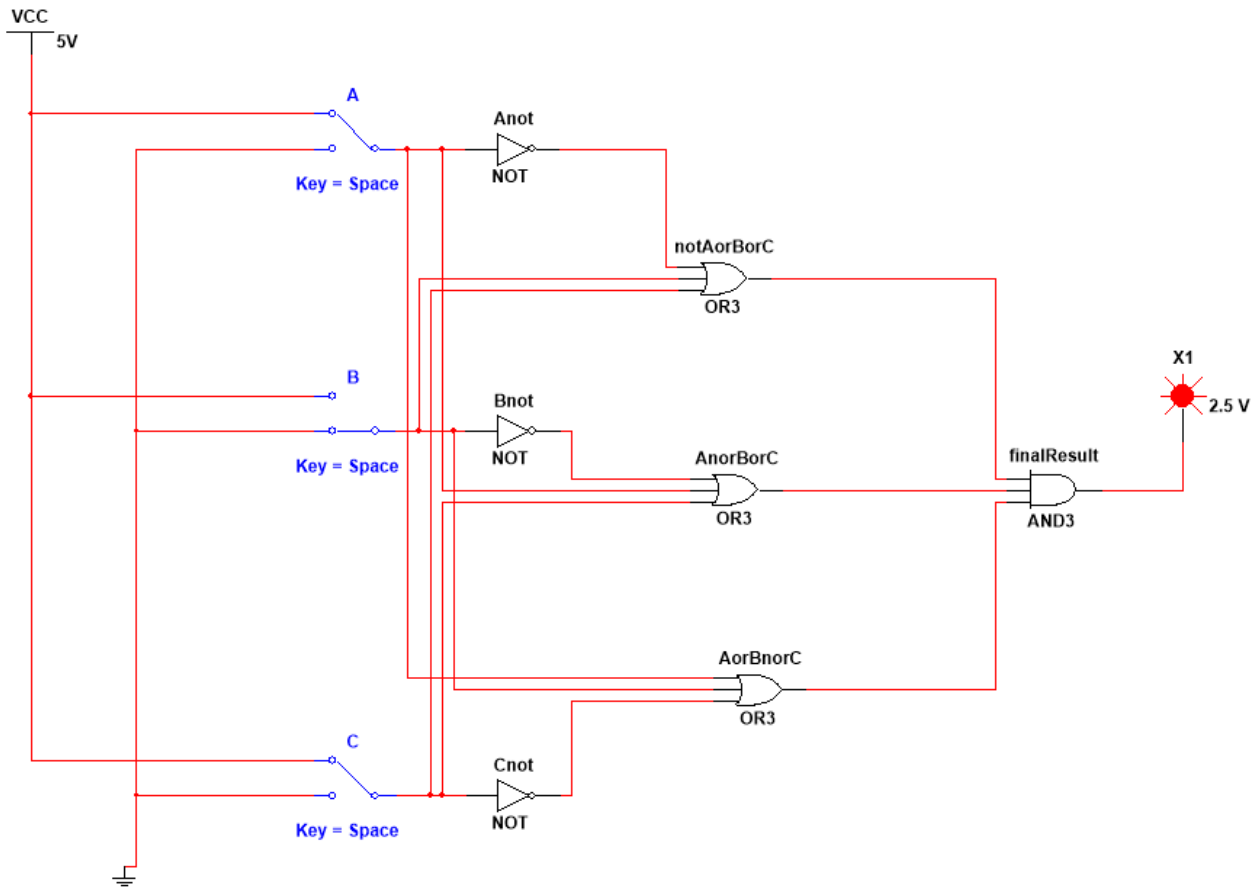
ABC' + AB'C + A'BC :



A	B	C	A'	B'	C'	AB
0	0	0	1	1	1	0
0	0	1	1	1	0	0
0	1	0	1	0	1	0
0	1	1	1	0	0	0
1	0	0	0	1	1	0
1	0	1	0	1	0	0
1	1	0	0	0	1	1
1	1	1	0	0	0	1

A'BC	AB'	AB'C	A'B	ABC'	ABC' + AB'C + A'BC :
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	1	0	0
1	0	0	1	0	1
0	1	0	0	0	0
0	1	1	0	0	1
0	0	0	0	1	1
0	0	0	0	0	0

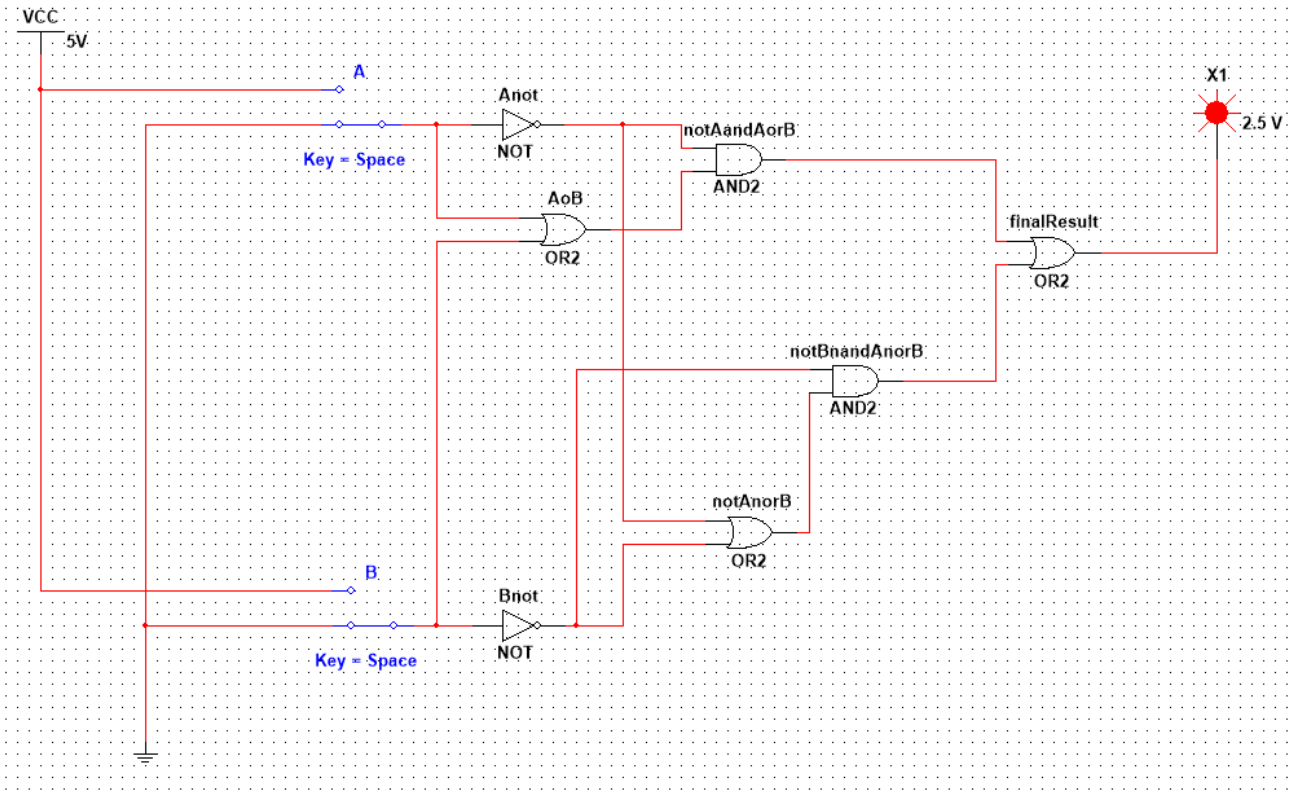
(A' + B + C) (A + B' + C) (A + B + C') :



A	B	C	A'	B'	C'
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

A'+B	A'+B+C	A+B'	A+B'+C	A+B	A+B+C'	(A'+B+C) + (A+B'+C) + (A+B+C')
1	1	1	1	0	1	1
1	1	1	1	0	0	0
1	1	0	0	1	1	0
1	1	0	1	1	1	1
0	0	1	1	1	1	0
0	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1

A’ (A + B) + B’ (A’ + B’):



A	B	A’	B’
0	0	1	1
0	0	1	1
0	1	1	0
0	1	1	0
1	0	0	1
1	0	0	1
1	1	0	0
1	1	0	0

A+B	A'(A+B)	A'+B'	B'(A'+B')	A’ (A + B) + B’ (A’ + B’)
0	0	1	1	1
0	0	1	1	1
1	1	1	0	1
1	1	1	0	1
1	0	1	1	1
1	0	1	1	1
1	0	0	0	0
1	0	0	0	0