# Bahria University,

## Karachi Campus


## LAB EXPERIMENT NO.

## 13

## LIST OF TASKS

| TASK NO | OBJECTIVE |
|---|---|
| 01 | What is the difference between:<br>a. Flip-Flop and Latch<br>b. Synchronous and Asynchronous inputs |
| 02 | What are the applications of different Flip-Flops? |
| 03 | What is the difference between edge triggering and level triggering? |
| 04 | Show the Multisim simulation of SR, JK, D, and T Flip-Flops. |
| 05 | Implement a 4-bit Synchronous Up Counter using J-K Flip-Flops in Multisim. |
| 06 | Implement a Ring Counter and a Johnson (Twisted Ring) Counter using D Flip-Flops in Multisim. |

**Submitted On:**

**Date: 17/12/2025**

# Task No. 01:

"What is the difference between:

a) Flip-Flop and Latch

b) Synchronous and Asynchronous inputs"

# Solution:

| | Flip-Flop | Latch |
|---|---|---|
| ***Trigger Type*** | Edge-triggered | Level-triggered |
| ***Input Influence*** | Output only changes at the very moment of the clock edge. | Output can change anytime the control signal is active |
| ***Complexity*** | More complex | Simpler circuits |
| ***Operation*** | Used in synchronous circuits | Used in asynchronous circuits |

| | Synchronous Inputs (D,J,K) | Asynchronous Inputs (PRE,CLR) |
|---|---|---|
| ***Timing Control*** | Controlled by the Clock. Only affect the output at the clock edge. | Independent of the Clock**.** Affect the output *immediately*. |
| ***Purpose*** | To load or store data during normal, timed operation. | To override the clock and force the device to a specific state. |
| ***Priority*** | Low priority (must wait for the clock). | High Priority (override all other signals). |

# Task No. 02:

"What are the applications of different Flip-Flops?"

# Solution:

Flip-flops are the most fundamental building blocks of digital systems, as they are capable of storing a single bit of information (a 0 or a 1). Because they are edge-triggered, they ensure that all parts of a complex circuit change their state together, in sync with a main clock signal. The specific application for a flip-flop depends on how its inputs (D, J, K, T) are wired, which determines how it reacts to the clock pulse.

- ## D (Data or Delay) Flip-Flop

  - **Function:** This is the most common type used today. It simply stores the value present on its input D when the clock edge hits. It effectively delays the input signal by one clock cycle.
  - **Applications:**
    - **Registers:** Groups of D flip-flops are used as Registers to temporarily hold data (like an instruction or a number) inside a processor or memory system.
    - **Shift Registers:** They form circuits that move data bits around one position at a time.
    - **Sampling:** They "sample" the data input at a precise time determined by the clock.

- ## JK Flip-Flop

  - **Function:** This is considered the universal flip-flop because it can be configured to behave like any other type (SR or T). It has a special Toggle mode: if both inputs (J and K) are high, the output state flips with every clock pulse.
  - **Applications:**
    - **Counters:** They are perfectly suited for building various types of Counters (circuits that count clock pulses), as the toggle feature is ideal for changing states in sequence.
    - **Frequency Division:** They are used to halve the frequency of a clock signal by using them in the toggle mode.

- ## T (Toggle) Flip-Flop

  - **Function:** This is the simplest to understand in terms of counting. When its input (T) is held high (logic 1), its output flips (toggles) from 0 to 1, or 1 to 0, with every clock pulse.
  - **Applications:**
    - **Simple Counters:** They are widely used for building simple ripple counters and other counting circuits.
    - **Frequency Division:** As the output only changes every two clock pulses, it is the most direct way to implement a divide-by-two frequency divider circuit.

# Task No. 03:

**"What is the difference between edge triggering and level triggering?"**

# Solution:

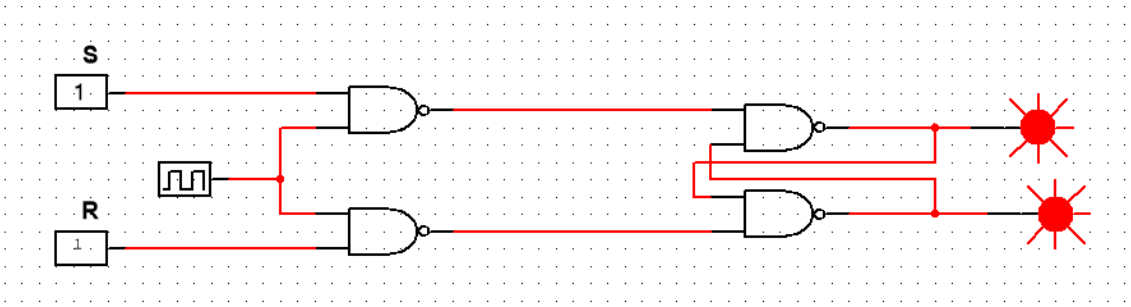
| | Edge Triggering | Level Triggering |
|---|---|---|
| ***Activation*** | The circuit becomes active only at a single point in time i.e. when the clock signal moves from Low to High | The circuit is active for the entire time the clock signal is at a specific level |
| ***Output Change*** | The output only changes state at that instantaneous edge. The output is held constant otherwise. | The output can change continuously as long as the clock signal is at the active level. It's "transparent" during this time. |
| ***Timing*** | Gives precise timing control. Every action is perfectly synchronized to the clock pulse's edge. | Can lead to less precise timing. If the input changes while the clock is active, the output changes immediately. |
| ***Symbol*** | A small triangle on the clock pin | No special symbol; often just a line for the enable/clock pin. |

# Task No. 04:

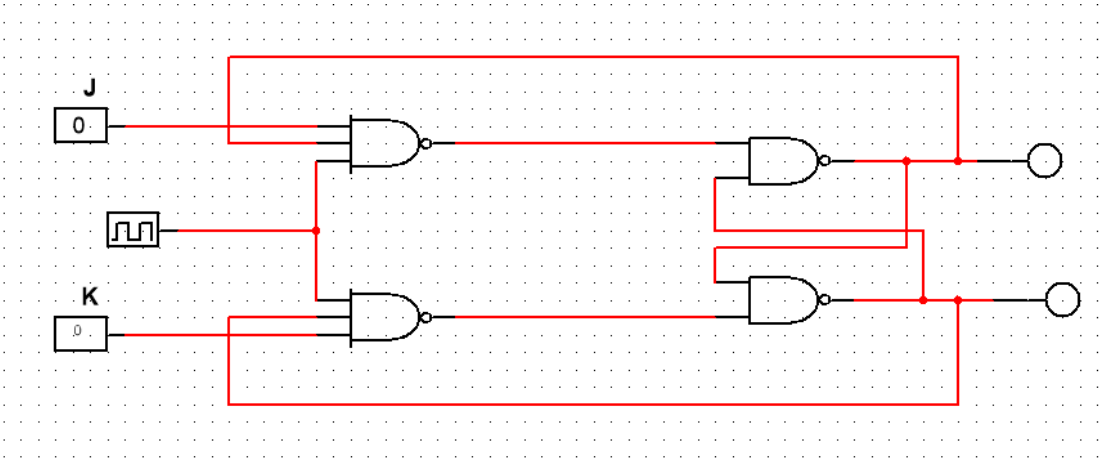
**"Show the Multisim simulation of SR, JK, D, and T Flip-Flops."**

# Solution:

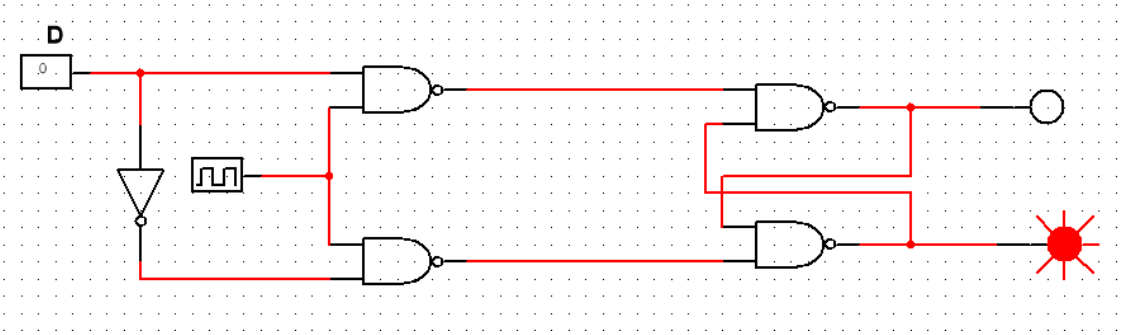
**SR flip-flop:**



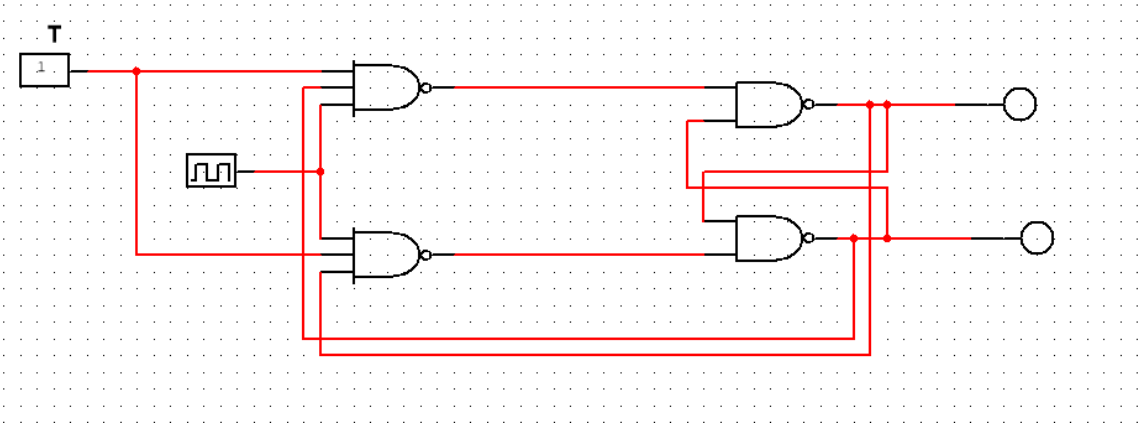
## JK flip-flop:




## D flip-flop:



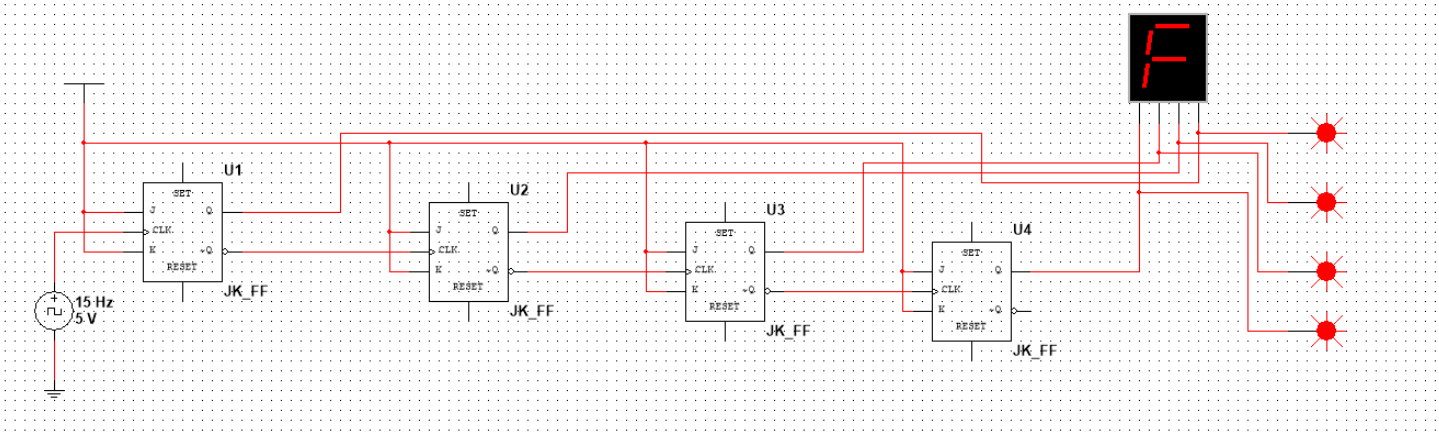

## T flip-flop:



# Task No. 05:

**"Implement a 4-bit Synchronous Up Counter using J-K Flip-Flops in Multisim"**

# Solution:

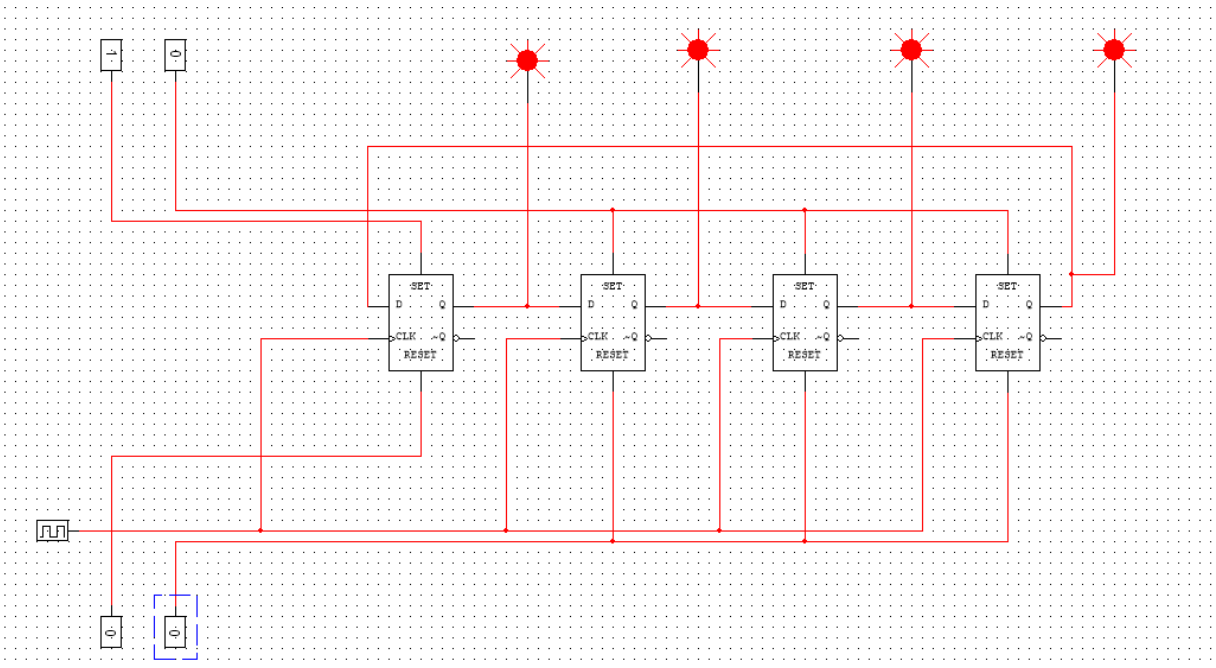



# Task No. 06:

**"Implement a Ring Counter and a Johnson (Twisted Ring) Counter using D Flip-Flops in Multisim."**

# Solution:

### Ring counter:



## Johnson counter: