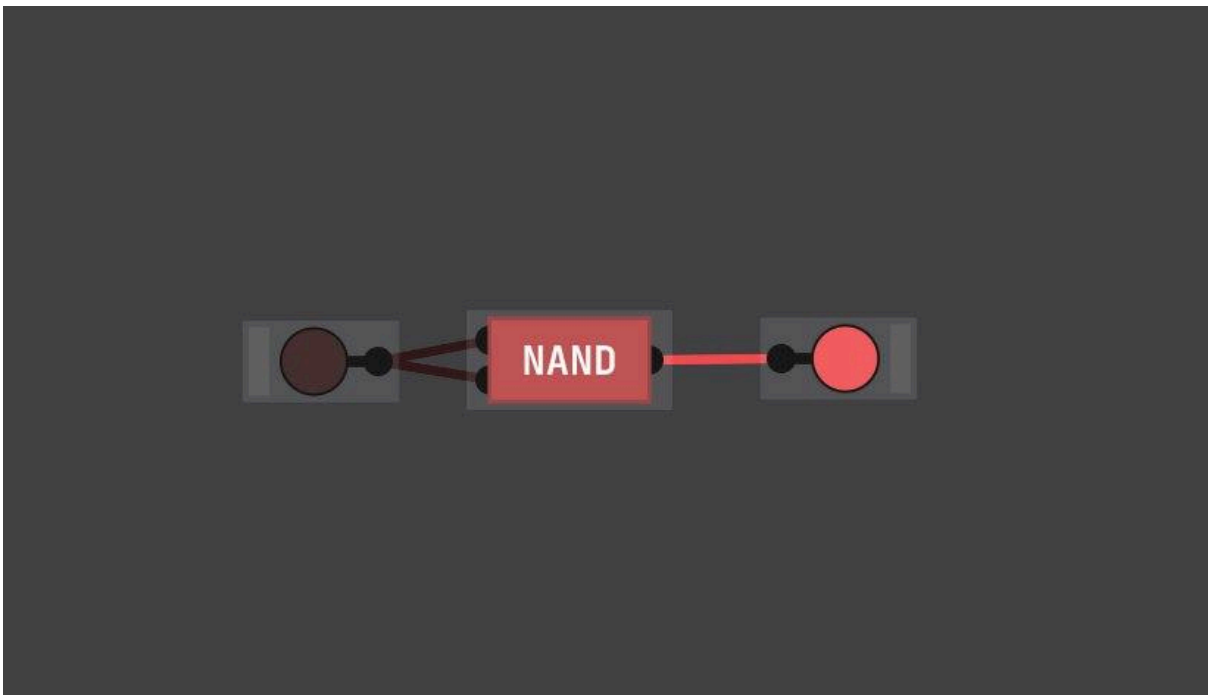
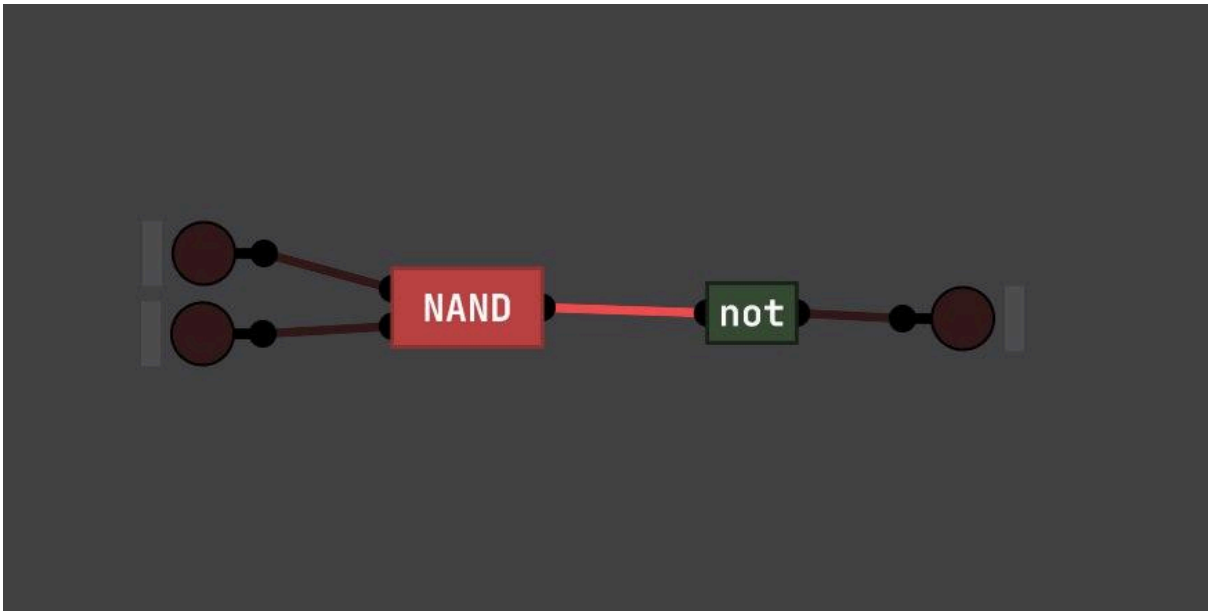
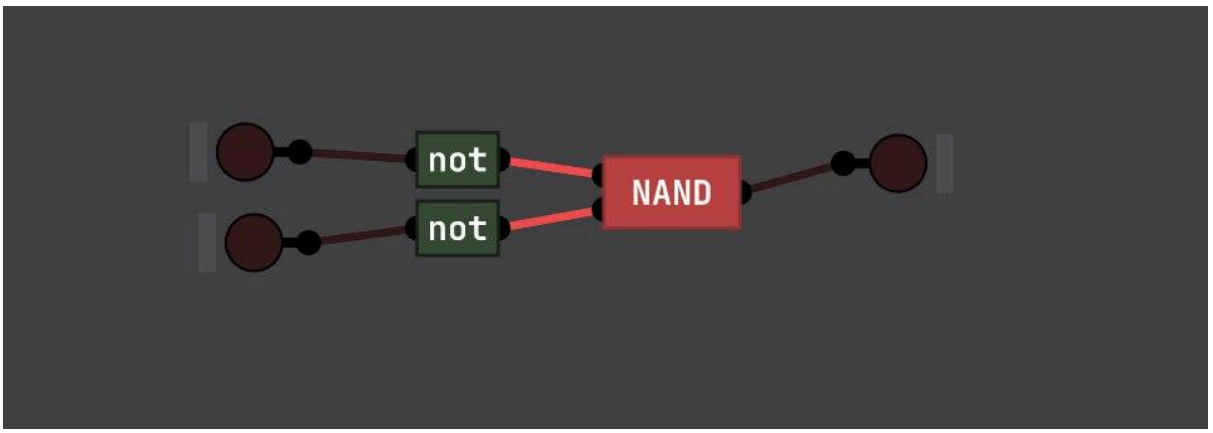


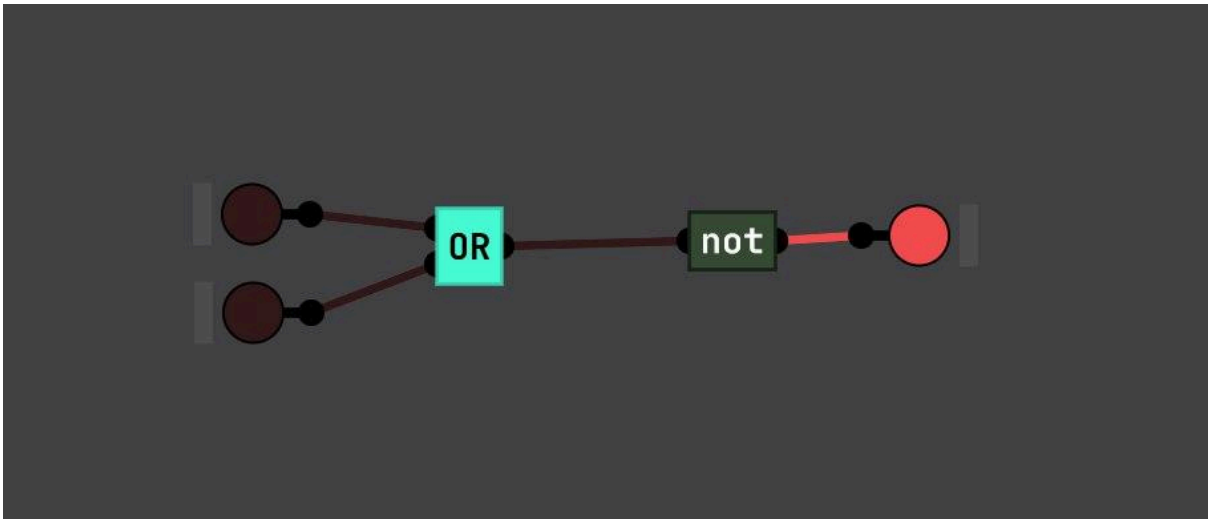
NOT gate



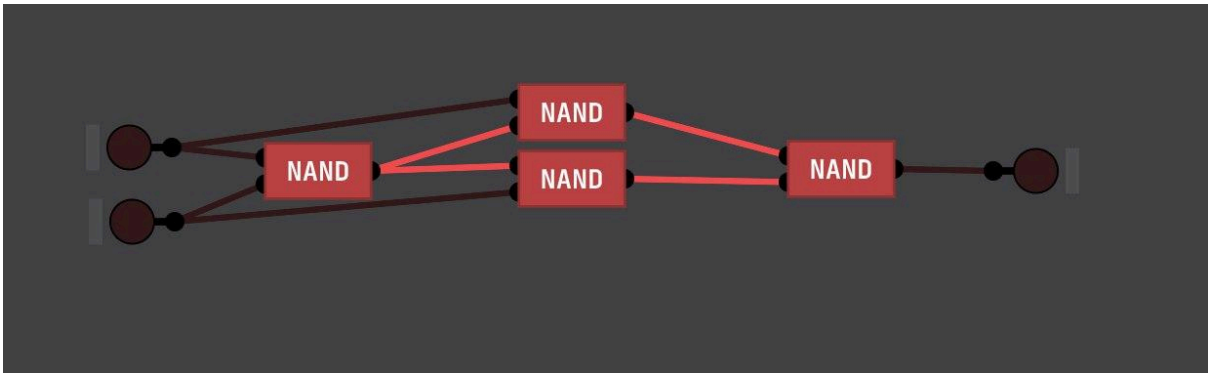
AND gate



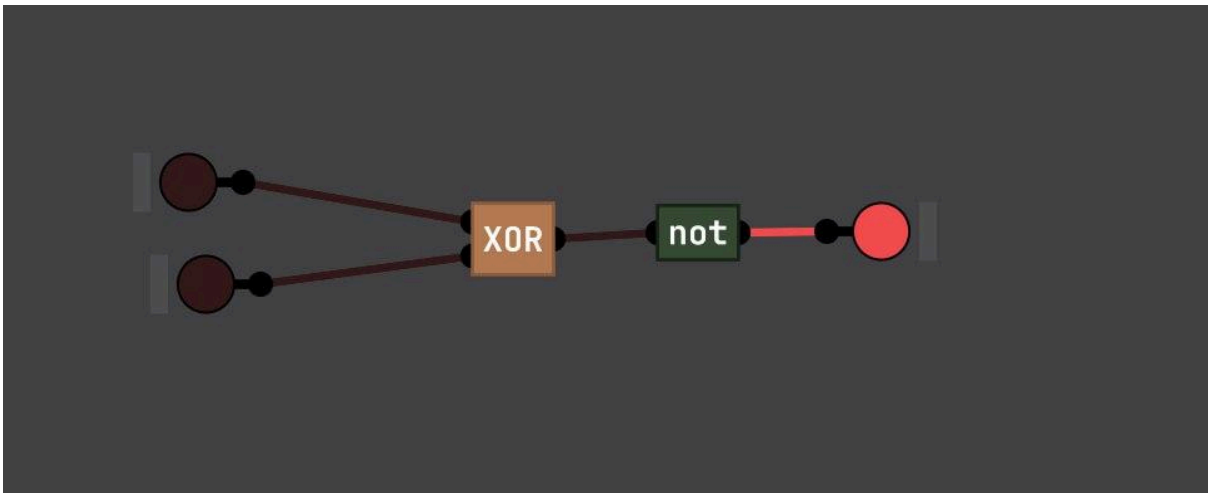
OR gate



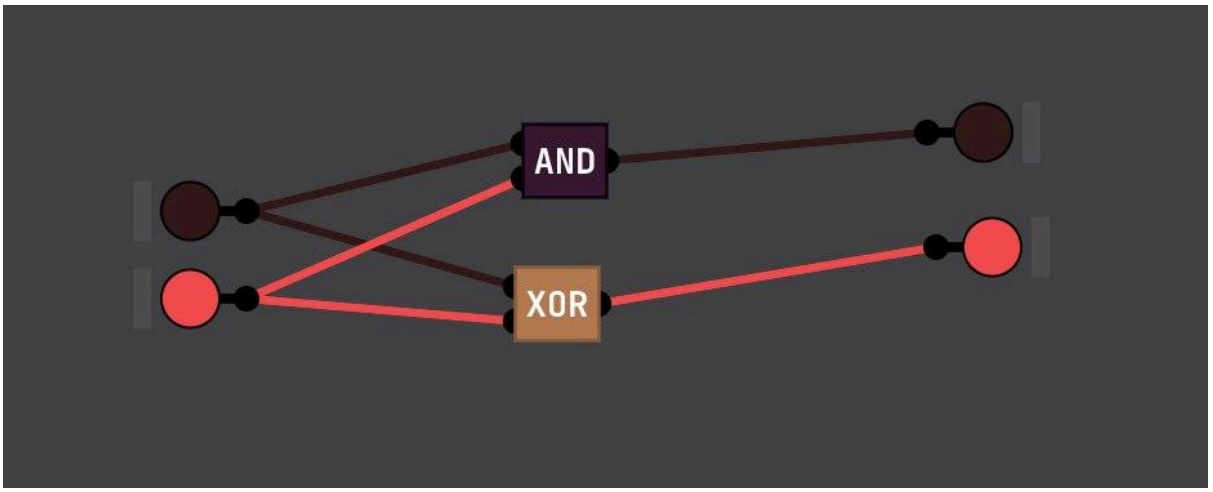
NOR gate



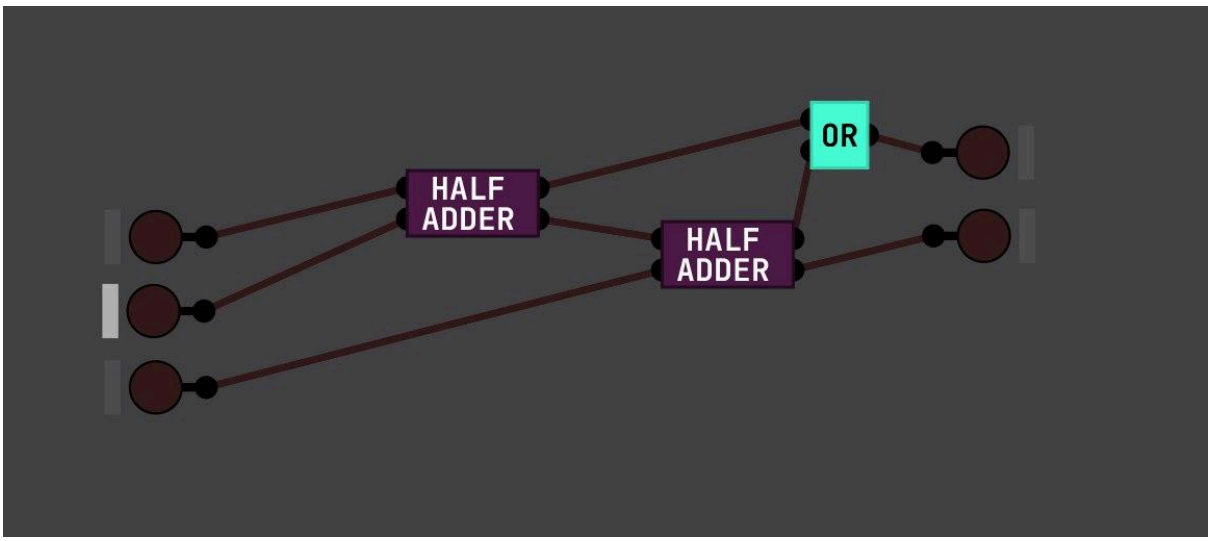
XOR gate



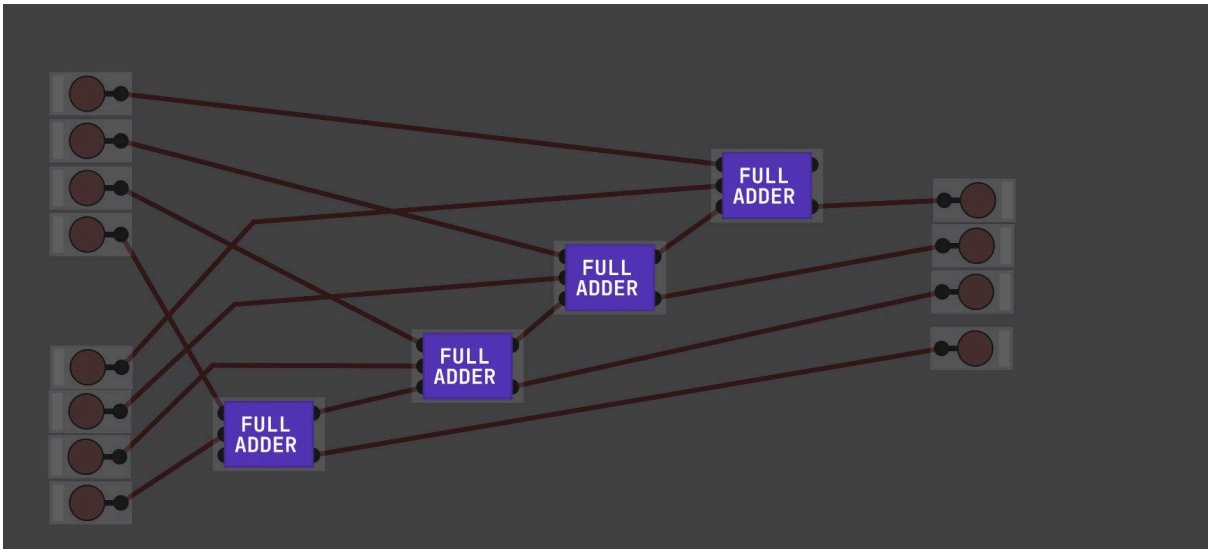
XNOR gate



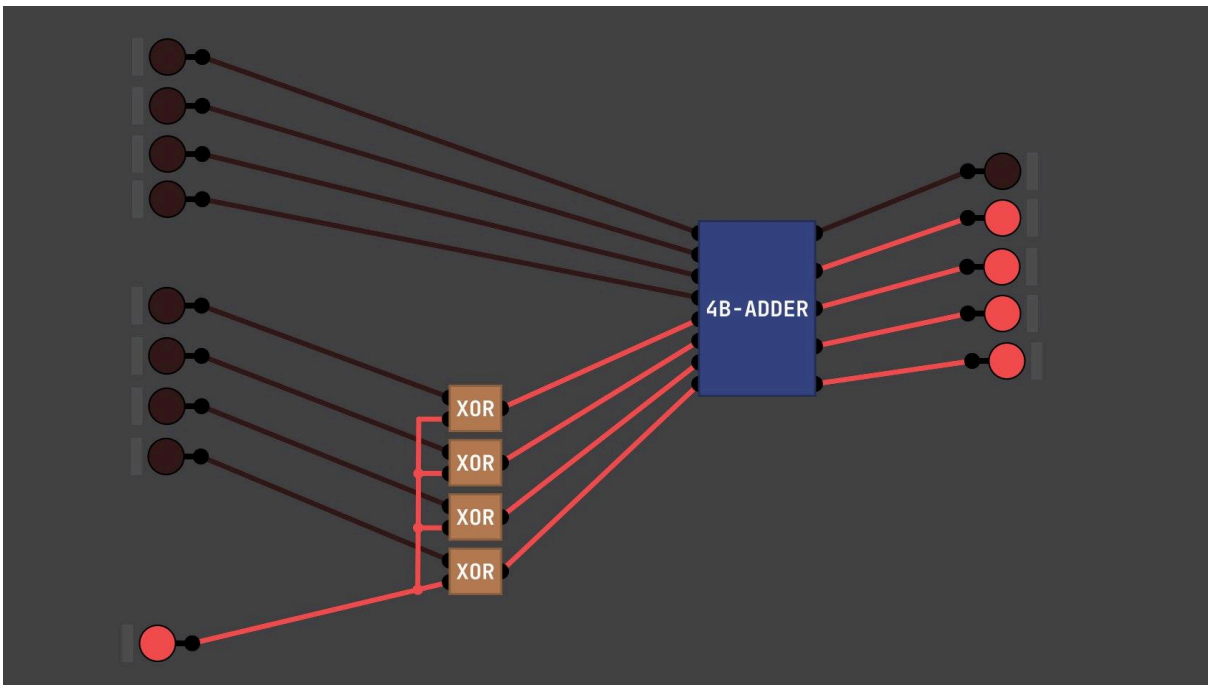
HALf adder



FULL adder



4 BIT Adder



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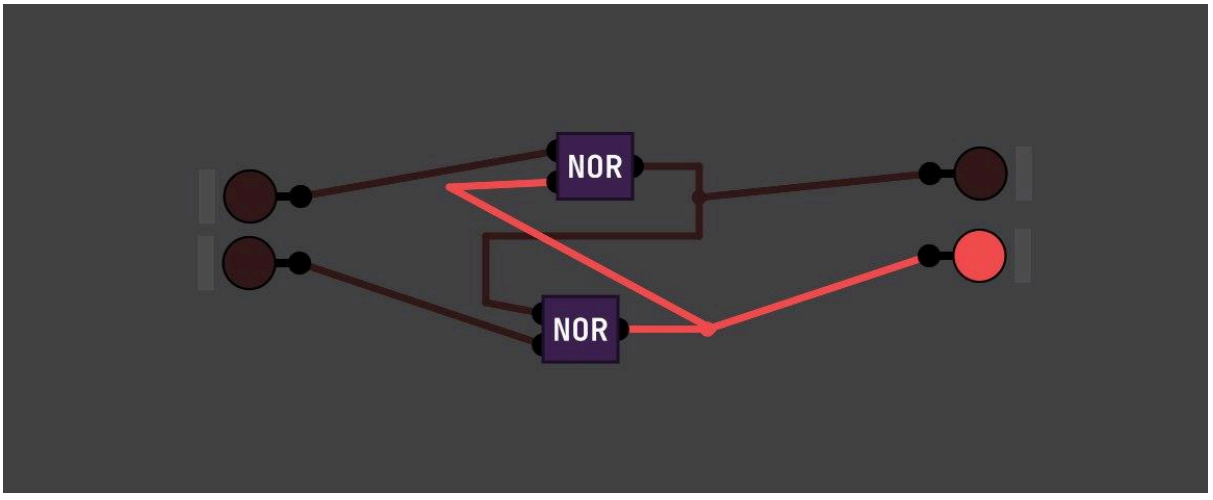
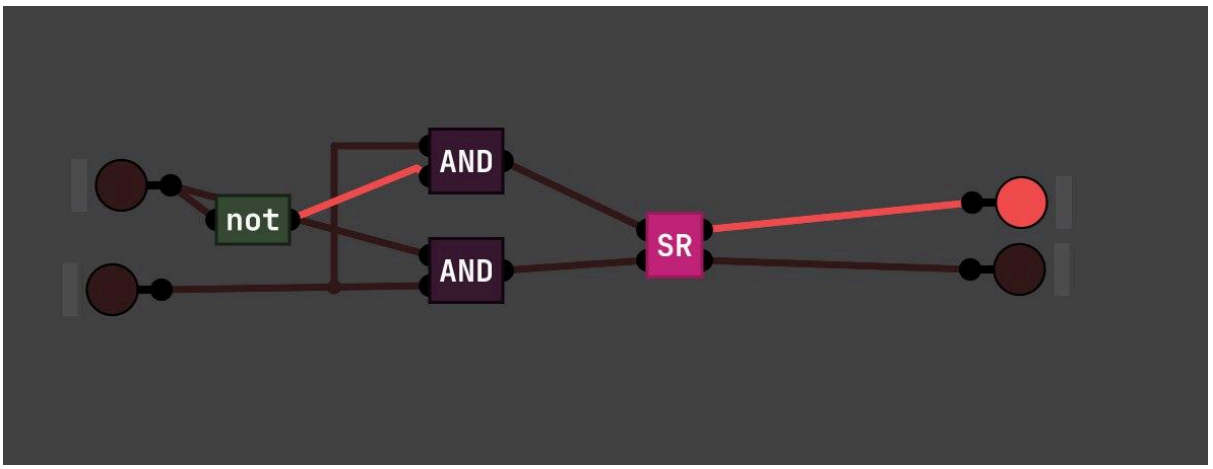
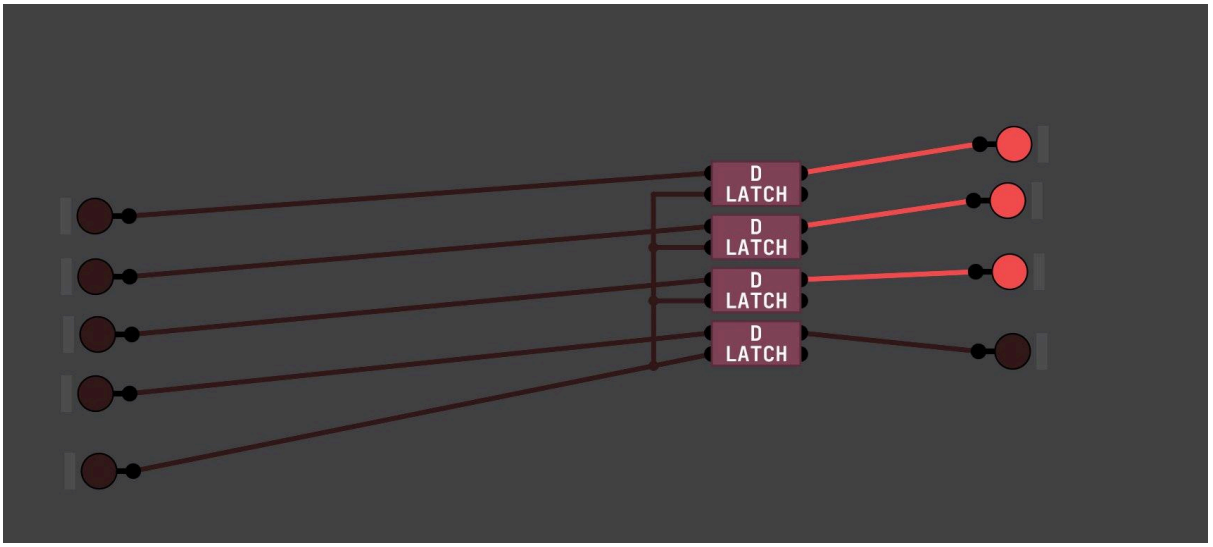


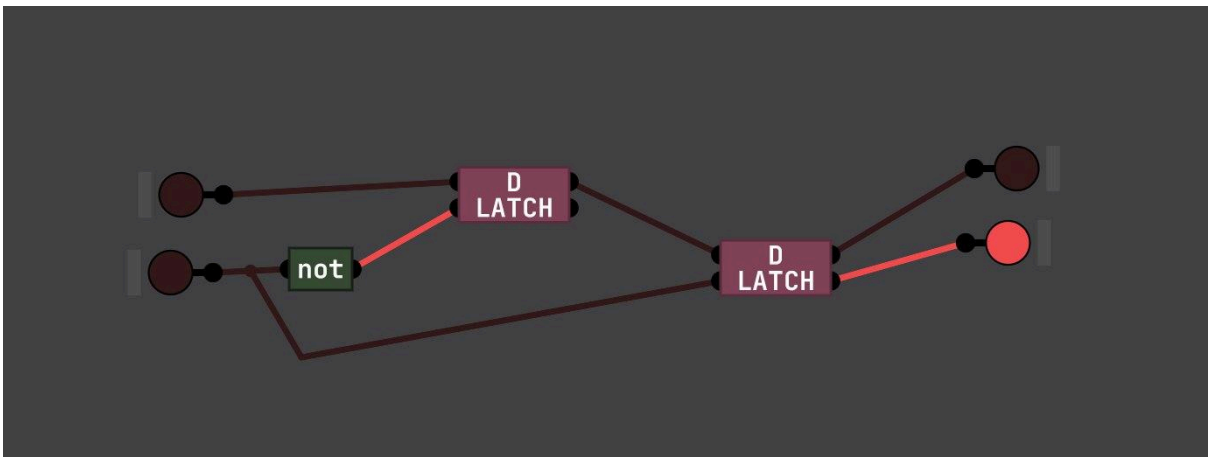
SR



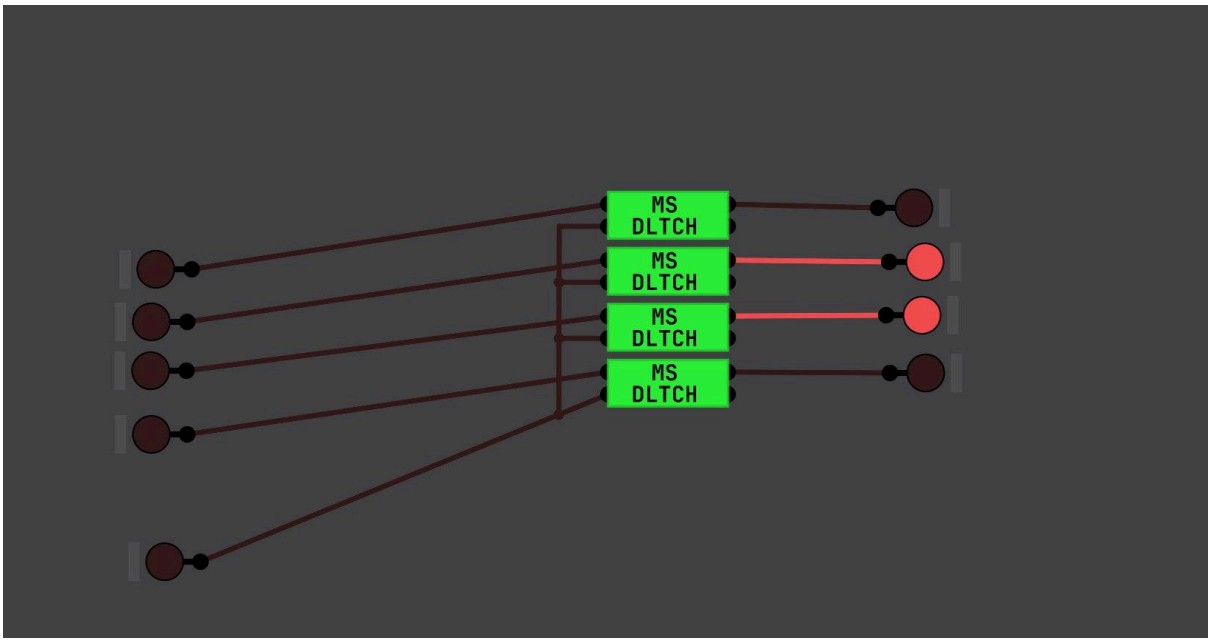
DLATCH



D LATCH REGISTER



MS D LATCH



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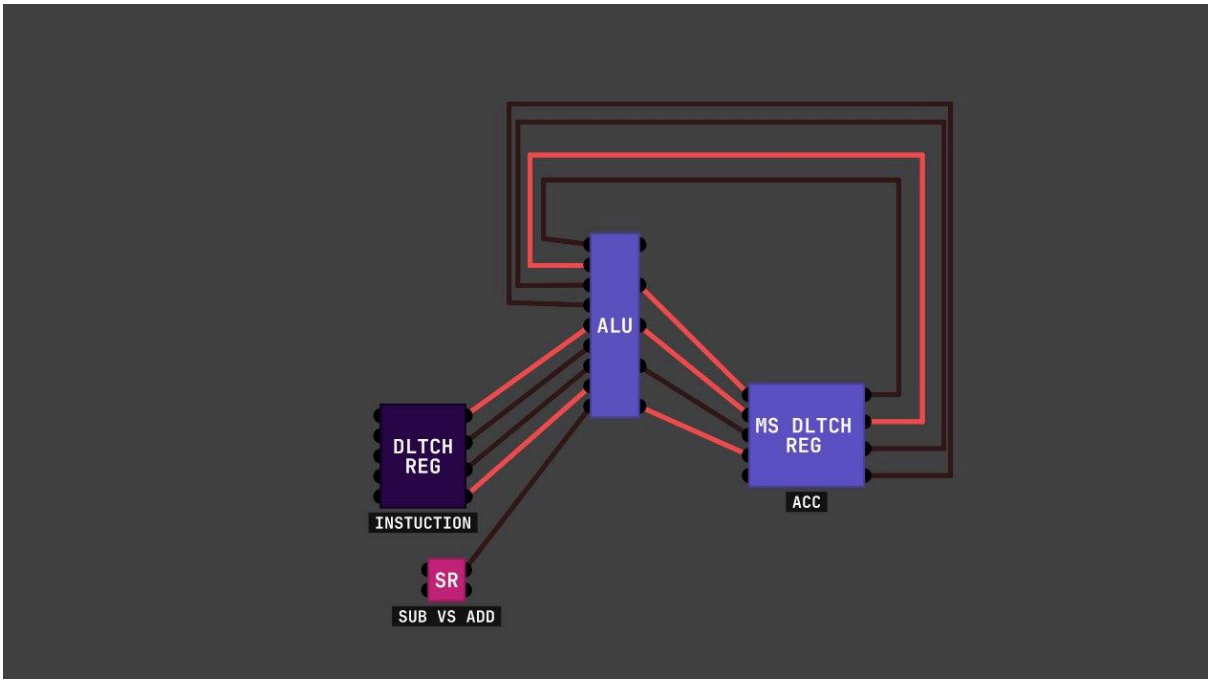
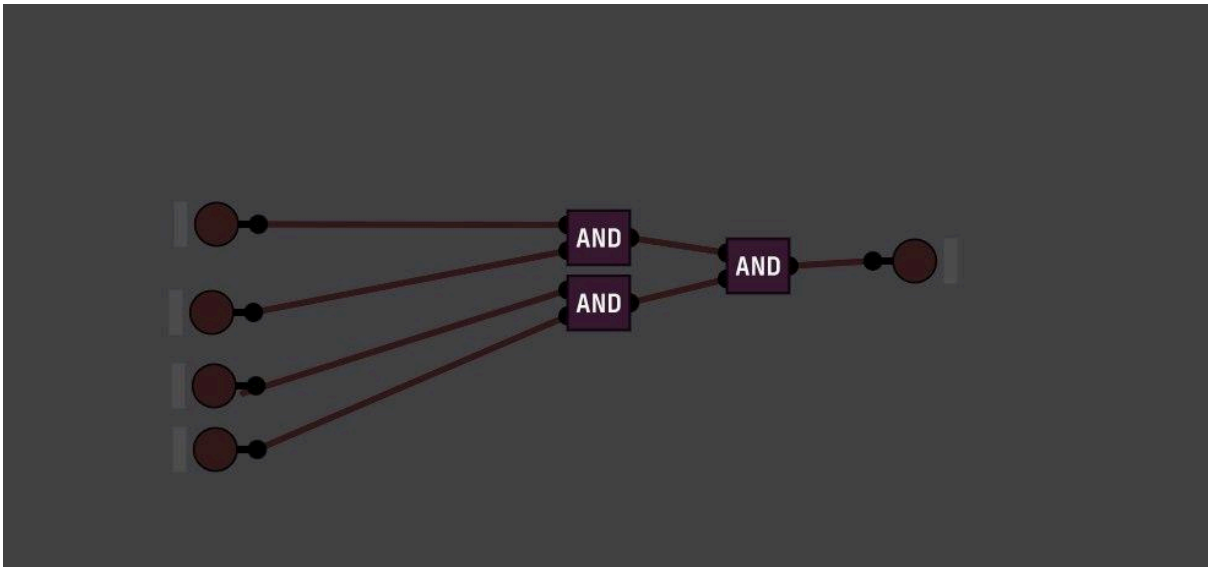
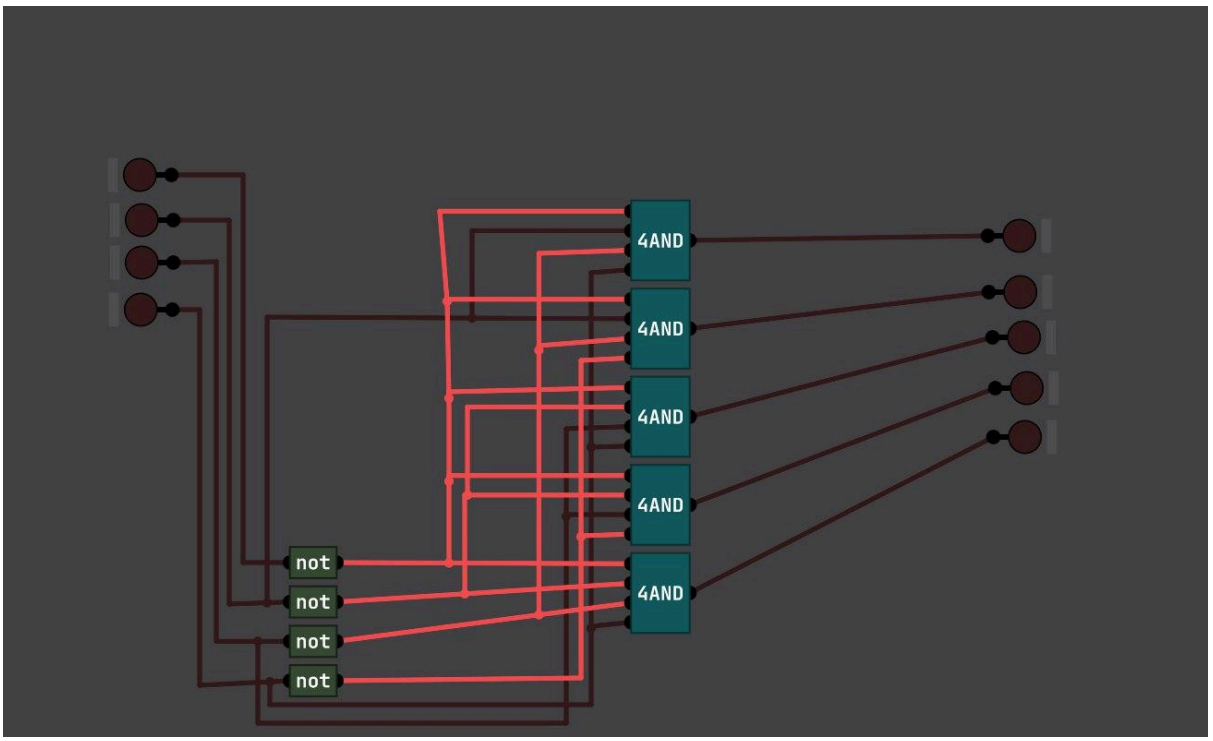

ALU
DLTCH
REG
INSTUCTION
MS DLTCH
REG
ACC
SR
SUB VS ADD

CPU


AND
AND
AND

4AND



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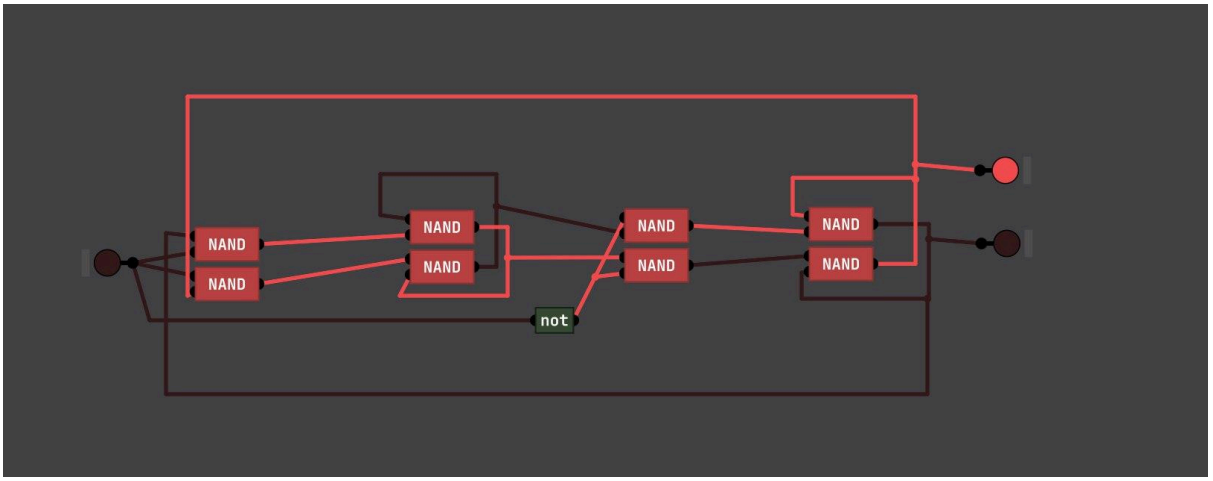

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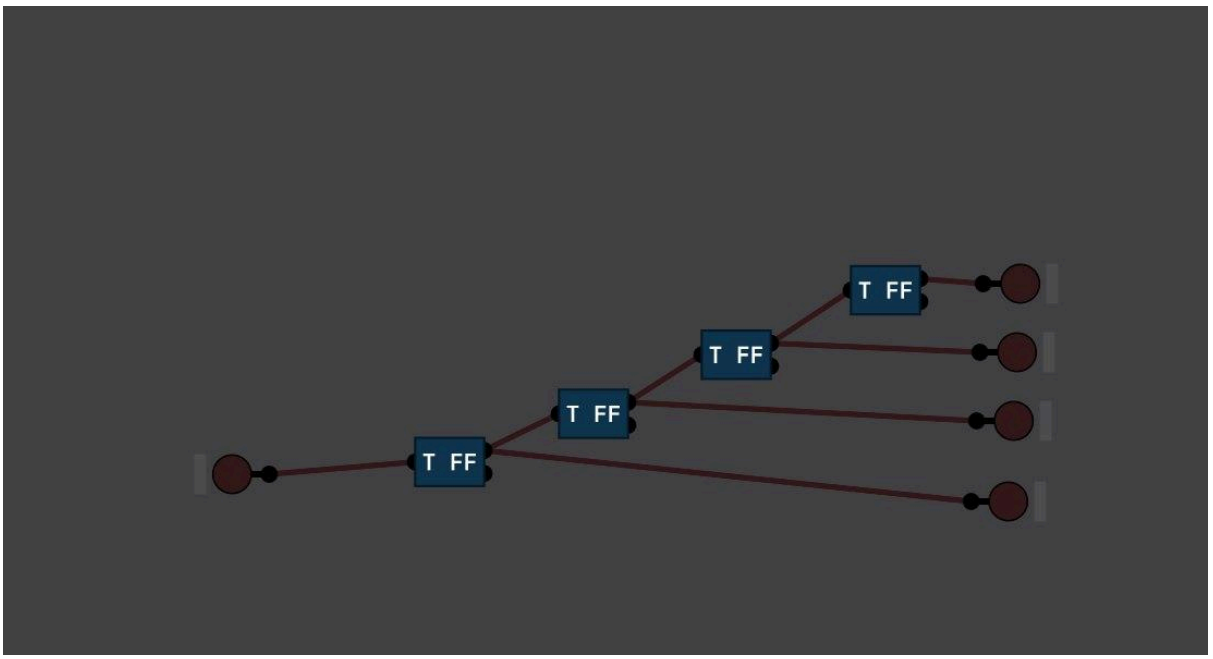
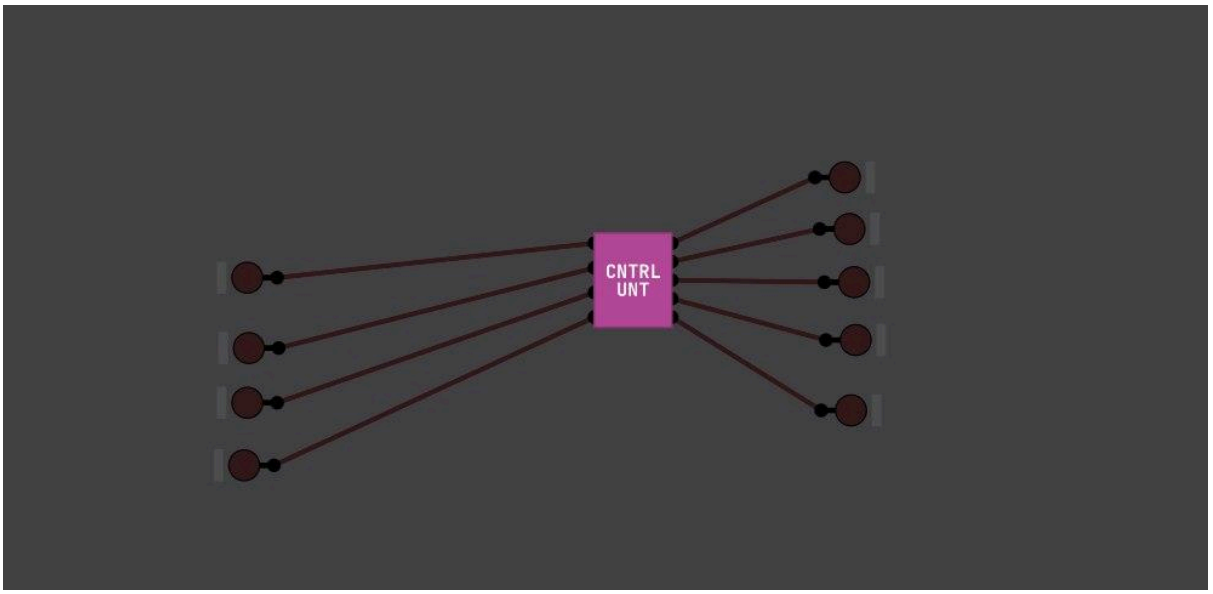
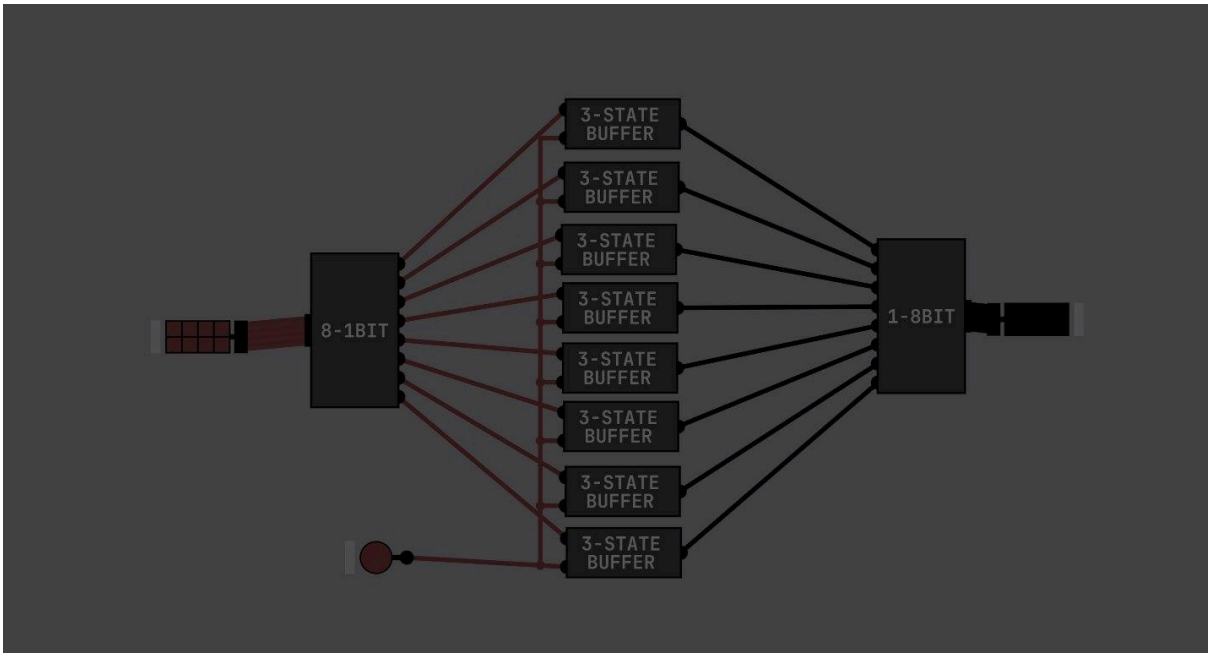


PRG CNTR



4-5 DECODER



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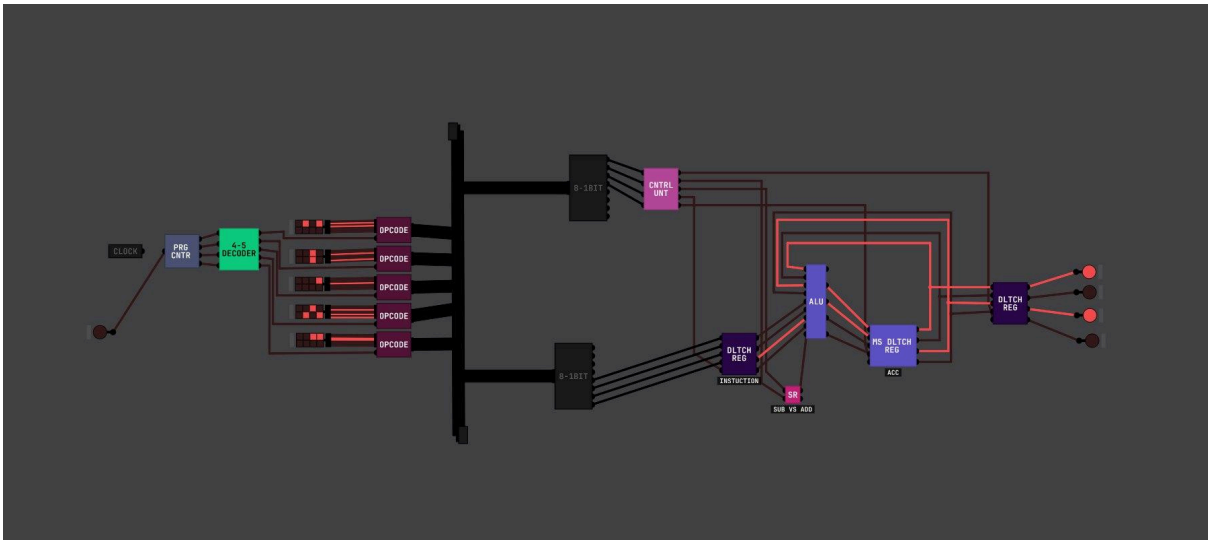

FINISH 8 BIT CPU