National University of Computer and Emerging Sciences

Laboratory Manuals

for

Digital Logic Design

Lab Instructor(s)	
Section	

Department of Computer Science
FAST-NU, Karachi, Pakistan

Lab Session 12 Lacthes and Flop - Flops

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After completing this lab, you would be able to know

PART A

Design SR Latch, D Latch and verify their functional characteristics

Explain the difference between Sequential and Combinational logic
Define 'Set', 'Reset', 'Preset' and 'Clear' concepts.

PART B

Design D Flip-Flop, JK Flip Flop and verify their functional characteristics
Define 'Set', 'Reset', 'Preset' and 'Clear' concepts in Flip-Flops

PART A

Components Required

Breadboard & DC power supply on ETS-7000 Trainer, IC 74LS02, IC 74LS04, IC 74LS08, IC 74LS74, Logic Probe & Jumper wires.

Theory

Combinational Logic Circuit

a) In combinational logic circuit the output of the logic circuit depends only on the present input combinations

b) No matter the inputs are changed in any order, the outputs will remain the same for a particular input combination.

Sequential Logic Circuit

c) In sequential logic the output depends not only on the present input combinations but also on the past state of the output.

d) The output depends on the sequence in which the inputs are changed.

e) This implies that a sequential logic circuit has some kind of memory.

Latch & Flip-Flop

In digital circuits, a ***flip-flop*** is a term referring to an electronic circuit (a bistable multivibrator) that has two stable states 0 and 1. A flip-flop is a memory device and thus will store a value while power remains in the circuit. Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops. Latches are said to be level sensitive devices; flip-flops are edge-sensitive devices. Both are the simplest examples if ***sequential systems***.

1. SR Latch Using NOR Gate

A bistable multivibrator has two stable states, as indicated by the prefix **'bi'** in its name. Typically, one state is referred to as ***set*** and the other as ***reset.*** The simplest bistable device, therefore, is known as a ***set-rest***, or ***S-R Latch***.

To create an SR Latch, we can wire two NOR Gates in such a way that the output of one feedbacks to the input of the another, and vice versa. Consider the figures below for SR Latch circuit diagram as well as Pin Configuration of IC 74LS02.

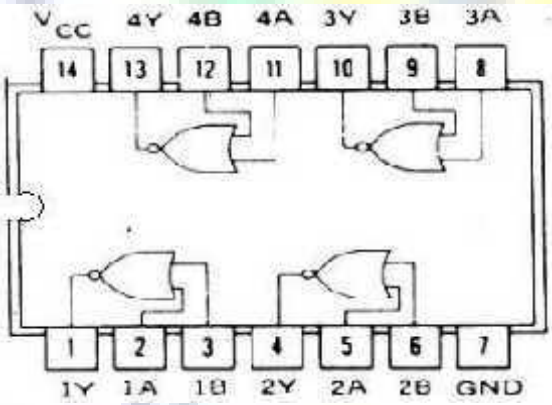


Figure. IC 74LS02 Pin Configuration

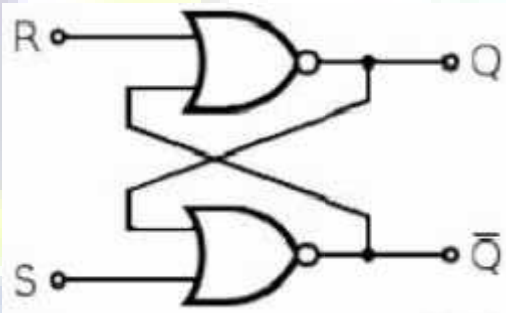


Figure. SR Latch Logic Diagram

Function Table of SR Latch

Inputs		Outputs		Comments
S	R	Q	Q'	

2. D Latch

This latch is known as data latch. It has a data input (D) and enable input (E). It will not respond to a signal input if the enable input is 0. When the enable input is 1, however, Q output follows the D input. This latch has no ***"invalid"*** or ***"illegal"*** state. Q and Q' are always opposite of one another.

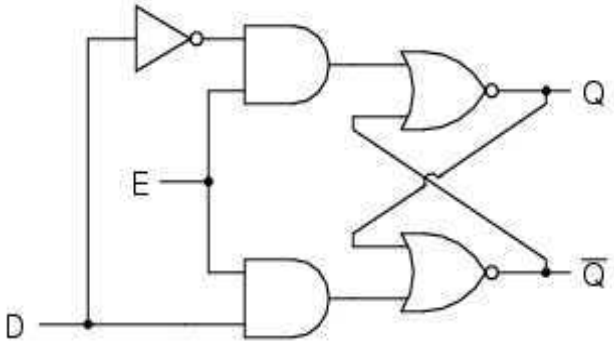


Figure. D Latch Logic Diagram

Figure. Graphic symbol (a) **RS Latch (**b) **D Latch**

Function Table of D Latch

Inputs		Outputs		Comments
E	**D**	**Q**	**Q'**	

PART B

Components Required

Breadboard & DC power supply on ETS-7000 Trainer, IC 74LS74, Logic Probe & Jumper wires

Flip-Flop

In digital circuits, a ***flip-flop*** is a term referring to an electronic circuit (a bistable multivibrator) that has two stable states 0 and 1. A flip-flop is a memory device and thus will store a value while power remains in the circuit. Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops. Latches are said to be level sensitive devices; flip-flops are edge-sensitive devices. Both are the simplest examples if ***sequential systems***.

Symbol for Flip-Flop

A general type of symbol used for a flip-flop is shown in Figure.1. It has multiple inputs, and two outputs labeled Q & Q' which are the inverse of each other. The Q output is called the ***normal output*** and Q' is the ***inverted output***. If we say that the flip-flop is in the High-state, we mean that Q = 1 & if we say that a flip-flop is in Low-state we mean that Q = 0 of course, the Q' state will always be the inverse of Q.

The high state i.e. Q = 1 & Q' = 0 of a Flip – flop is also known as **SET** state. The low state i.e. Q = 0 & Q' = 1 is then called **RESET** state. The reset state is also called the clear state.

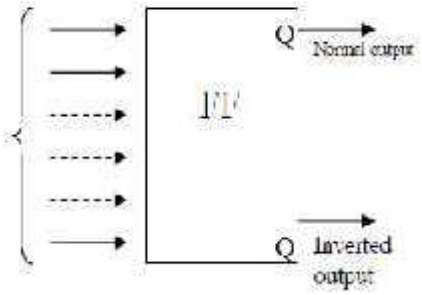


Figure.1 Symbol for Flip-Flop

1. Edge Triggered D Flip-Flop

The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such s the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. We will use IC 74LS74 to observe the operation of D flip-flop. It has Active Low 'Preset' and 'Clear' inputs to directly set and reset flip- flop.

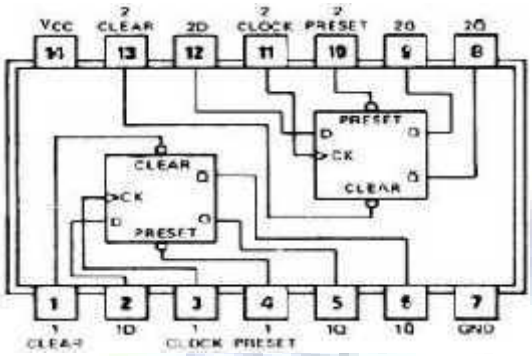


Figure.7 IC 74LS74 Pin Configuration

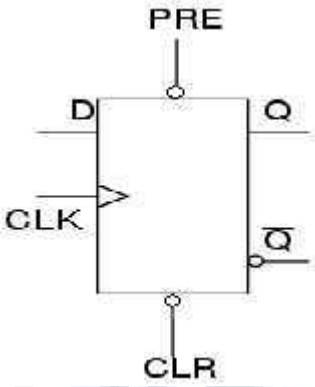


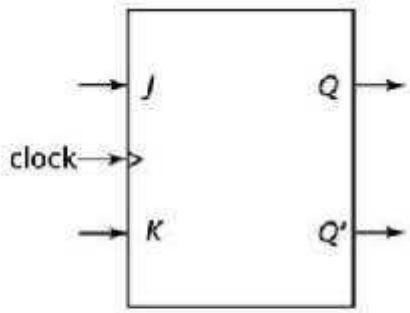
Figure.8 Graphic symbol D flip-flop

Function Table of D Flip-Flop

Inputs				Outputs		Comments
D	**CLK**	**Preset**	**Clear**	**Q**	**Q'**	

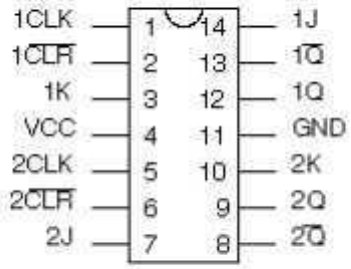
2. JK flip-flop

The JK type flip-flop consists of two data inputs: J and K, and one clock input. There are again two outputs Q and Q' (where Q' is the reverse of Q).



J	K	clock	Q
X	X	not ↑	Q_0
0	0	↑	Q_0
0	1	↑	0
1	0	↑	1
1	1	↑	Q_0'

Dual Jk Flip Flop 74ls73:



INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

Report for Experiment 12

Name **Student ID** **Section B-1-D1-F1-B2-D2-F2**

Exercise # 1. Implement SR Latch by using logic gate on Breadboard and also on Logic Works.

Exercise # 2. Implement D Latch by using logic gate on Breadboard and also on Logic Works.

Exercise # 3. Implement JK Flip Flop on Breadboard and also on Logic Works.

Exercise # 4. Implement D Flip Flop on Breadboard and also on Logic Works.

Quote of the week

A river cuts through rock, not because of its power, but because of its persistence.

Signature

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