National University of Computer & Emerging Sciences, Karachi

School of Computing -Spring 2022

Mid-2 Examination

18th April 2022, 08:30 am – 09:30 am

Course Code: CS2006	**Course Name: Operating System**
Instructor Names: Dr. Ghufran Ahmed, Ms. Anaum Hamid, Ms. Tania Erum, Ms. Mubashra Fayyaz, and Ms. Safia Baloch	
Student Roll No:	**Section No:**

Instructions:

- Return the question paper.
- Read each question completely before answering it. There are **4 questions** and **2 pages.**
- All the answers must be solved according to the sequence given in the question paper.

Time: 60 minutes. **Max Marks: 50**

CPU Scheduling – [Estimated time: 10 mins]

Question no. 01 **[Marks: 4+3+4 = 11]**

a. Consider a system that has a CPU-bound process, which requires a burst time of 25 seconds. The multilevel Feedback Queue scheduling algorithm is used with TQ=2 sec and in each level, it is incremented by 5 sec. Then how many times the process will be interrupted, and in which queue the process will terminate the execution?

The process needs 25 Seconds for total execution.

At Queue 1 it is executed for 2 seconds and then interrupted and shifted to queue 2.

At Queue 2 it is executed for 7 seconds and then interrupted and shifted to queue 3.

At Queue 3 it is executed for 12 seconds and then interrupted and shifted to queue 4.

At Queue 4 it is executed for 4 seconds, and it completes.

Hence the process is interrupted 3 times and completed on queue 4.

b. Explain the processor affinity?

Answer: Processor affinity means that once a process has executed partially on a processor, it is usually worthwhile to keep processing it on the same processor. In other words, it would be more costly to switch it to another processor to continue executing.

c. Discuss in detail about Load balancing in an operating system.

In SMP, need to keep all CPUs loaded for efficiency.**Load balancing** attempts to keep workload evenly distributed.**Push migration** – periodic task checks load on each processor, and if found pushes task from overloaded CPU to other CPUs**. Pull migration** – idle processors pulls waiting task from busy processor

Threads and Concurrency – [Estimated time: 15 mins]

Question no. 02 **[Marks:5+5+4=14]**

a. Determine if the following problems exhibit task/data parallelism or both. Give reasons in one or two lines each:

I. Transpose a matrix in parallel.

II. Calculating the salary of all employees of a company.

III. Taking input from IoT cameras in FAST for single abnormal event detection.

IV. Taking input from IoT cameras in FAST for scene detection (e.g., books, students, blackboard, teacher. detection modules working in parallel for classroom scene detection.

V. National ID card-making procedure at multiple counters of NADRA.

solution:
a) data
b) data
c) data
d) task
e) task

b. **ABC** is a software industry-made app for machine tool design that can be run 35% parallel on an 8 cores machine. The client needs more speed, **ABC** redesigns the app that can run on 16 cores with 40% parallel code. Discuss the speedup difference.

a) S= (1-.35)= .65

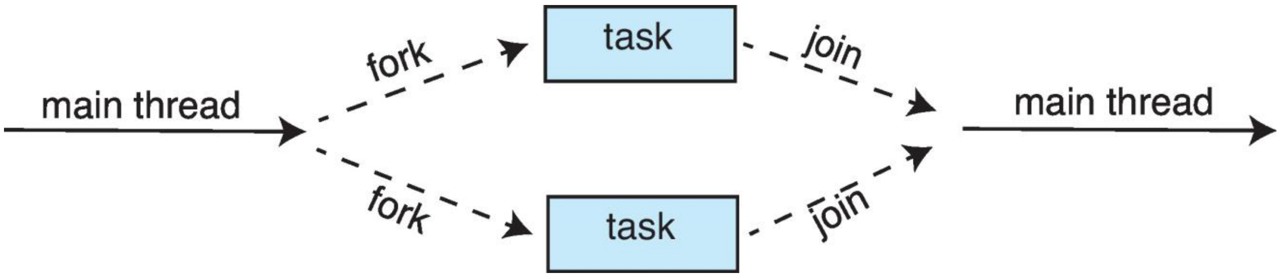
speedup= 1/ s+((1-s)/N) = 1/(.65 + .35/8) = 1.44

b) 1/ .60 + (.40/16) = 1.6

Speedup increased by 0.16 only after integrating double computing unit because speed is dependent as much as upon parallel code comparatively with resources

c. Explain Fork-join operation and illustrate by the diagram?

fork-join is issued by one thread when it wants to stop and wait for the termination of another thread. On termination of the target thread, the original thread resumes execution. Grading Scheme: 1 point for this thread waits for the joined-to thread to finish



Process Synchronization and Tools – [Estimated time: 15 mins]

Question no. 03 **[Marks:6+7=13]**

a. Consider two concurrently running threads: A with operations A1 and A2, and B with operations B1 and B2.

It is required that
- B2 be executed only after A1 has been completed and
- A2 be executed only after B1 has completed

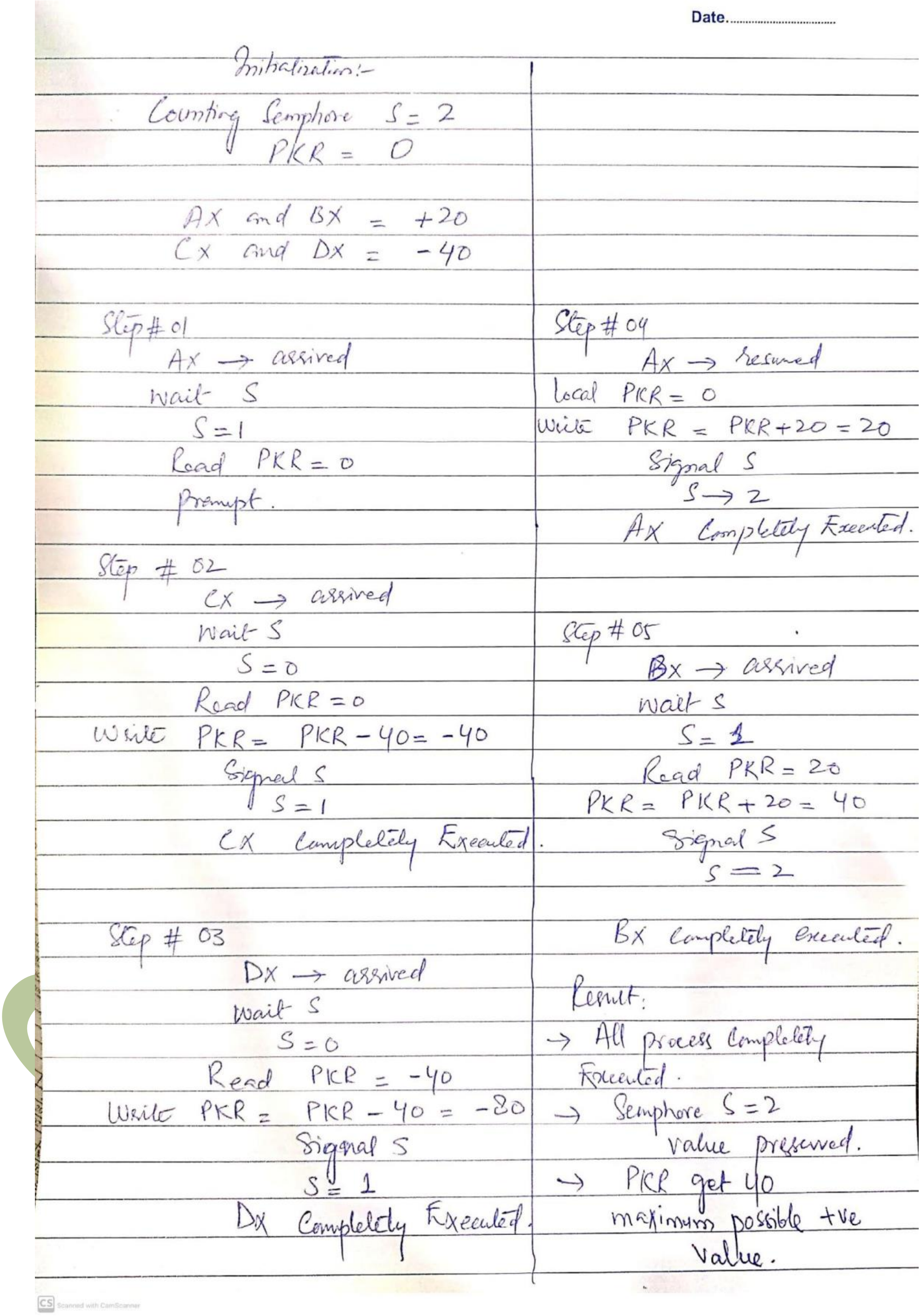
Synchronize threads A and B considering the above requirements.

```
sem A1Done = 0; sem B1Done = 0;

//Thread A
A1
up(A1Done)
down(B1Done)
A2

 //Thread B
B1
up(B1Done)
down(A1Done)
B2
```

b. Four agents (AX, BX CX and DX) from terminals of an investment market create processes concurrently. These concurrent processes make changes in the value of Pakistani rupees by modifying the global shared variable: **PKR**. Processes created by agents AX and BX read **PKR** from memory, increment the value by 20K, store it back in memory, and then terminate. Processes created by agents CX, and DX read **PKR** from memory, decrement the value by 40K, store it back in memory, and then terminate. Synchronize and design the strategy to get the maximum possible value of **PKR** after all processes complete their execution?



Date..............................

Initialization:-

Counting Semphore S = 2
PKR = 0

AX and BX = +20
CX and DX = -40

Step # 01
AX → assived
wait S
S = 1
Read PKR = 0
Prempt.

Step # 02
CX → assived
Wait S
S = 0
Read PKR = 0
Write PKR = PKR - 40 = -40
Signal S
S = 1
CX Completely Executed.

Step # 03
DX → assived
wait S
S = 0
Read PKR = -40
Write PKR = PKR - 40 = -80
Signal S
S = 1
DX Completely Executed.

Step # 04
AX → resumed
Load PKR = 0
Write PKR = PKR + 20 = 20
Signal S
S → 2
AX Completely Executed.

Step # 05
BX → assived
wait S
S = 1
Read PKR = 20
PKR = PKR + 20 = 40
Signal S
S = 2

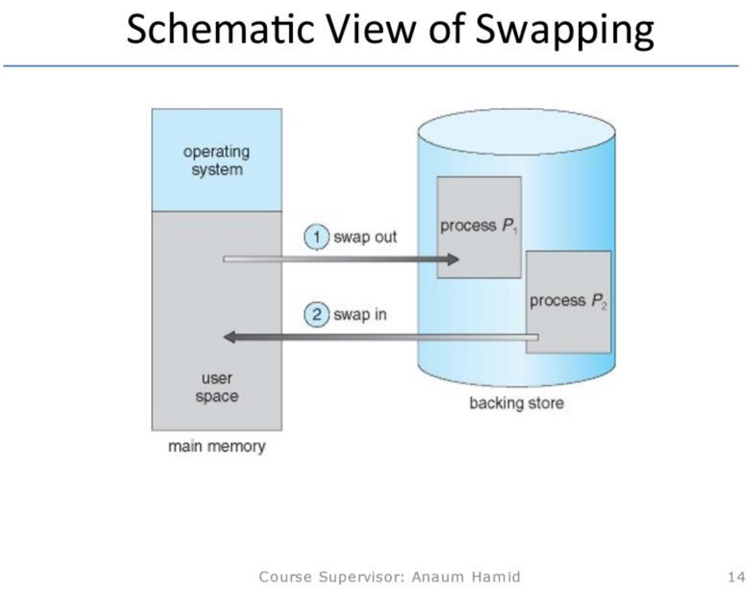
BX Completely executed.

Result:
→ All process Completely Executed.
→ Semphore S = 2 value preserved.
→ PKR get 40 maximum possible +ve value.

Main Memory– [Estimated time: 10 mins]

Question no. 04 **[Marks: 3+4+5 = 12]**

a. Suppose P1 is currently in execution required for bringing P2 into main memory via dynamic linking. Main Memory runs out of the capacity due to the degree of multiprogramming. What can be a solution to this problem? Illustrate your answer through a diagram.



Schematic View of Swapping

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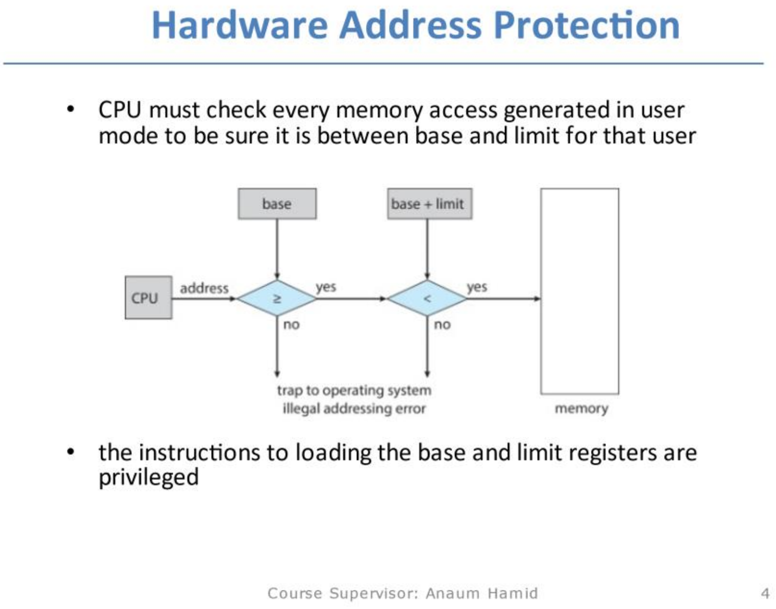
b. Considering the memory protection mechanism, how does an operating system classify an instruction as legal or trap. Describe in detail the security mechanism of a process loaded in memory. Illustrate your answer with a diagram.



Hardware Address Protection

- CPU must check every memory access generated in user mode to be sure it is between base and limit for that user

- the instructions to loading the base and limit registers are privileged

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c. Suppose a user process of 3072 KB is rolled-out from main memory to hard disk with a standard transfer rate of 1Mbps. Calculate how long swapping will take if another user's process of 2048 KB rolls into the main memory.

User process size is 3072KB
Data transfer rate is 1Mbps = 1024 kbps
Roll out Time = process size / transfer rate
= 3072 / 1024
= 3 seconds = 3000 milliseconds

Another user process size is 2048KB
Roll in time = process size / transfer rate
= 2048 / 1024
= 2 seconds = 2000 milliseconds.
Total time = 3000 + 2000 = 5000 milliseconds / 5 sec.