Project Name

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Project Description:
This project aims to prepare a pipelined RISC-V processor for potential fabrication by refining and optimizing its design. Key objectives include replacing non-synthesizable memory loading methods with SRAM (compiled memories) to enhance memory efficiency, reduce area, and lower power consumption.
The current technique used to load memory content is non-synthesizable, and this will be replaced with a debug unit that supports external interfacing.
Additionally, the Debug Unit will enable post-fabrication testing and memory loading, while the Verilog code will be optimized to achieve the highest possible operating frequency.
After these modifications, a comprehensive backend design flow will be conducted, including synthesis, floor planning, power analysis, placement, routing, and timing analysis, to ensure the processor is ready for physical implementation.

Project Requirements:

- Change memory interface to achieve Maximum area & Power efficiency.
- Add External interface to Load desired memory.
- Add debug capabilities to the processor.
- Physical design (layout) of the processor.
- complete backend flow and Simulations of the RISC-V.

Project Specifications:

- SRAM memories (compiled memories).
- Design a debug unit & external memory interference.
- Using synopsis for Design & compiler.

Development Stages / Design Flow	Tools
RISC-V code Implementation	System Verilog
Functional simulation	XMSIM/VCS/ NCSIM
Synthesis	Design Vision - Synopsys
Layout Design	First Encounter - Synopsys

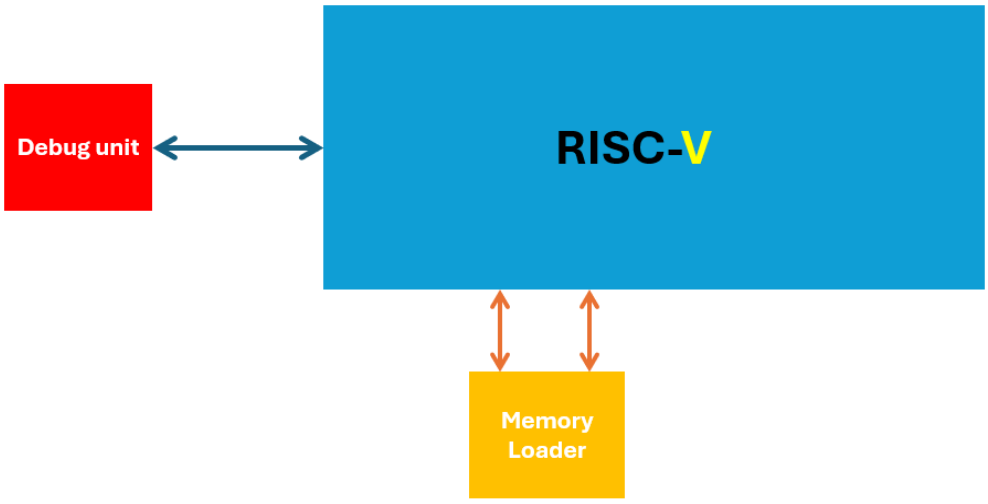
Literature
Provide a summary of the literature used for the project.

A RISC-V pipeline is a processing architecture that improves throughput by dividing instruction execution into multiple stages, enabling different parts of several instructions to be executed simultaneously.
A significant portion of the processor's area is occupied by its memories (data memory and instruction memory). By using compiled memories, we can achieve greater efficiency in terms of area and power consumption.
Additionally, the processor currently employs a non-synthesizable technique to load memory content, which will be replaced with an external interface to facilitate interaction with external systems. This change will also enhance debugging capabilities.
Furthermore, additional debug features will be integrated into the processor to support better testing and analysis.

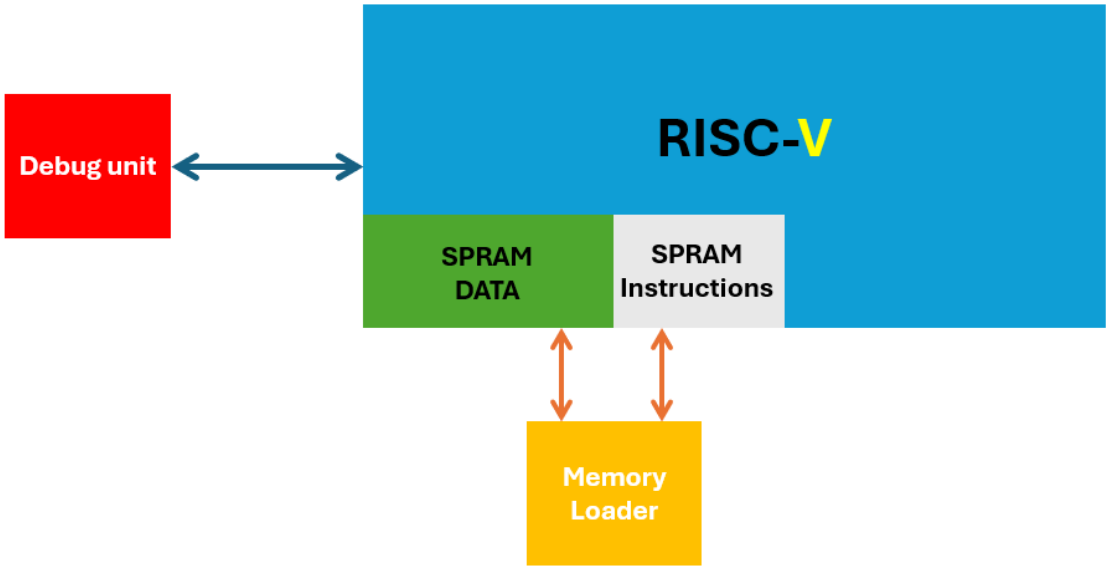
Alternative solutions
Using FPGA memories and the control unit as a debug tool to monitor internal signals, while leveraging the initial lines of code to load the desired memory into the compiled memory.

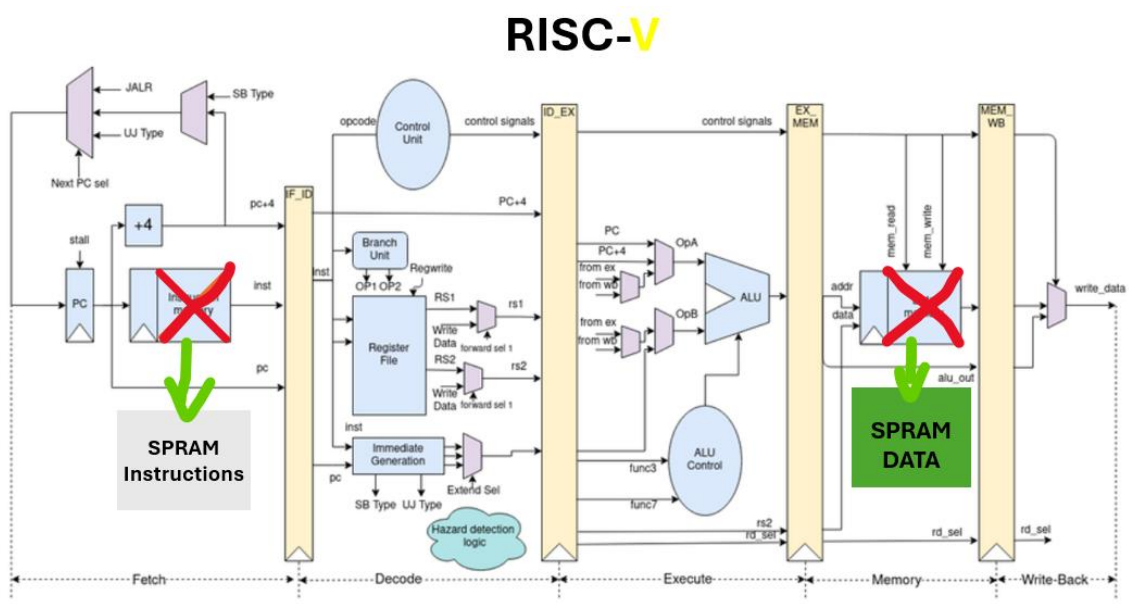
Selected solution
Using SRAM memories, which are area & power efficient, allowing simultaneous read and write operations to multiple addresses. Create a dedicated debugging unit, separate from the control unit, to load the memories before initiating any tests and to provide additional debugging capabilities.

Top Level Interface:



Top Level Architecture:





Memory loader will be connected to internal SRAM memory.

Project Schedule:

Provisional/Preliminary Schedule	**Week**
Architectural and Logic Design Learning & Functional simulation	1-4
RISC-V Module bring up and Debug	4-6
Memory changes (Integrating SRAM) & Synthesis	6-10
Debug Unit Design & test	10 - 12
exams	12-16
Final Layout Design & Report	16-18

Gantt chart: