A logo for a laboratory

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Customization of RISCV Code and Backend Design of a RISCV Processor Project report

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# **Abstract**

Our primary objective in this project is to modify and prepare the pipelined RISC-V processor, as taught in the “Digital Systems & Computer Structure” course, for a VLSI backend flow and potential chip fabrication while improving some of its functionally and adding debug capabilities.

The processor design provided in the course was intended for simulation and educational purposes only and is not synthesizable in its original form. To prepare it for fabrication, we made several structural and functional changes.

These include replacing the non-synthesizable memory initialization method with an external memory interface, switching to area-efficient compiled memories, and later improving the memory loading method and functionally of the module we worked on. and adding debugging capabilities that allow access to internal registers after fabrication.

As part of this effort, we also improved the Verilog implementation to support higher clock frequencies and better performance in the physical design flow.

On the path to achieving our goal, we modified and verified the RTL, followed by a backend flow including synthesis, scan insertion, logical equivalence checking, floor planning, power grid design, placement, clock tree synthesis, routing, and timing analysis.

# **Introduction**

## Project Goals and Requirements

Transit our current pipelined RISC-V module for implementation using Tower's 18nm RAM technology, reaching layout stage, with the following design goals:

* Maximumzing area & power efficiency.
* Optimizing chip memory.
* Create memory loading method.
* Debug capabilities for accessing internal registers post-fabrication.
* Optimizing chip Frequency.

## Alternative Solutions

The RISC-V processor we worked with can utilize FPGA-based memories and using the control unit as a debug tool to monitor internal signals. It also leverages the initial lines of code to load specific content into the memory. While this approach enables functional testing and debugging during development, it presents several limitations.

FPGA memories are not efficient in terms of area and power consumption, and the Verilog code used to integrate them is not optimal.

Additionally, the original design imposes restrictions on accessible memory addresses, which limits flexibility and scalability in more advanced use cases.

## Selected Solution

Using SRAM memories (Designed by Tower), which are both area & power-efficient, allowing simultaneous read and write operations to multiple addresses, and making the chip synthesizable.

A memory loading method will be added, to allow memory initialization and testing post-fabrication.

Additionally, creating a dedicated debugging unit, separate from the control unit, to provide additional debugging capabilities & accessing internal registers after fabrication, one register at a time, while halting the processor.

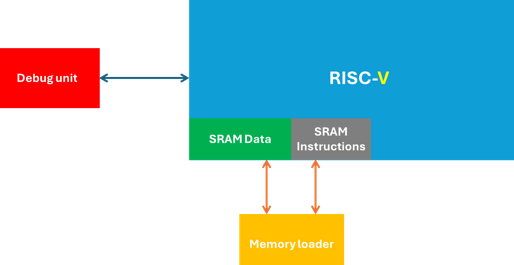


Figure 1: top-level description of the solution

* Add a second photo of the RISC-V with the debug unit wires and mux

# **2. Verilog Implementation’s**

## 2.1 SRAM & memory loading method Integration into RISCV

Both the instruction & data memories in the original RISC-V design had to be replaced.

However, the selected SRAMs do not support direct memory initialization during simulation. This limitation prevented the loading of test programs and data, effectively blocking the ability to verify and test the RISC-V core in a simulated environment.

To overcome this, a custom memory loading mechanism was implemented, Allowing the loading of both instruction and data memories at runtime via an external interface or testbench control, by enabling pre-execution memory initialization.

this solution ensures full support for simulation-based testing, preserving the functional validation and debugging capabilities of the RISC-V processor.

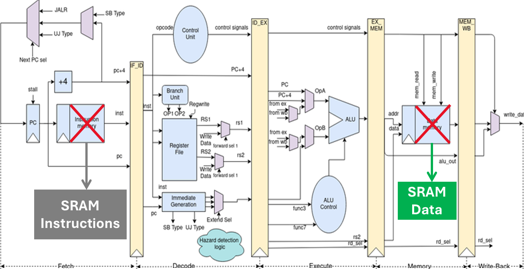


Figure 2: SRAM changes

### 2.1.1 Instruction memory changes

In the used RISC-V, an instruction is a vector of 32 bits.

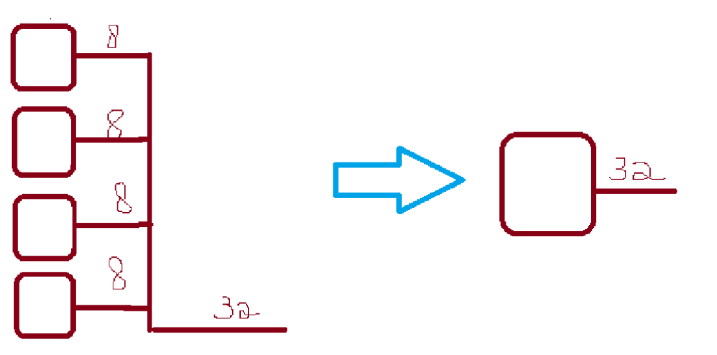
4 Fpga RAMS on chip (65536\*8) were replaced by one tower RAM (2048\*32), thus reducing wires and simplifying logic (less wires & eliminating the need of slicing of current instruction address & joining the sliced instruction parts from all Fpgas) in the processor.

Figure 3: Simplified Diagram of Instruction Memory Modifications

### 2.1.2 Data memory changes

In the implemented RISC-V design, load and store operations for bytes, half-words, and full words are fully supported.

However, it is important to note that correct and expected processor behaviour is guaranteed only when memory addresses used for these operations are word-aligned—that is, the address must be divisible by 4 (address % 4 == 0).

Misaligned accesses may lead to undefined behaviour or require additional hardware handling, which was not implemented in this design.

The four original FPGA memory blocks (each 65,536 × 8) were replaced with four Tower 18nm SRAM blocks (each 4,096 × 8), ensuring continued support for the previously mentioned memory operations.

To obtain full functionality Verilog logic was implemented, this logic extends the processor's capabilities to correctly handle load and store operations for all addressable memory locations—including those that are not word-aligned (i.e., addresses not divisible by 4). As a result, the processor now fully supports byte-, half-word-, and word-level memory access across the entire memory space.

The added logic **Reorders memory block addresses and data** accordingly, dynamically mapping each byte to the correct SRAM address and block, the least significant two bits of the address determine the alignment.

A diagram of a block diagram

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Figure 4: Simplified Diagram of data Memory Modifications

### 2.1.3 Memory Loading Mechanism

As explained previously, Tower SRAMs do not support direct memory initialization during simulation, additionally, in the real world, post-fabrication, it is desirable to be able to load memory onto the chip to run benchmarks and tests.

A memory loading mechanism was implemented, utilizing three 32-bit vectors to specify the data and instructions to be loaded—two vectors for data and one for instructions. Additionally, three vectors were used to designate the addresses where the data and instructions would be loaded, along with two control wires to manage the loading process.

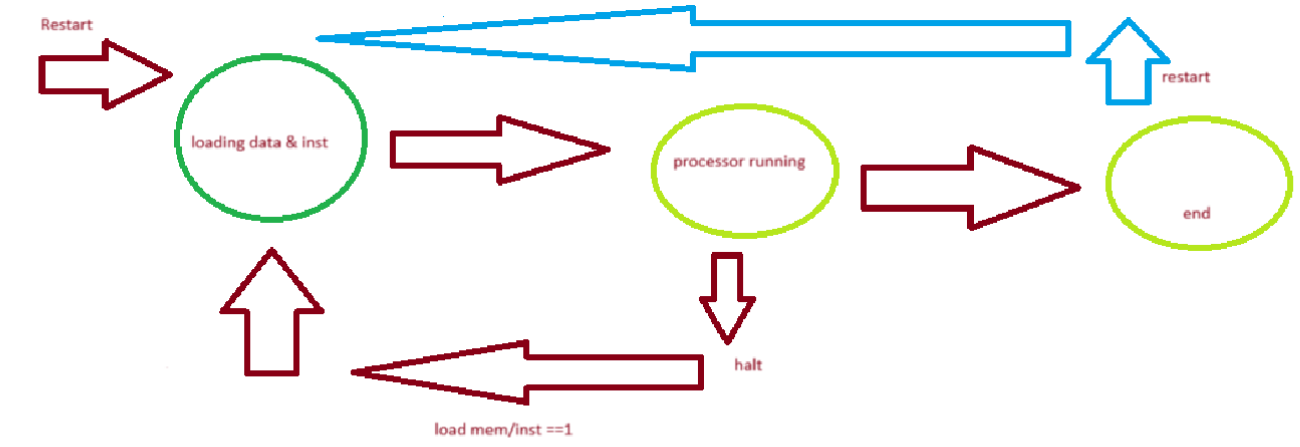
When one of the control wires is set, the processor halts and enters a “loading” state, where it loads the provided data to the specified addresses every cycle.

Figure 5: Simplified Diagram of processor states

## 2.2 Debug unit Integration into RISCV