A 216μW 281MHz-1.126GHz Self-Calibrated SSCG PLL with 0.6V Supply Voltage in 55nm DDC™ CMOS Process

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Abstract

This paper presents a low power, wide frequency range charge-pump phase-locked loop (PLL) with Spread Spectrum Clock Generation (SSCG) feature. The PLL employs a self-calibration scheme to set the coarse frequency range and utilizes a differential MOS varactor for fine tuning of voltage-controlled oscillator (VCO). This approach results in a wide operating frequency range from 281 MHz to 1.126 GHz while running at 0.6V in 55nm Deeply Depleted Channel™ (DDC) process. Measured SSCG spectrum shows the reduction of the maximum peak by 16 dB for the frequency modulation ranges of 5%. At 800 MHz VCO frequency, the measured PLL RMS jitter is 8.16ps and the total power consumption is 216μW at 0.6V, whereas the same PLL in standard CMOS process consumes 701μW and shows 12.75ps RMS jitter at 0.85V. This leads to 9 dB improvement in Figure of Merit (FoM) demonstrating the benefits of using DDC process. Active die area is 0.06 mm^2.

Introduction

Key to mobile electronics is the extension of battery life which can be fulfilled by low-power and low-voltage component design. PLL is an essential clock generation building block used in virtually every SoC for various applications including the emerging Internet of Things (IoT) and wearable electronics. Designing a low power PLL is challenging since the PLL operating frequency range is constrained proportionately in low supply voltage due to reduced voltage-controlled oscillator (VCO) tuning range. Typically a CMOS VCO with 20% frequency tuning range is desirable to compensate for process and temperature variations. Additionally, low voltage PLL circuit has to cope with smaller head-room issue. To resolve these issues, we present a PLL circuit architecture allowing wide operating frequency range at the supply voltage as low as 0.6V implemented with DDC process. The DDC process has been shown to achieve ultra-low voltage SRAM operation [1] and to improve digital and analog performance [2] by aggressive reduction in random dopant fluctuation and improvement in device electrostatic characteristics. In following sections, we describe the proposed circuit architecture and report measured PLL performance difference between DDC and conventional processes.

PLL Design Issues

As the PLL operating frequencies increase while the supply voltages scale down in advanced technologies, the VCO gain (K_{VCO}, expressed in MHz/V) increases considerably resulting in a large K_{VCO}, which can degrade the PLL phase noise and spur performance severely. To achieve both wide tuning range and small K_{VCO}, the VCO frequency tuning range is divided into sub-bands with sufficient frequency overlap. Fig. 1 shows the proposed VCO architecture and simulated frequency vs. VCO tuning voltage (*Vtune*) characteristics. Note that there exists a *Vtune* range (from V_{LL} = 0.21V to V_{HL} = 0.44V) to produce the stable frequency locking as the K_{VCO} becomes too small outside this range. These voltages are used as the low and high limit of *Vtune* in the auxiliary coarse tuning (or self-calibration) loop described below. A 4-stage ring oscillator based on current starved pseudo-differential inverters is used in the VCO. The bias current of the delay cell is programmed by 6-bit DAC code which is coming from the coarse tuning loop. Supply voltage of the VCO is regulated to minimize power supply noise. Fig. 2 shows the architecture of the proposed PLL including the coarse tuning loop running continuously to guarantee a stable PLL lock over a wide frequency tuning range. Coarse tuning of the VCO is based on the measurement and comparison of *Vtune* relative to its acceptable range between V_{LL} and V_{HL}. The calibration loop consisted of comparators, counter, 6-bit current DAC, and the VCO updates the coarse tuning code to find the code that allows the fine-tuning of the main PLL loop to reach the target frequency. Fine-tuning of the VCO is done by adjusting the capacitance value of the delay cells. This calibration circuit can be applied at power-up time to lock the PLL to the target frequency and be turned off to save power consumption; or it can run all the time to adjust itself to environmental change such as temperature shift.

The VCO delay cell uses inversion-mode MOS (I-MOS) varactors driven by a differential amplifier as shown in Fig. 1a. An I-MOS has the widest tuning range than other MOS varactor structures [3] and can be scaled down easily in CMOS. A cross section and a capacitance vs. gate voltage (C-V) characteristics of an I-MOS varactor are shown in Fig. 3. Traditionally, varactor tuning is done by changing V_{SD} while keeping V_B at fixed potential of V_B = 0. However, both V_B and V_{SD} are used to extend the varactor tuning range in this work. The bias voltages (V_B and V_{SD}) have a direct impact on the flat-band voltage of the MOS capacitor (varactor) resulting in the shift of C-V curves as the MOS capacitor inversion point is changed. The differential varactor tuning voltage is generated by a single-to-differential amplifier circuit. The reference voltage (0.3V in this design) is chosen to maximize the capacitive tuning range.

Measurement Results

Efficiency of the self-calibration loop adopted in this paper was tested by changing the temperature of the chip while PLL is in operation. With the calibration circuit off, as the coarse tuning code is fixed during PLL power up, the VCO frequency could be at an unlockable place where *Vtune* is either too low or too high. Alternatively, even with a stable condition at 25°C (point-A in Fig. 4a, 4b) initially, as the temperature changes to 105°C, the VCO characteristics drifts toward higher frequency as shown in Fig. 4a, thus the operating point moves to point-C where the target frequency cannot be found. Therefore, the PLL goes to an out-of-lock state at 105°C. Contrary to this, when the calibration circuit is on, the coarse tune circuit checks the *Vtune* voltage periodically and changes the coarse tuning code to a next adjacent code when the *Vtune* goes outside the high or low limit. This process of finding a stable operating point is illustrated in Fig. 4b. Measured jitters with the calibration circuit off and on cases are shown in Fig. 4c and Fig. 4d, respectively.

The same PLL chip is fabricated using both DDC technology and conventional CMOS to compare the performance between two processes. Measured PLL locking frequency range and jitter vs. Vdd at room temperature are shown in Fig. 5. DDC process shows wider PLL operating frequency range compared to standard process due to higher gm, lower threshold voltage variations, and wider C-V varactor characteristics resulting from higher body effect. Better RMS jitter performance with DDC process is primarily coming from lower thermal noise, lower threshold voltage variation, and smaller headroom requirement. Measured operating frequency range is from 281 MHz to 1.126 GHz at 0.6V supply voltage in DDC process. Power consumption at 0.6V in DDC process is only 216 μW and RMS jitter is 8.16ps with instrument measurement error compensation (Fig. 6). Measured PLL phase noise at 0.6V power supply is shown in Fig. 7. When the supply voltage is increased to 0.9V, the operating range becomes wider, from 760MHz to 2.8GHz. The PLL also has SSCG function for the frequency modulation range from 0.5%~5% and it shows 16dB peak reduction at 5% frequency spreading for both down and center spreading as shown in Fig. 8. The chip size is 0.06 mm^2 in 55nm process. Die photo is shown in Fig. 9. In standard CMOS process, the PLL can only work down to 0.85V. The PLL built with the DDC technology-based process demonstrates 70% power reduction compared to the PLL built with conventional CMOS process, as shown in the performance comparison parameters in Table I.

References

[1] K. Fujita et. al., "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications," *IEDM Tech. Dig.,* Dec 2011, pp. 749-752

[2] L. Clark, D. Zhao, T. Bakhishev, et al., "A highly integrated 65-nm SoC process with enhanced power/performance of digital and analog circuits," *IEDM Tech.Dig.,* 2012, pp.335-338.

[3] P. Andreani, and S. Mattisson, "On the use of MOS varactors in RF VCO's," *IEEE JSSC,* vol. 35, no. 6, pp. 905–910, June 2000.

[4] Y. Lo et. al., "Designing an ultralow-voltage Phase-Locked Loop using a bulk-driven technique," *IEEE Trans. on Circuits and Systems-II,* vol. 56, no. 5, pp. 339–343, May 2009.

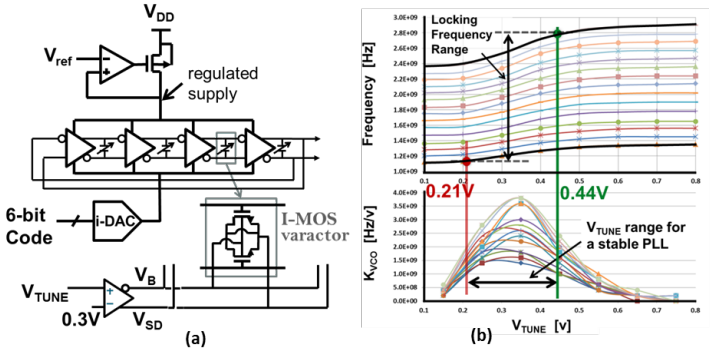

Fig. 1. (a) VCO block diagram (b) VCO characteristics, frequency range and its gain, K_{VCO}.

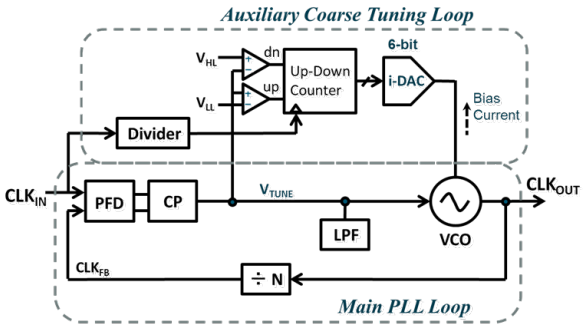

Fig. 2. PLL block diagram with an auxiliary coarse tuning (self-calibration) loop.

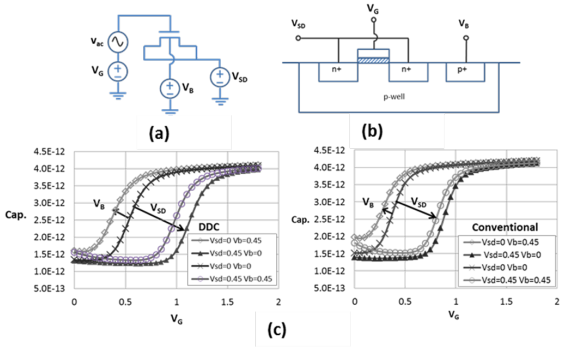

Fig. 3. (a) An inversion-mode Varactor and (b) its cross section, (c) I-MOS varactor C-V curves of DDC and conventional device for various V_B and V_{SD}.

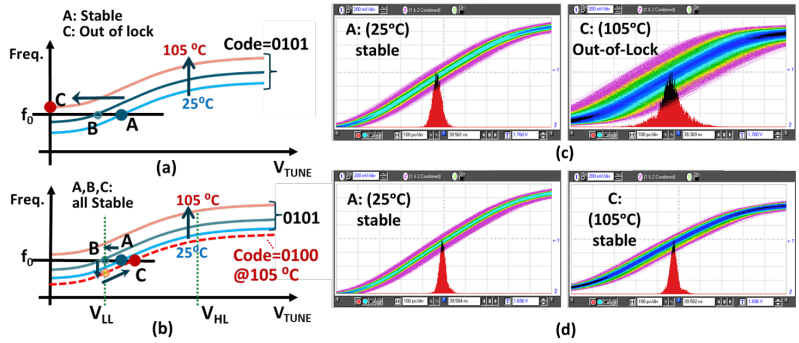

Fig. 4. An example of the *continuous coarse tune circuit effect* to temperature change during PLL operation (a) for *coarse tune* circuit OFF, (b) for *coarse tune* circuit ON. And Jitter measurements (c) with the circuit OFF, and (d) with the circuit ON.

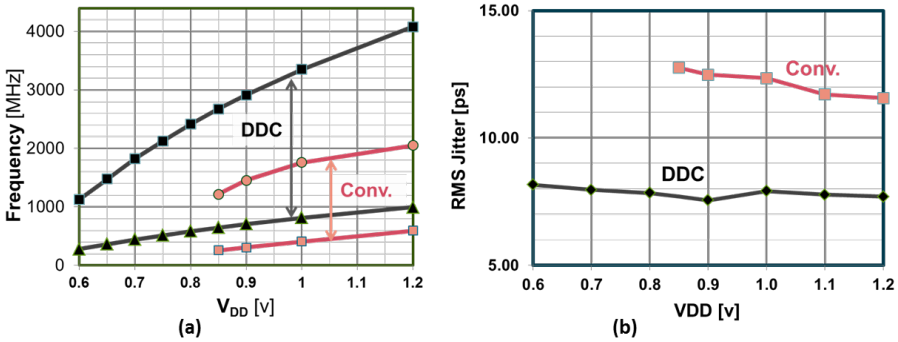

Fig. 5. Measurement results; (a) frequency locking range vs. supply voltage, (b) RMS jitter vs. supply voltage.

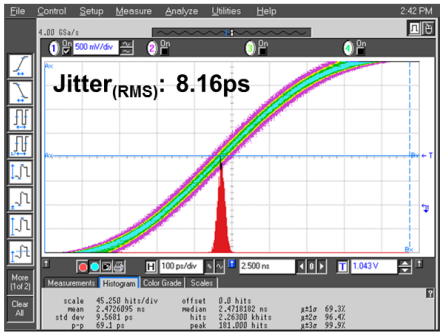

Fig. 6. Measured jitter histogram for 800MHz clock at 0.6V; PLL RMS jitter is 8.16ps after 5ps scope jitter subtracted.

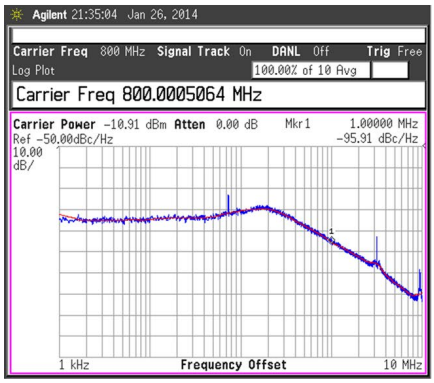

Fig. 7. Measured phase noise of PLL for 0.6V power supply.

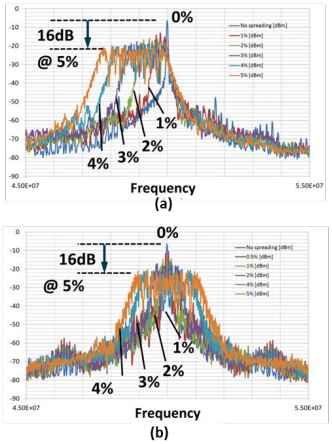

Fig. 8. Measured frequency spread spectrum of (a) down, and (b) center spreading.

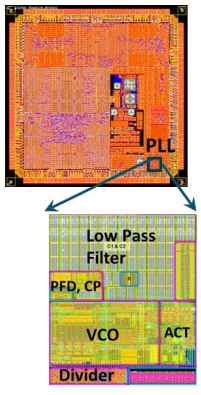

Fig. 9. Die photo and layout (A=0.06mm^2).

TABLE I
PERFORMANCE COMPARISON

	Ref[4]	This Work	
Process	0.13µm CMOS	Conventional 55nm CMOS	DDC 55nm CMOS
Supply Voltage	0.5V	0.85V	0.6V
PLL Locking Range [MHz]	360 ~ 610	257 ~ 1,218	281 ~ 1,126
RMS Jitter	8.01ps @550MHz	12.75ps @800MHz	8.16ps @800MHz
Power Comsumption	1.25mW @550MHz	701µW @800MHz	216µW @ 800MHz
Active Die Area	0.04mm^2	0.06mm^2	0.06mm^2
FoM [dB]	-221	-219	-228

* **FoM** $= 10 \cdot \log\left(Jitter^2 \cdot Power/1mW\right)$