ECEN620: Network Theory
Broadband Circuit Design
Fall 2014

Lecture 10: Voltage-Controlled Oscillators

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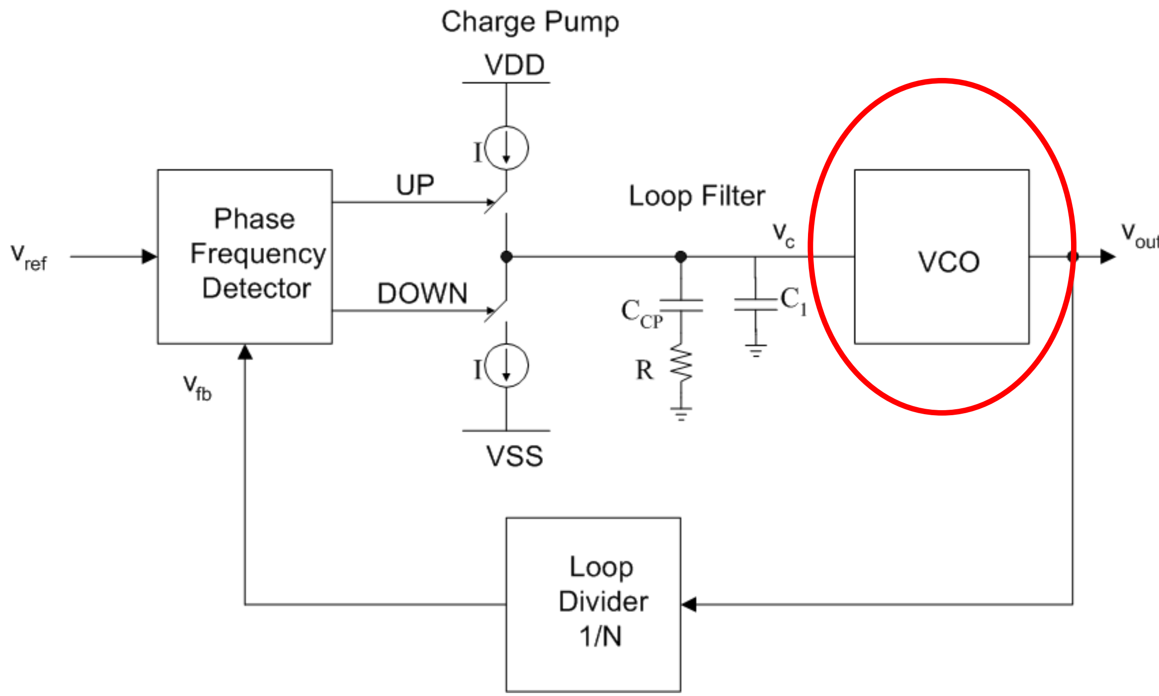
Announcements & Agenda

- HW3 is due Friday Oct 17

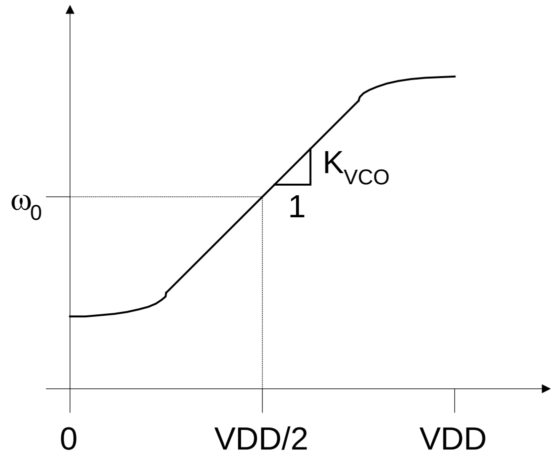
- VCO Fundamentals
- VCO Examples
- VCO Noise

Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



Voltage-Controlled Oscillator

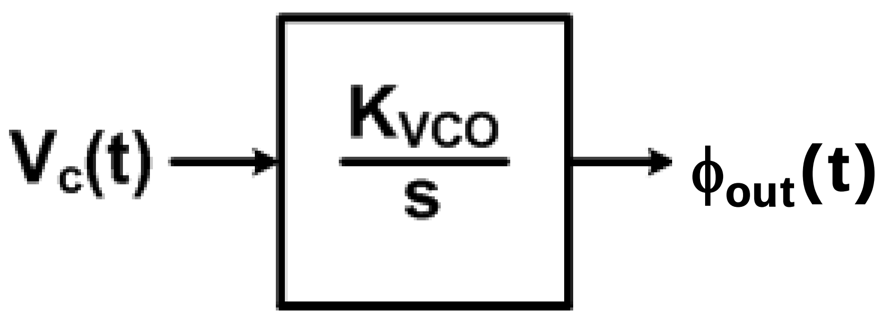


$$\omega_{out}(t) = \omega_0 + \Delta\omega_{out}(t) = \omega_0 + K_{VCO} v_c(t)$$

- Time-domain phase relationship

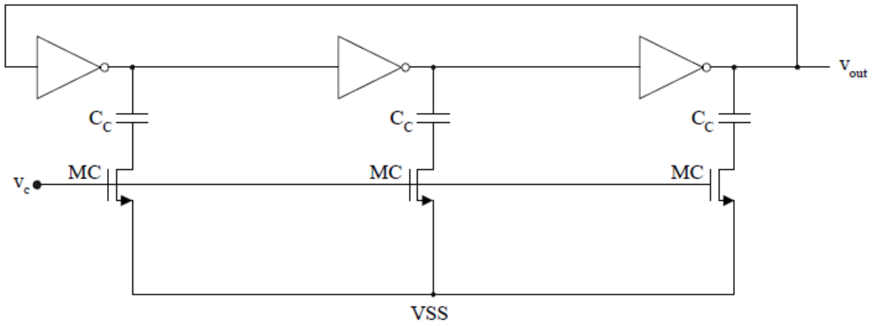
$$\phi_{out}(t) = \int \Delta\omega_{out}(t)\mathrm{dt} = K_{VCO}\int v_c(t)\mathrm{dt}$$

Laplace Domain Model

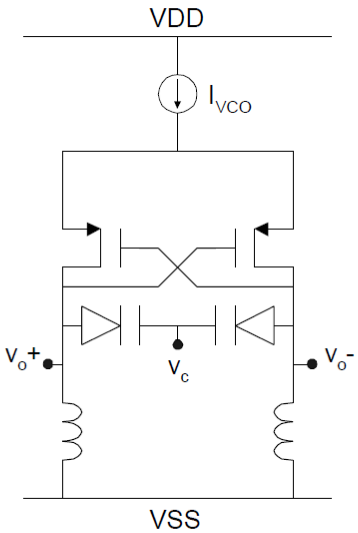


Voltage-Controlled Oscillators (VCO)

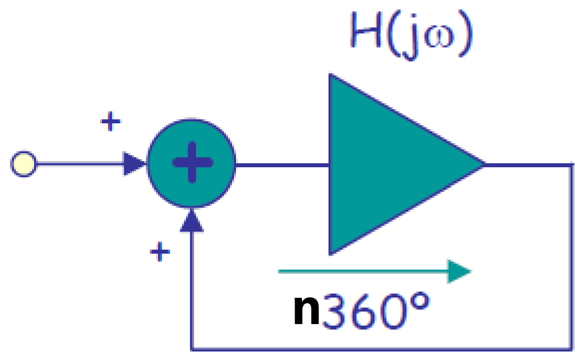
- Ring Oscillator
  - Easy to integrate
  - Wide tuning range (5x)
  - Higher phase noise



- LC Oscillator
  - Large area
  - Narrow tuning range (20-30%)
  - Lower phase noise



Barkhausen's Oscillation Criteria



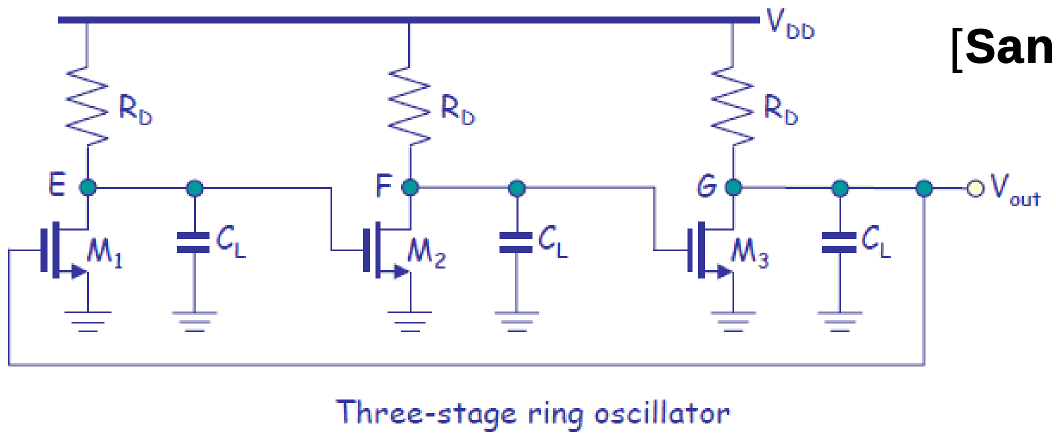
[**Sanchez**]

Closed-loop transfer function: $\dfrac{H(j\omega)}{1-H(j\omega)}$

- Sustained oscillation occurs if $H(j\omega)=1$

- 2 conditions:
  - Gain = 1 at oscillation frequency ω_0
  - Total phase shift around loop is n360° at oscillation frequency ω_0

Ring Oscillator Example



[**Sanchez**]

$$H(s) = -\frac{A_0^3}{\left(1+\frac{s}{\omega_0}\right)^3}$$

$$\omega_{osc} = \sqrt{3}\omega_0$$

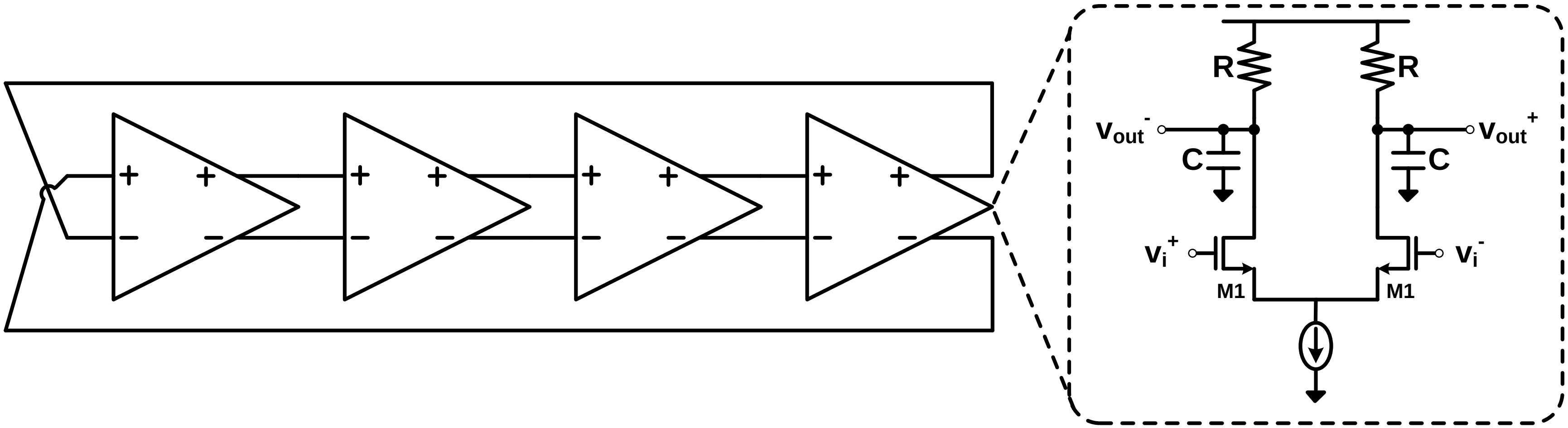
$$\tan^{-1}\frac{\omega_{osc}}{\omega_o} = 60^\circ$$

$$\frac{A_0^3}{\left[\sqrt{1+\left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right]^3} = 1$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{-A_0^3}{(1+s/\omega_0)^3}}{1+\frac{A_0^3}{(1+s/\omega_0)^3}} = \frac{-A_0^3}{(1+s/\omega_0)^3 + A_0^3}$$

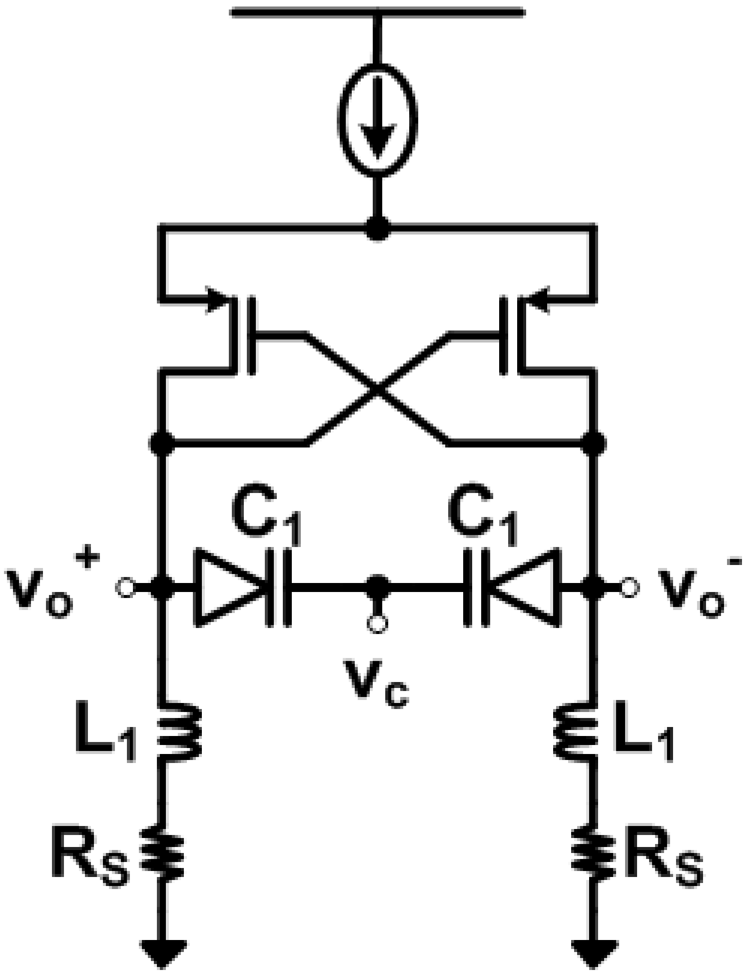
$$A_0 = 2$$

Ring Oscillator Example



- 4-stage oscillator – work this one out yourself
  - A_0 = sqrt(2)
  - Phase shift = 45°
- Easier to make a larger-stage oscillator oscillate, as it requires less gain and phase shift per stage, but it will oscillate at a lower frequency

LC Oscillator Example



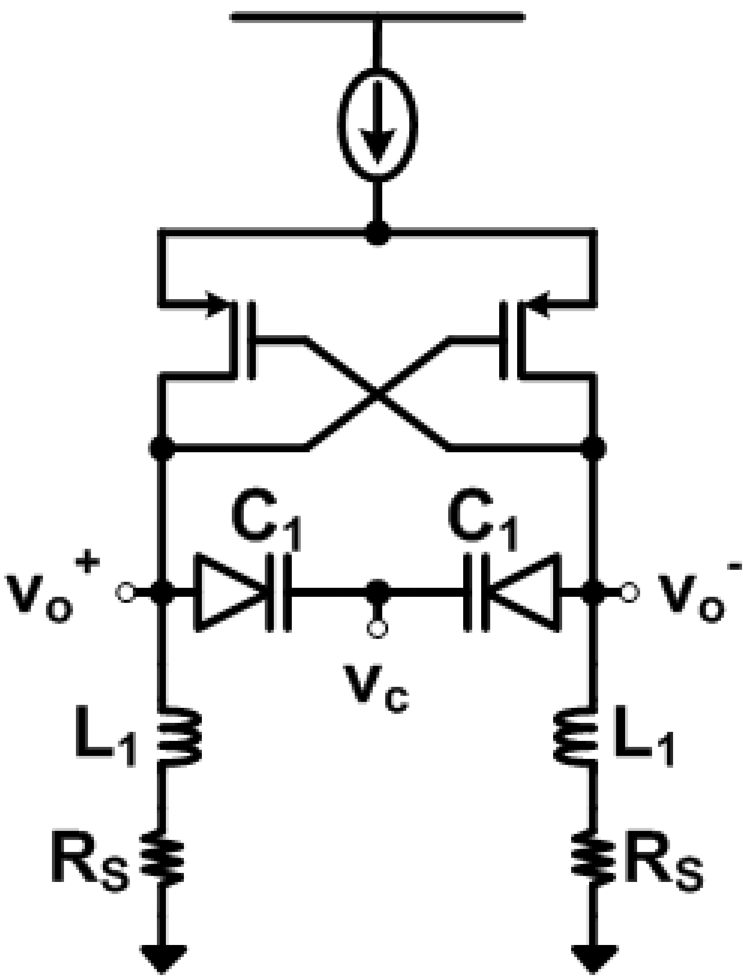
- Oscillation phase shift condition satisfied at the frequency when the LC (and R) tank load displays a purely real impedance, i.e. 0° phase shift

LC tank impedance

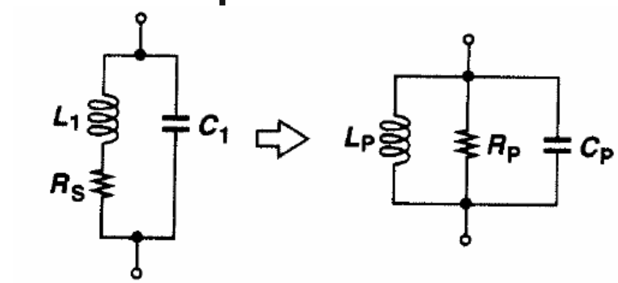
$$Z_{eq}(s) = \frac{R_S + L_1 s}{1 + L_1 C_1 s^2 + R_S C_1 s}$$

$$\left|Z_{eq}(s = j\omega)\right|^2 = \frac{R_S^2 + L_1^2 \omega^2}{\left(1 - L_1 C_1 \omega^2\right)^2 + R_S^2 C_1^2 \omega^2}$$

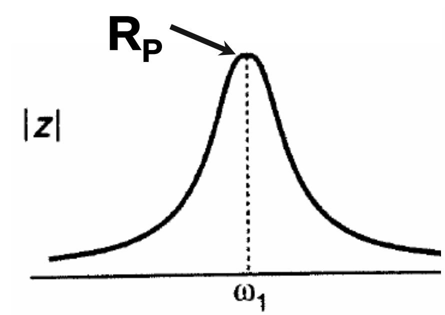
LC Oscillator Example

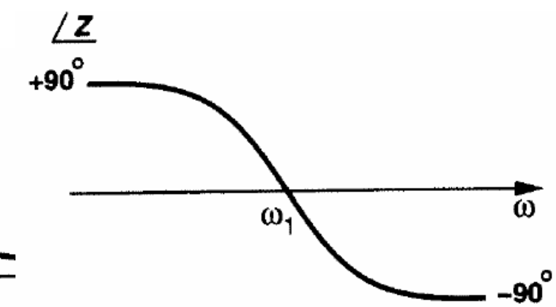


- Transforming the series loss resistor of the inductor to an equivalent parallel resistance



$$L_P = L_1\left(1+\frac{R_S^2}{L_1^2\omega^2}\right), \quad C_P = C_1, \quad R_P \approx \frac{L_1^2\omega^2}{R_S}$$

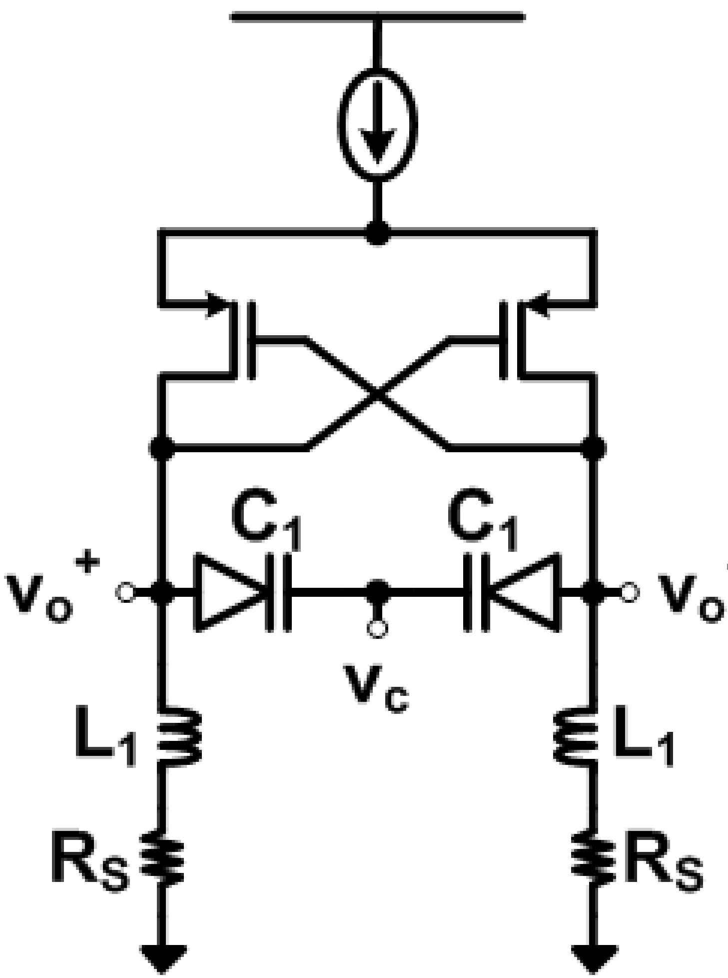




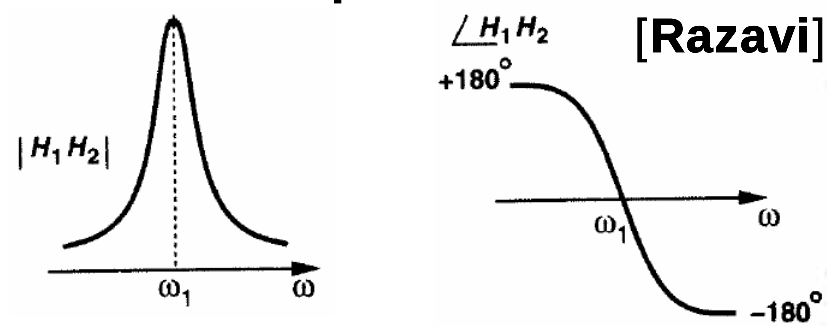
$$\omega_1 = \frac{1}{\sqrt{L_P C_P}}$$

[**Razavi**]

LC Oscillator Example



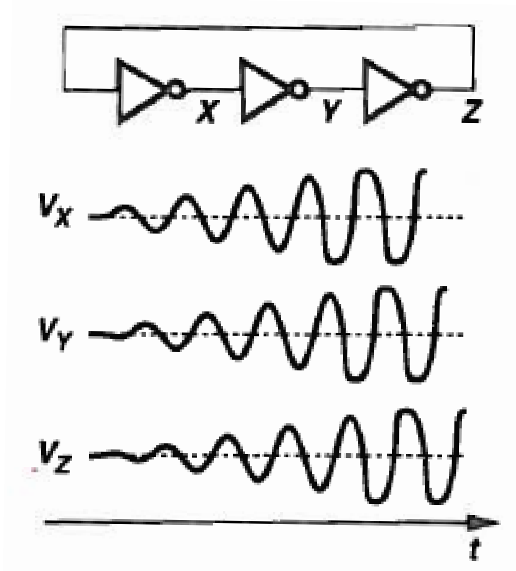
Loop Gain

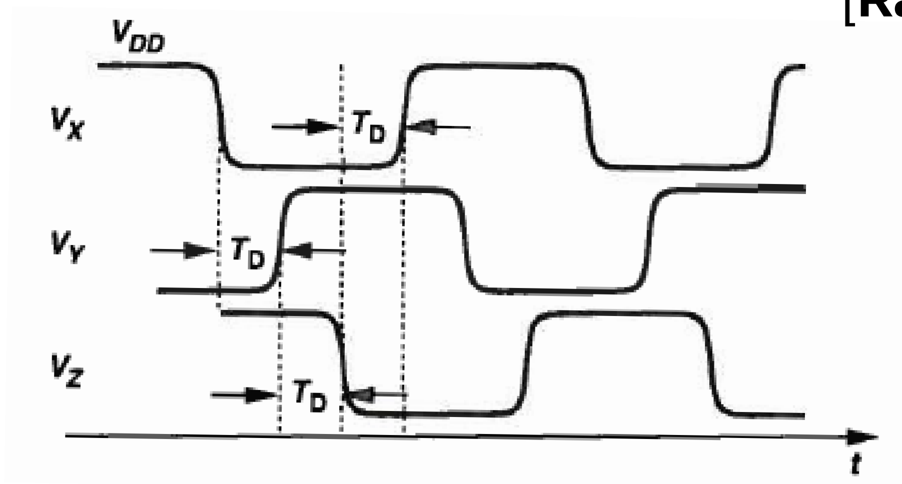


- Phase condition satisfied at $\omega_1 = \frac{1}{\sqrt{L_P C_P}}$
- Gain condition satisfied when $(g_m R_P)^2 \geq 1$
- Can also view this circuit as a parallel combination of a tank with loss resistance $2R_P$ and negative resistance of $2/g_m$
- Oscillation is satisfied when

$$\frac{1}{g_m} \leq R_P$$

CMOS Inverter Ring Oscillator



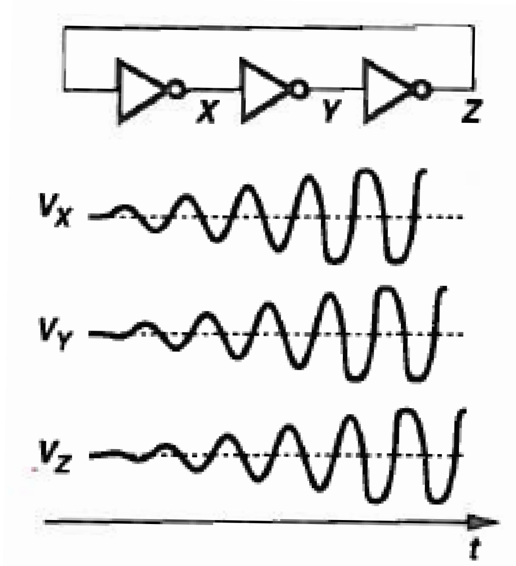


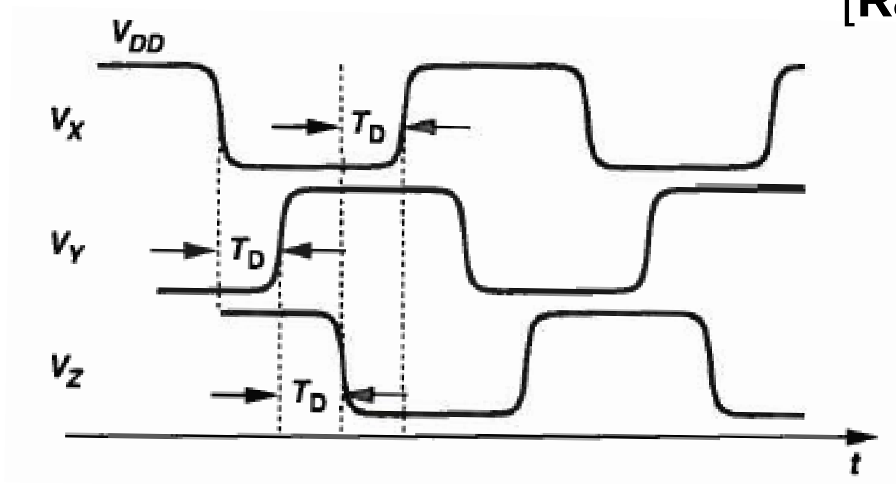
[**Razavi**]

- Noise in the system will initiate oscillation, with the signals eventually exhibiting rail-to-rail swings
- While the small-signal transistor parameters (g_m, g_o, C_g, etc...) can be used to predict the initial oscillations during small-signal start-up, these parameters can vary dramatically during large-signal operation

CMOS Inverter Ring Oscillator

[**Razavi**]

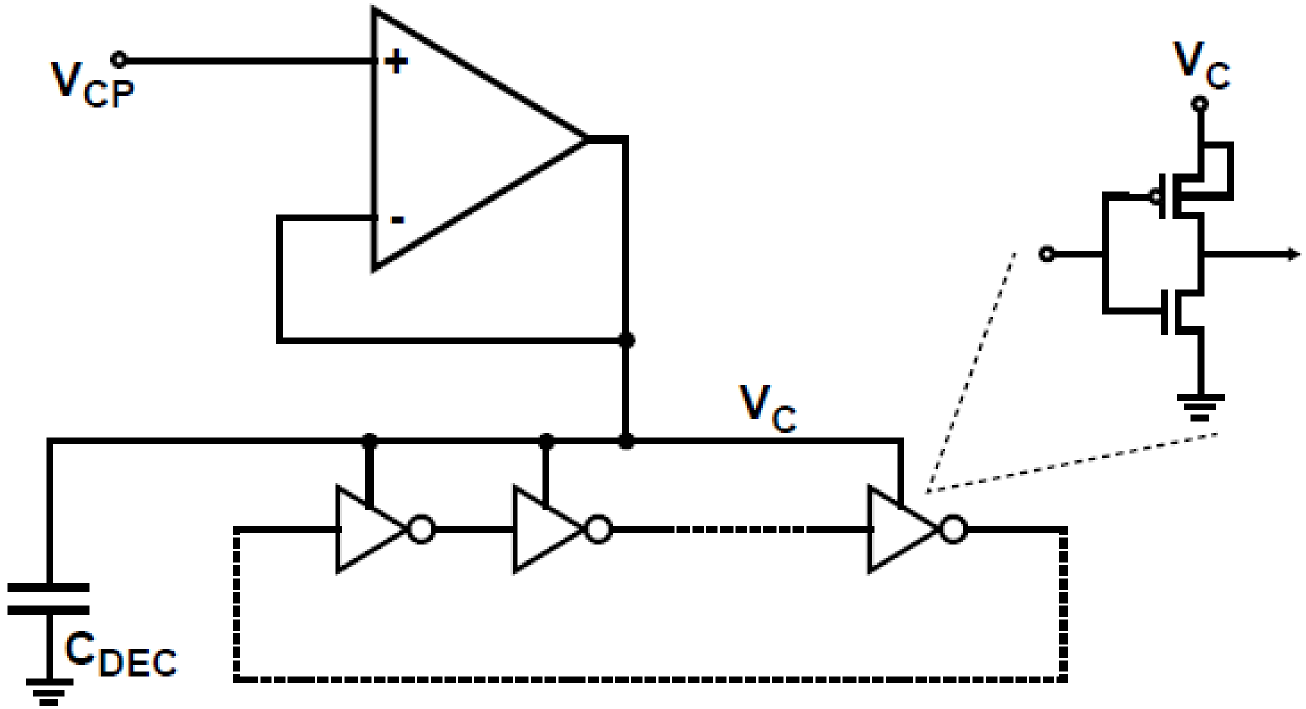




- For this large-signal oscillator, the frequency is set by the stage delay, T_D
- T_D is a function of the nonlinear current drive and capacitances of each stage
- As an "edge" has to propagate twice around the loop

$$f_{osc} = \frac{1}{6T_D}, \text{ or } \frac{1}{2NT_D} \text{ where N is the oscillator stage number}$$

Supply-Tuned Ring Oscillator

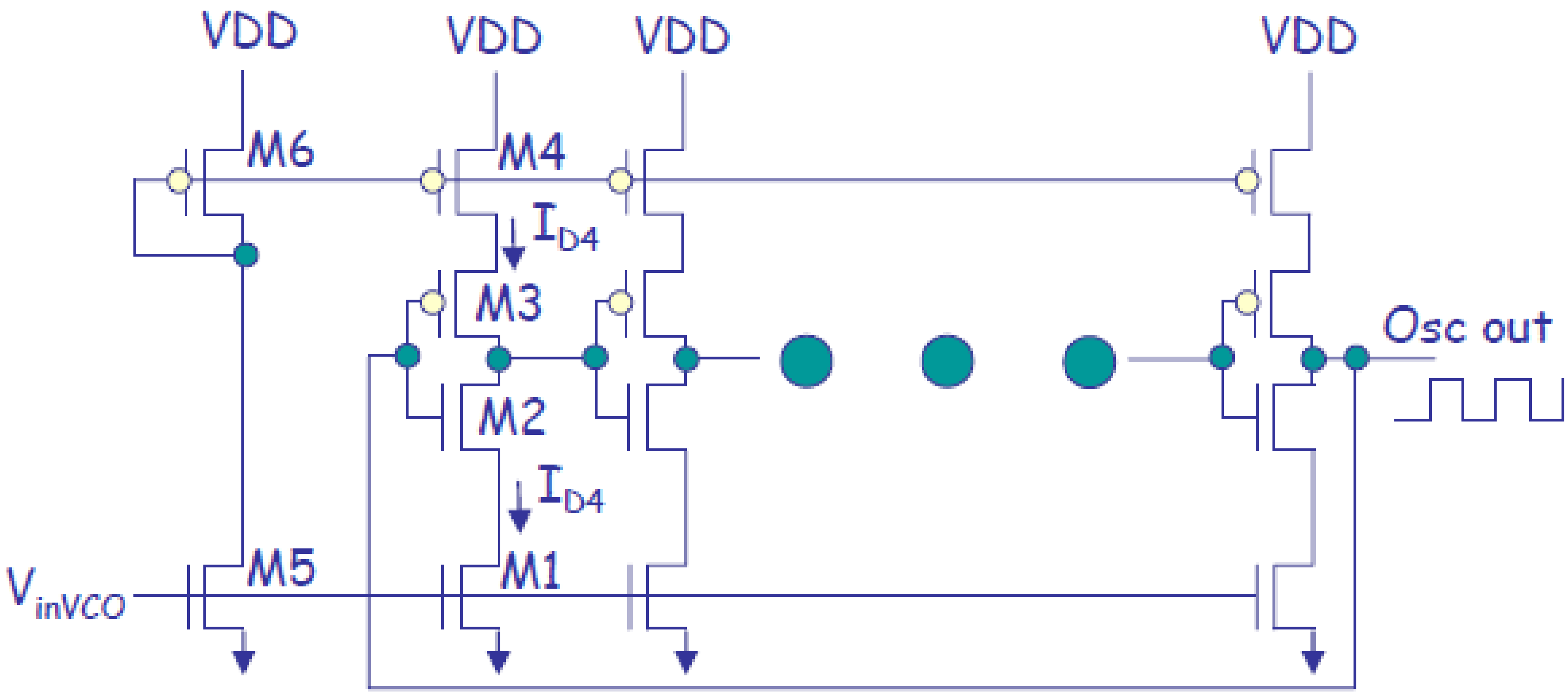


[Sidiropoulos VLSI 2000]

$$T_{VCO} = 2nT_D \approx \frac{2nC_{stage}}{\beta(V_c - V_{th})}$$

$$K_{VCO} = \frac{\partial f_{VCO}}{\partial V_c} = \frac{\beta}{2nC_{stage}}$$

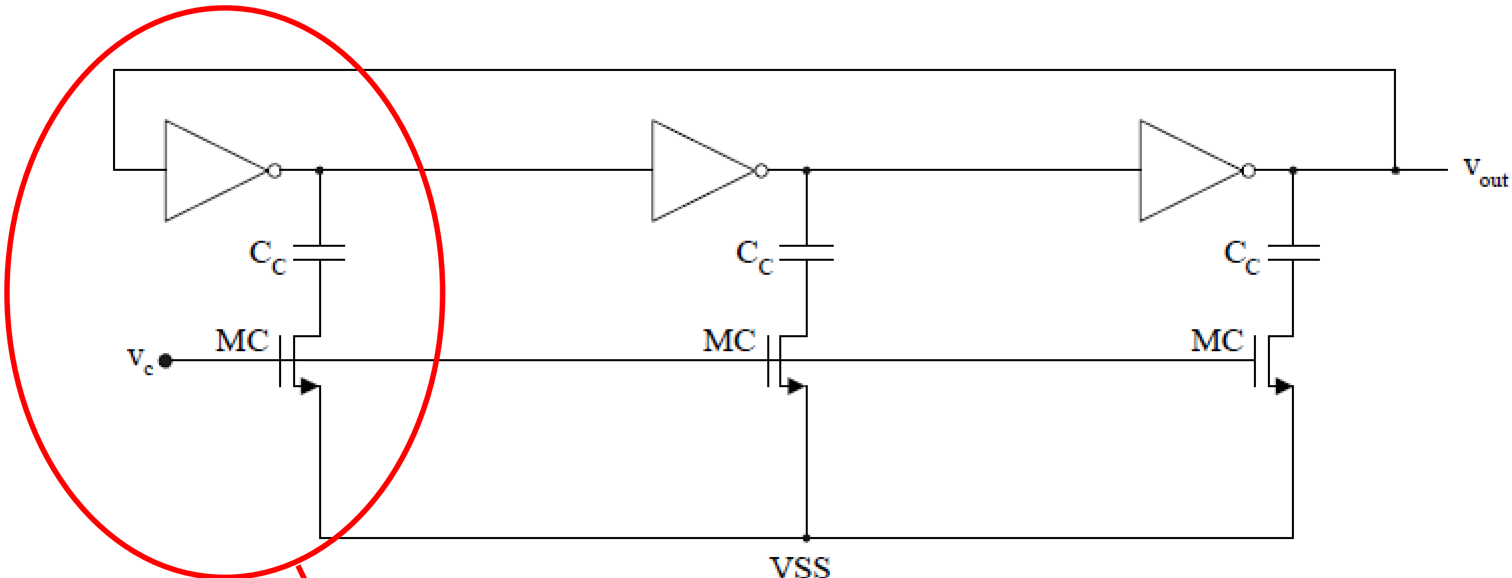
Current-Starved Ring Oscillator

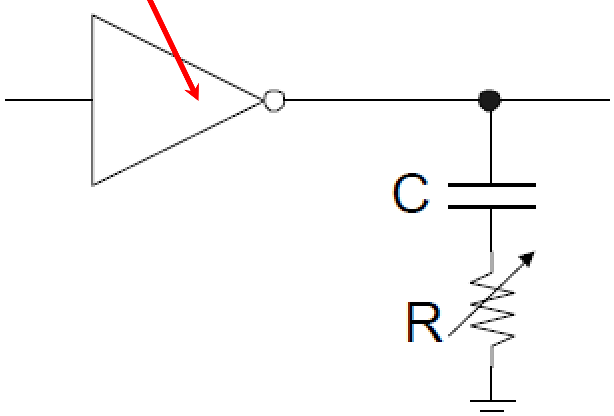


[**Sanchez**]

Current - starved VCO.

Capacitive-Tuned Ring Oscillator

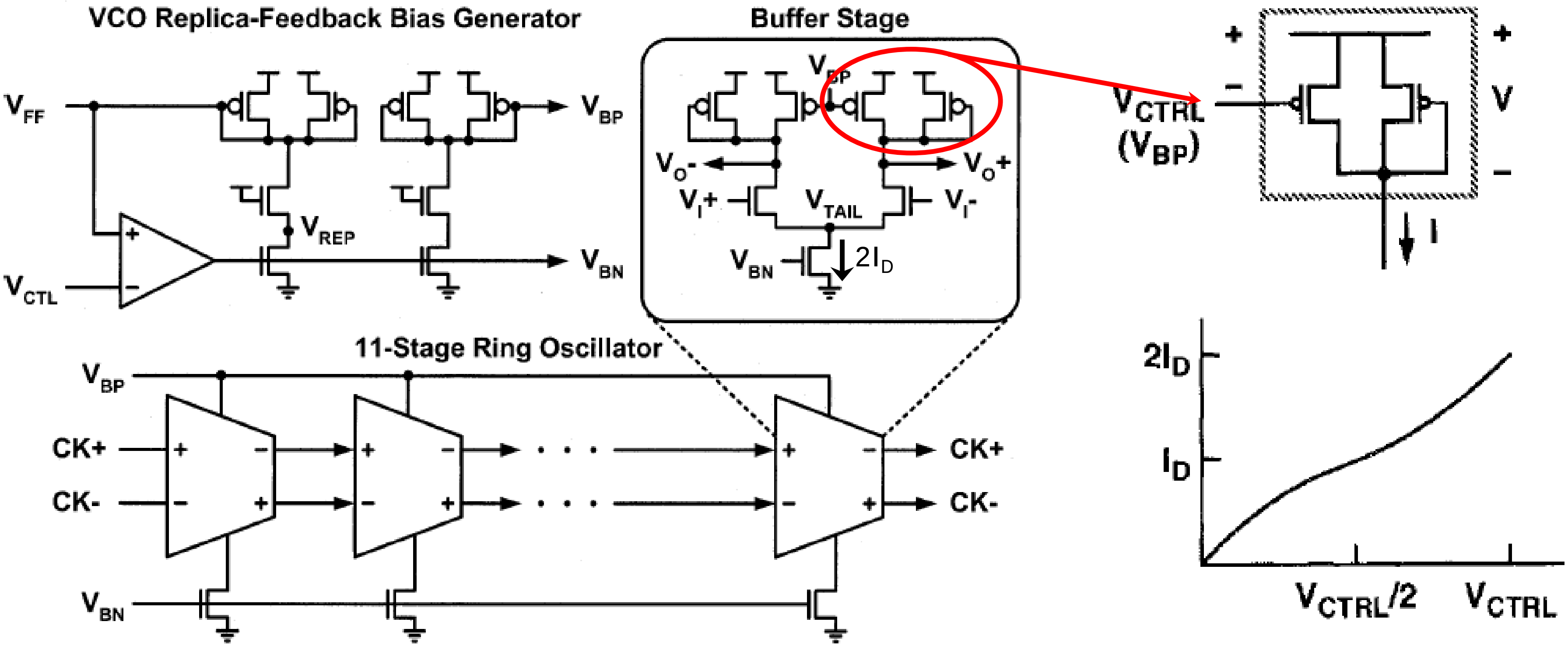




$$C_{eff} = \frac{C}{1 + sCR}$$

Symmetric Load Ring Oscillator

[Maneatis JSSC 1996 & 2003]



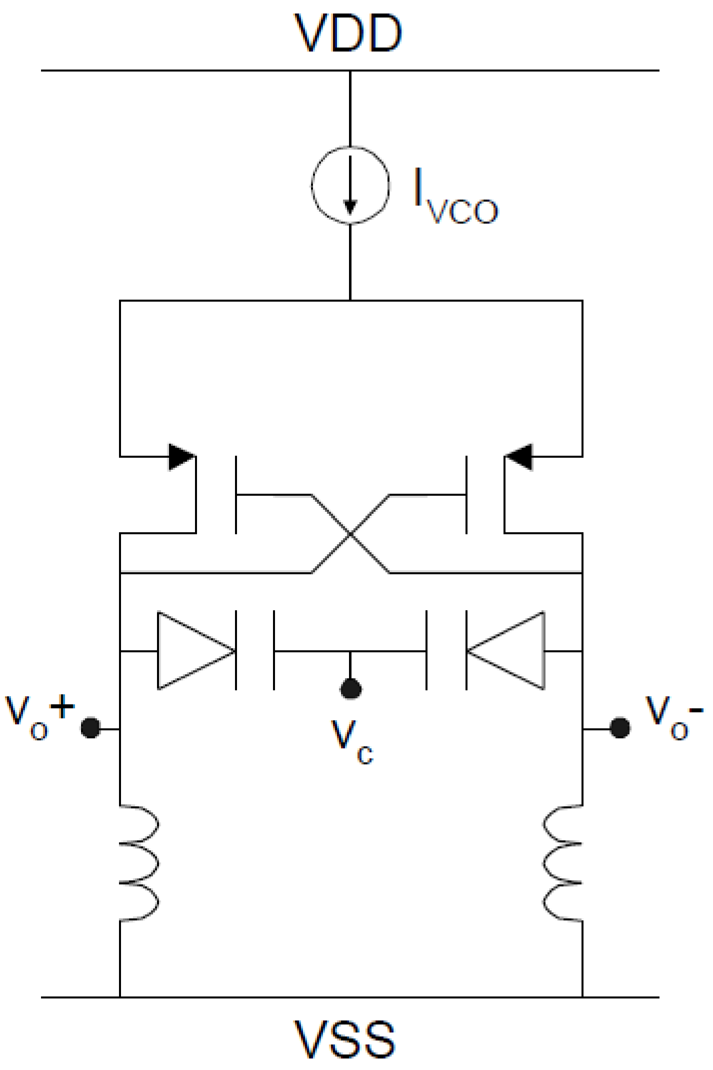
- Symmetric load provides frequency tuning at excellent supply noise rejection
- See Maneatis papers for self-biased techniques to obtain constant damping factor and loop bandwidth (% of ref clk)

LC Oscillator

- A variable capacitor (varactor) is often used to adjust oscillation frequency

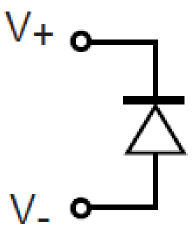
- Total capacitance includes both tuning capacitance and fixed capacitances which reduce the tuning range

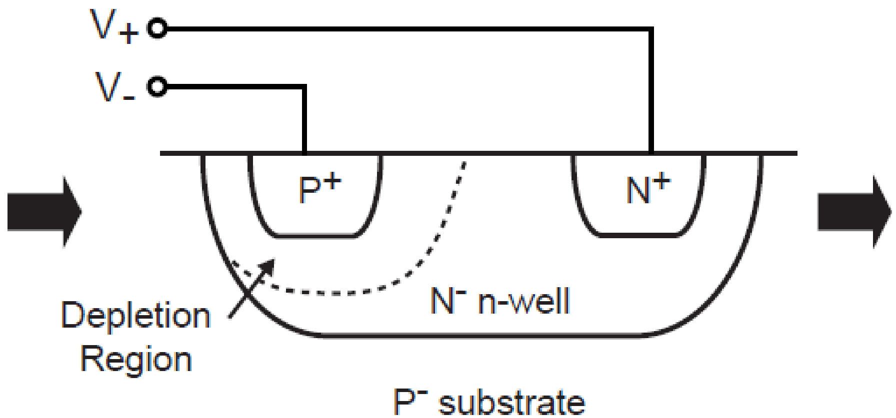
$$\omega_{osc} = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_P \left(C_{tune} + C_{fixed}\right)}}$$

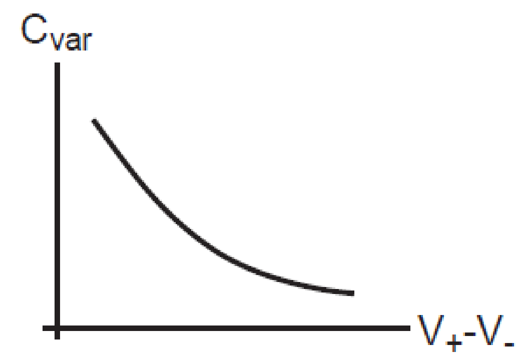


Varactors

- pn junction varactor
  - Avoid forward bias region to prevent oscillator nonlinearity

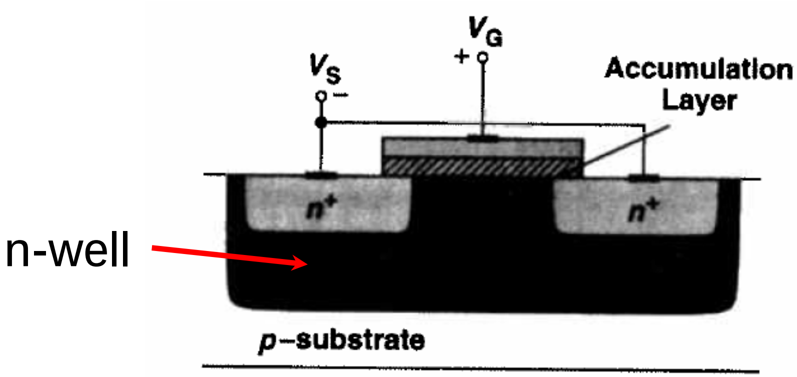


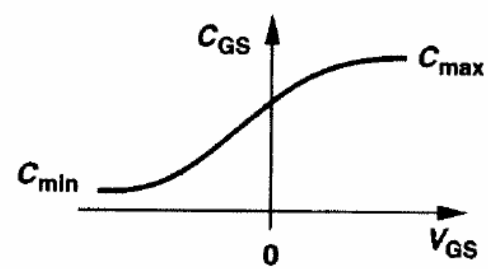




[Perrott]

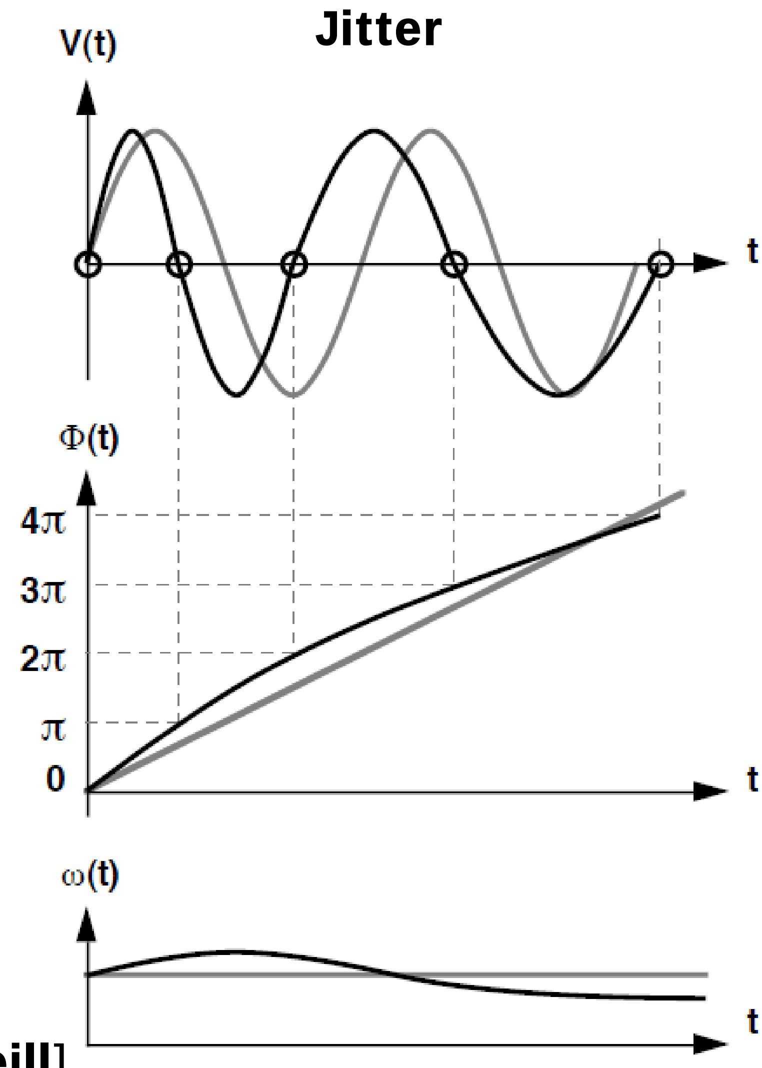
- MOS varactor
  - Accumulation-mode devices have better Q than inversion-mode



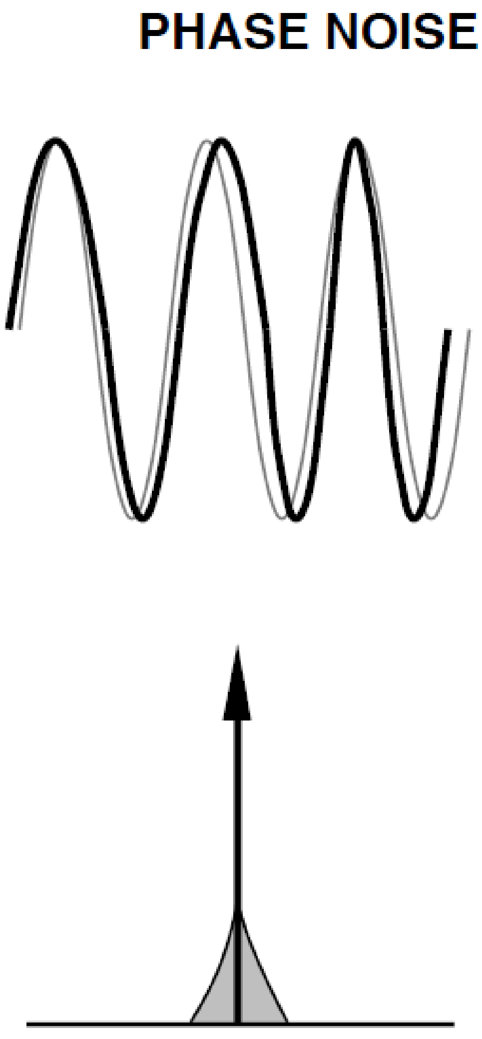


[Razavi]

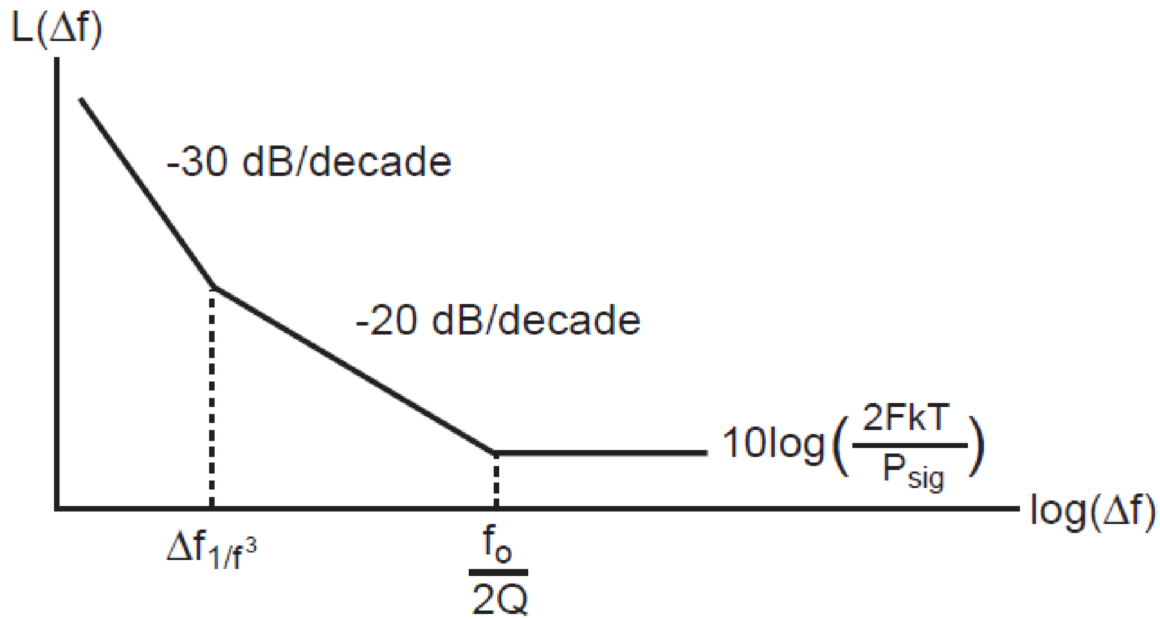
Oscillator Noise



[McNeill]



Oscillator Phase Noise Model



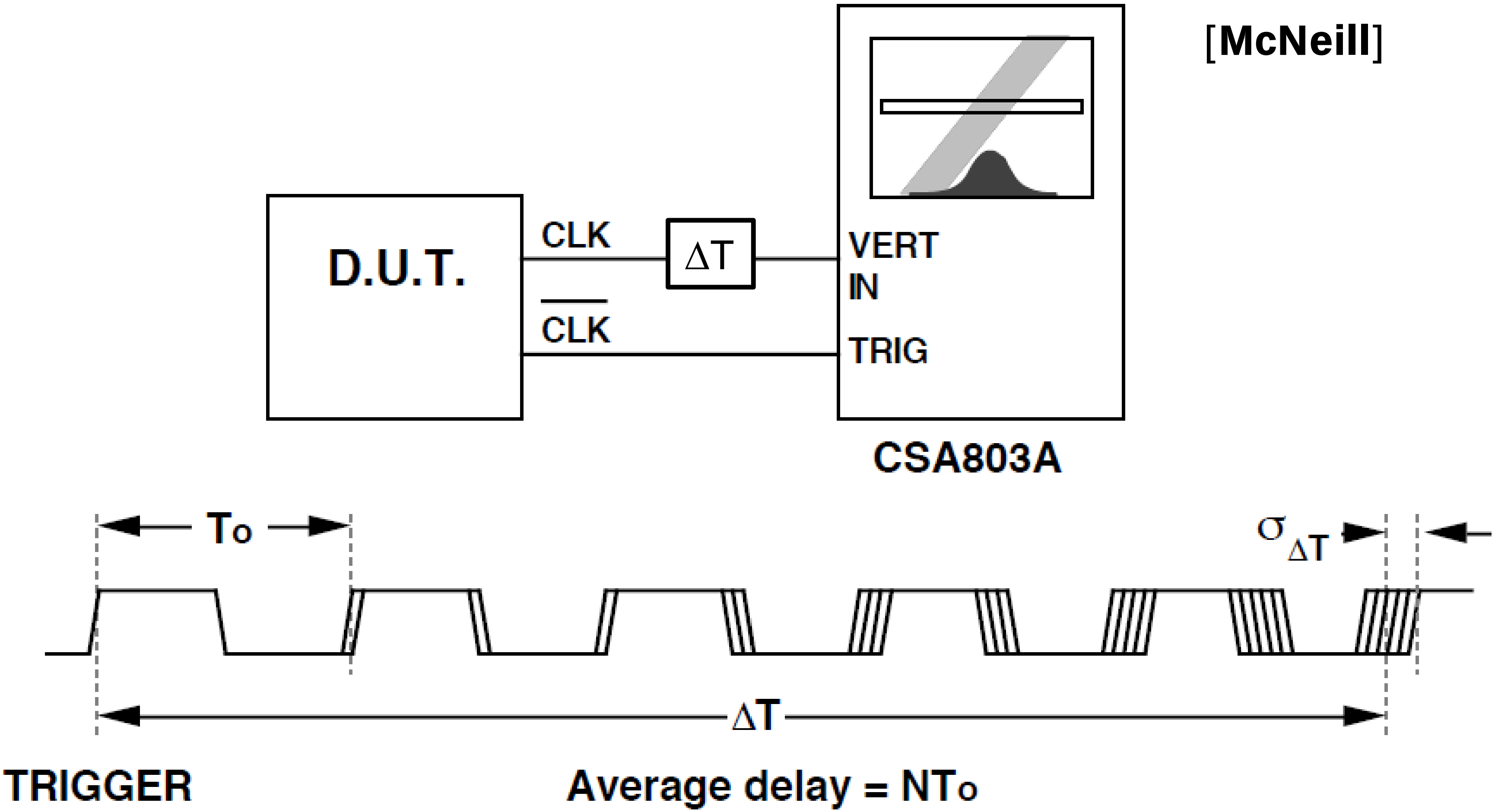
[Perrott]

$$L(f) = 10\log\left(\frac{\textbf{Noise Spectral Density}}{\textbf{Carrier Power}}\right) \ (\textbf{dBc/Hz})$$

Leeson's Model: $$L(\Delta f) = 10\log\left(\frac{2FkT}{P_{sig}}\left(1+\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right)\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right)$$

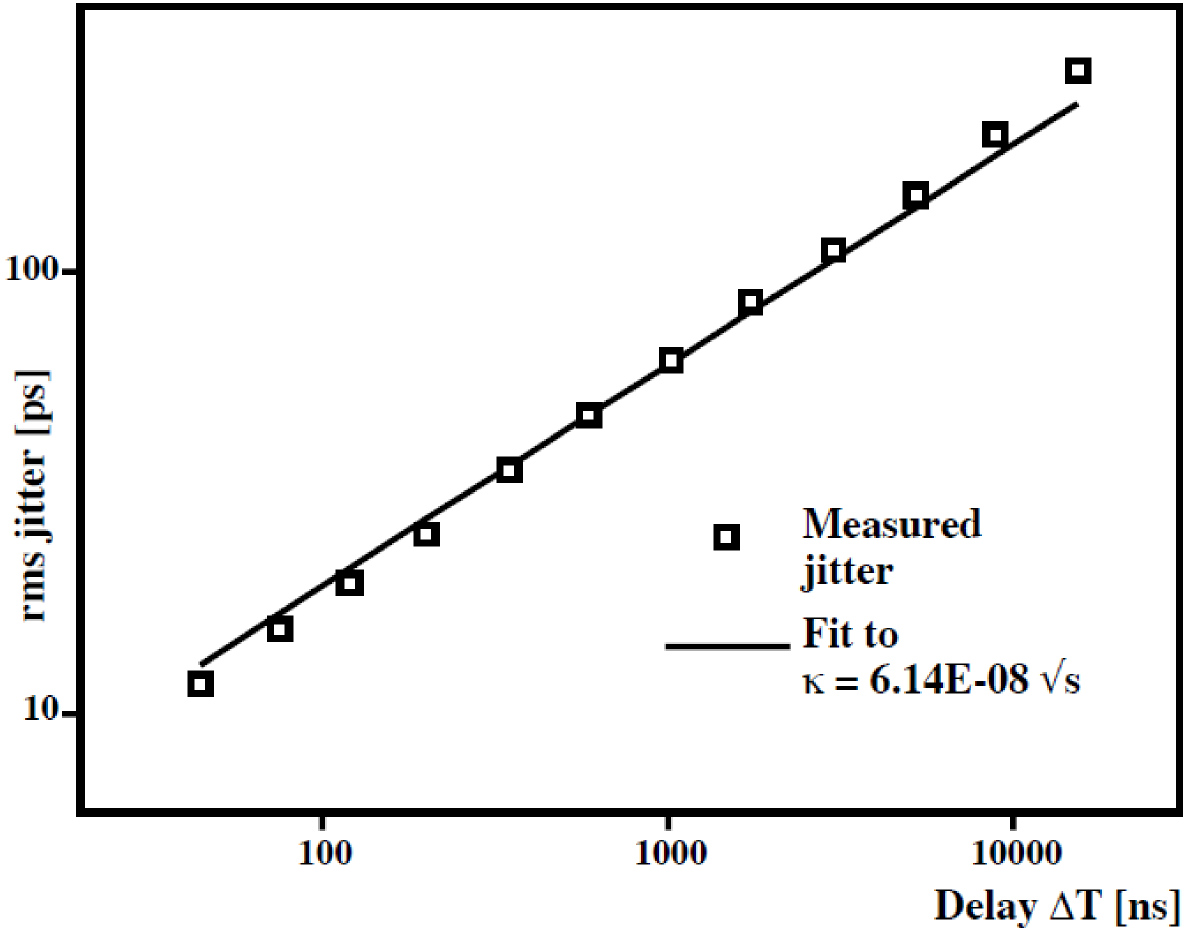
- For improved model see Hajimiri papers

Open-Loop VCO Jitter



- Measure distribution of clock threshold crossings
- Plot σ as a function of delay ΔT

Open-Loop VCO Jitter

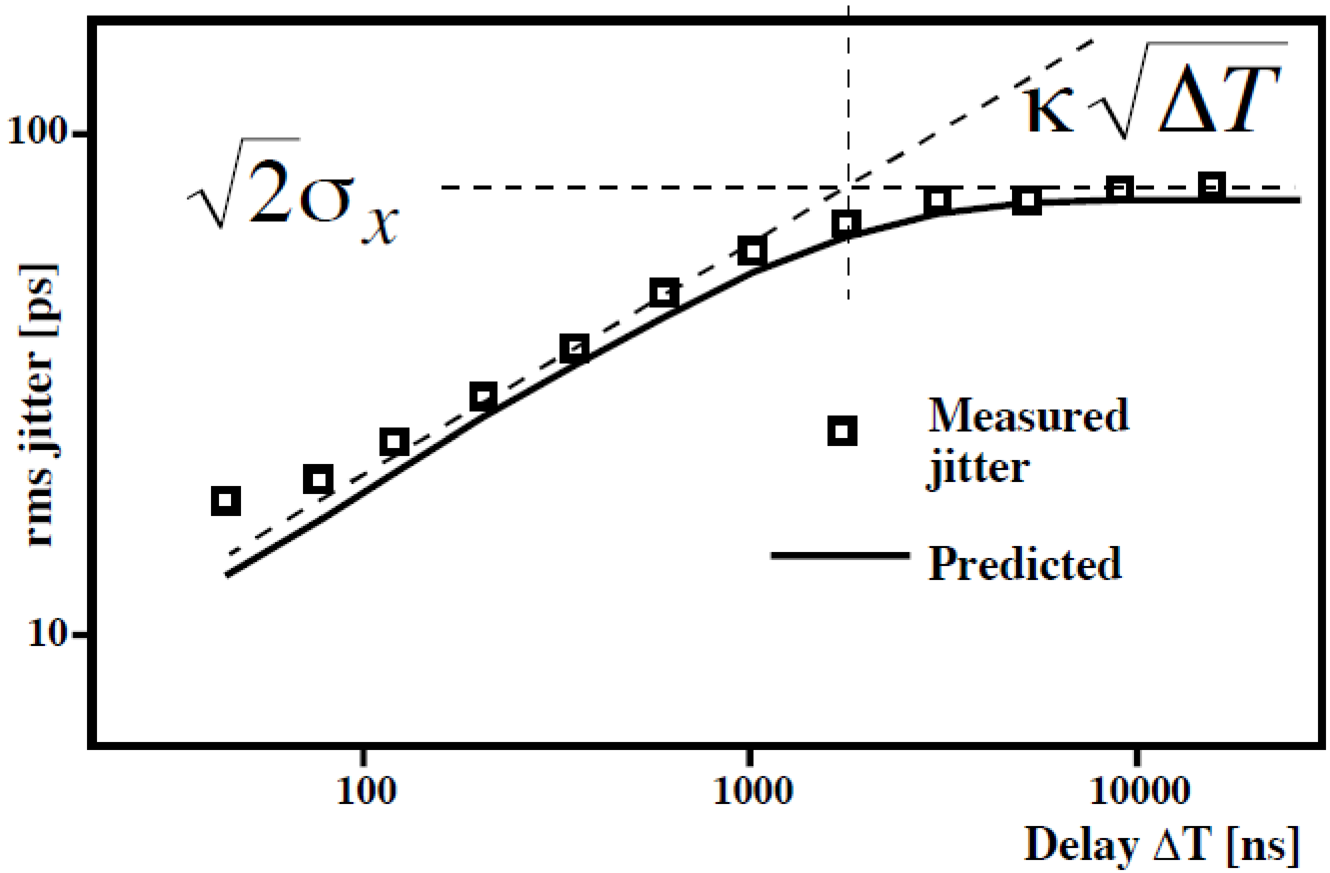


[McNeill]

$$\sigma_{\Delta T(OL)}(\Delta T) \approx \kappa \sqrt{\Delta T}$$

- Jitter σ is proportional to sqrt(ΔT)
- K is VCO time domain figure of merit

VCO in Closed-Loop PLL Jitter



[**McNeill**]

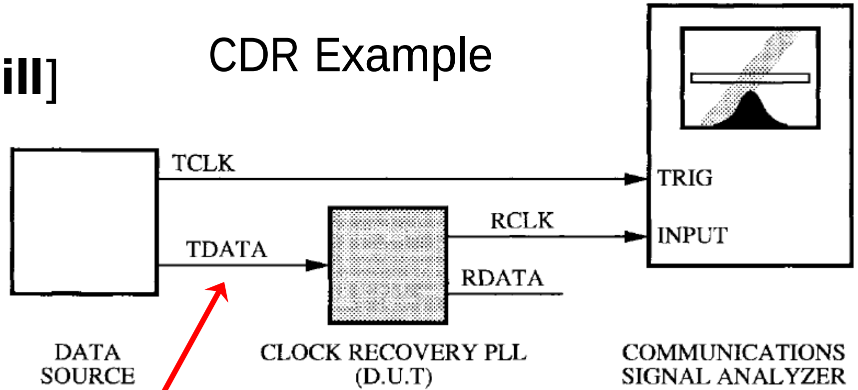
- PLL limits σ for delays longer than loop bandwidth τ_L

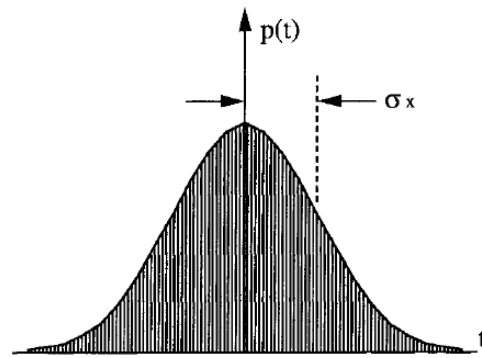
$$\tau_L = 1/2\pi f_L$$

Ref Clk-Referenced vs Self-Referenced

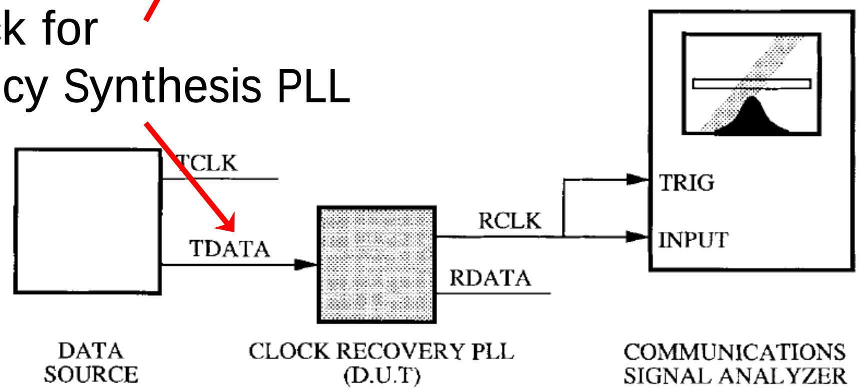
[**McNeill**]

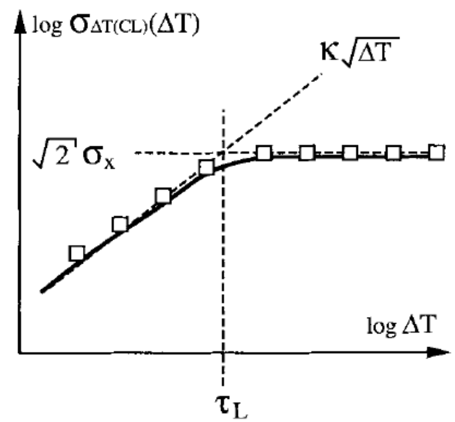
CDR Example





Ref Clock for
Frequency Synthesis PLL

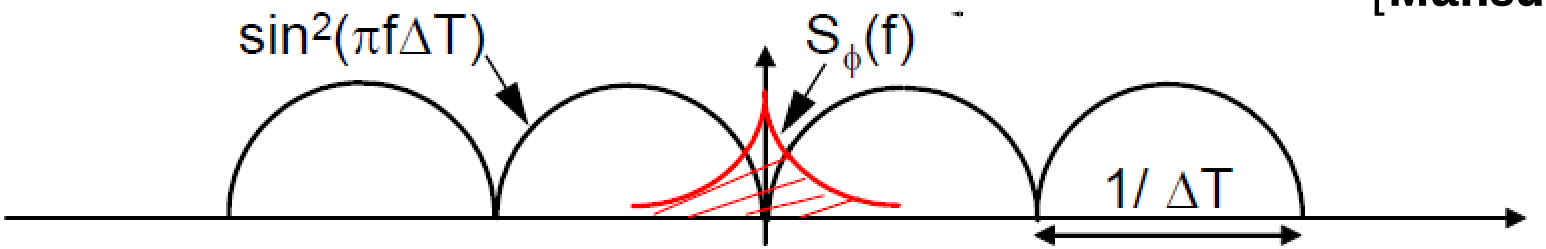




- Generally, we care about the jitter w.r.t. the ref. clock (σ_x)
- However, may be easier to measure w.r.t. delayed version of output clk
  - Due to noise on both edges, this will be increased by a sqrt(2) factor relative to the reference clock-referred jitter

Converting Phase Noise to Jitter

[**Mansuri**]



- RMS jitter for ΔT accumulation $$\sigma_{\Delta T}^2 = \frac{8}{\omega_o^2}\int_0^{\infty} S_{\varphi}(f)\sin^2(\pi f \Delta T)\,df$$
- As ΔT goes to ∞ $$\sigma_T^2 = \frac{2}{\omega_o^2} R_{\varphi}(0) = \frac{4}{\omega_o^2}\int_0^{\infty} S_{\varphi}(f)\,df$$
- Integration range depends on application bandwidth
  - f_{min} set by standard
    - Ex. Assumed CDR tracking bandwidth
  - Usually stop integration at $f_o/2$ or f_o due to measurement limitations and aliasing components

Next Time

- VCO Noise (cont.)
- Divider Circuits