EE230 RFIC II

Fall 2018

Project Description

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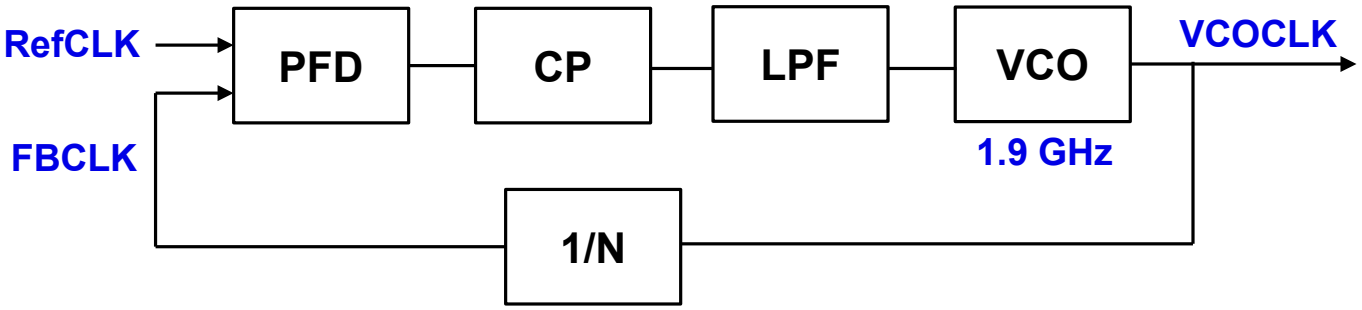
Project Description

1.9 GHz Charge Pump PLL

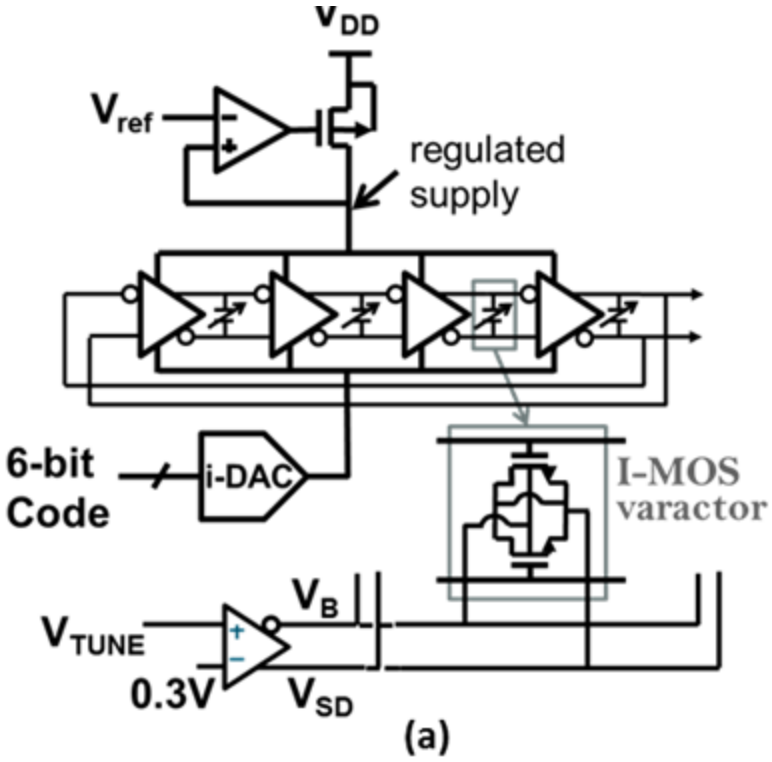


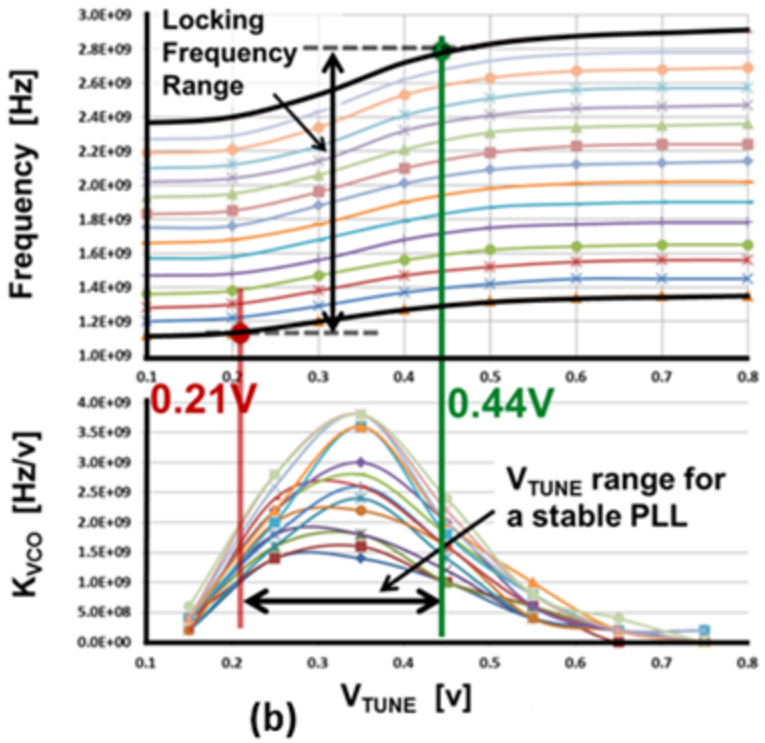
Project Logistics

1. A group of 2 students
2. Working alone is fine
3. Project presentation on Nov. 27, 29, and Dec. 4.
4. One Project Report per group
   - Report should include the followings
     - Verilog-A or Verilog-AMS model and simulation results
     - Matlab behavioral simulation showing stability
     - Schematic capture of major blocks
     - Key Simulation results
     - Summary table showing the performance achieved
   - Report should be in IEEE conference paper format
   - Project Report due : 5 PM, Dec 10

Project Description

Reference: Charge Pump PLL*





* A 216μW 281MHz-1.126GHz Self-Calibrated SSCG PLL
with 0.6V Supply Voltage in 55nm DDC™ CMOS Process – Unpublished work by Ahn & Lee

Target Spec – Beat the best

TABLE I
PERFORMANCE COMPARISON

	Ref[4]	This Work	
Process	0.13µm CMOS	Conventional 55nm CMOS	DDC 55nm CMOS
Supply Voltage	0.5V	0.85V	0.6V
PLL Locking Range [MHz]	360 ~ 610	257 ~ 1,218	281 ~ 1,126
RMS Jitter	8.01ps @550MHz	12.75ps @800MHz	8.16ps @800MHz
Power Comsumption	1.25mW @550MHz	701µW @800MHz	216µW @ 800MHz
Active Die Area	0.04mm^2	0.06mm^2	0.06mm^2
FoM [dB]	-221	-219	-228

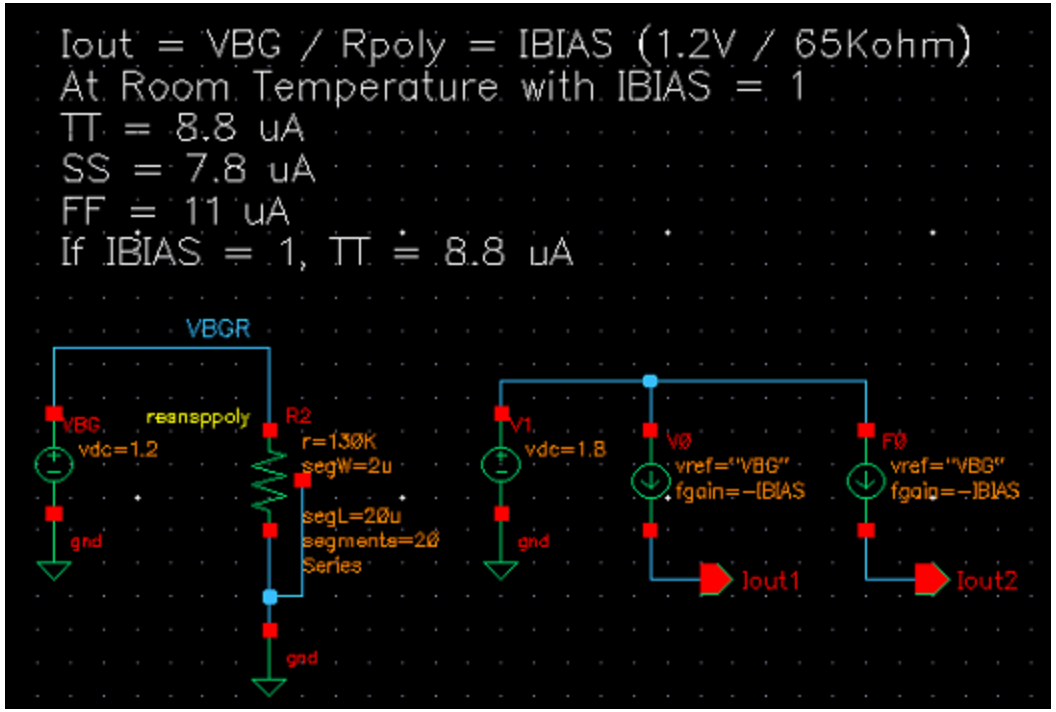
* $\mathbf{FoM} = 10 \cdot \log\left(Jitter^2 \cdot Power/1mW\right)$

Design Constraint

- Architecture: Type-II Integer-N Charge Pump PLL
- Goal is to achieve FoM < -220 dB with the following constraint
  - Use 45nm technology PDK in gpdk045
  - VDD=1V
  - Device types available for the design
  - → nmos1v, pmos1v, resnsppoly, Ideal cap
  - RefCLK = 30 MHz
  - Bias Current : Use “ideal_bias” current cell in the next slide
  - PVT corners
    - TT, 1V, 27C
    - SS, FF
    - 0.9V, 1.1V
    - -40C, 125C

Bias Current

Lib: ee288lib
Cell: ideal_bias
Choose different value for IBIAS to vary the output current level



References

- PLL
  - Rishi Ratan, From Chapter 3, MS Thesis, UIUC, 2014
  - H. Ahn and S. Lee*, File name: VLSI2014_PLL_v7*
- Verilog-A
  - VCO_VerilogA_ECE546_UIUC
  - PLL_Jitter_measurement_in_Spectre
- Verilog-AMS
  - Rishi Ratan, Chapter 6, MS Thesis, UIUC, 2014
- Jitter measurement
  - PLL_Jitter_measurement_in_Spectre
  - https://www.youtube.com/watch?v=VvkHPoSVpVc