Verilog-AMS Simulation in Cadence

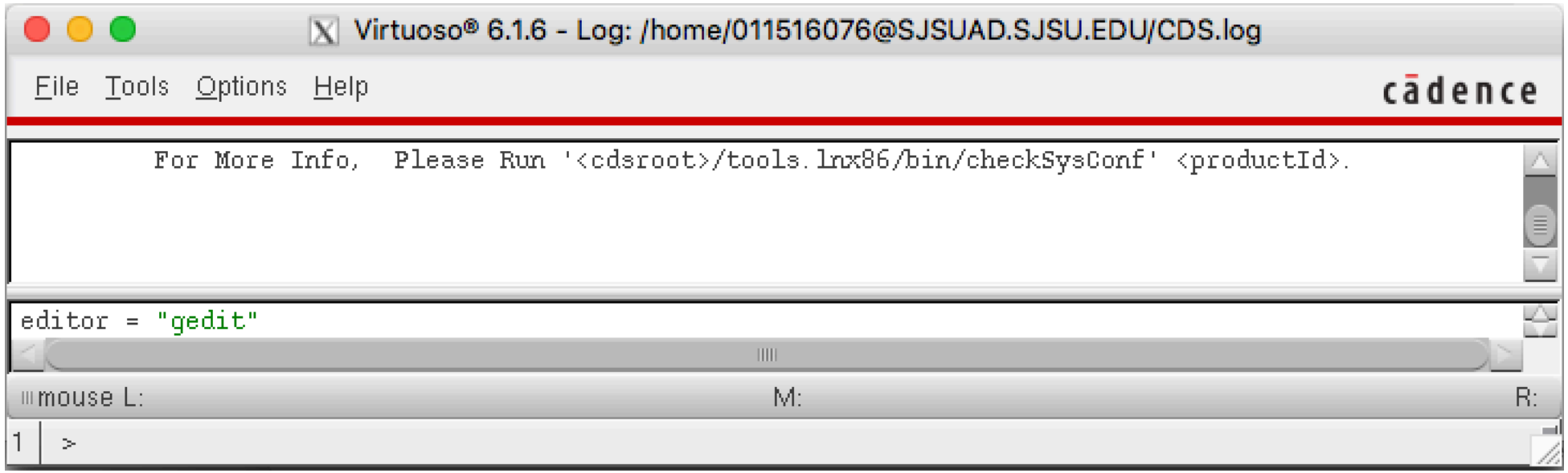
File Setup

- In cds.lib file in st45 folder add the line:

```
DEFINE connectLib /apps/cadence/IUS/tools/affirma_ams/etc/connect_lib/connectLib
```

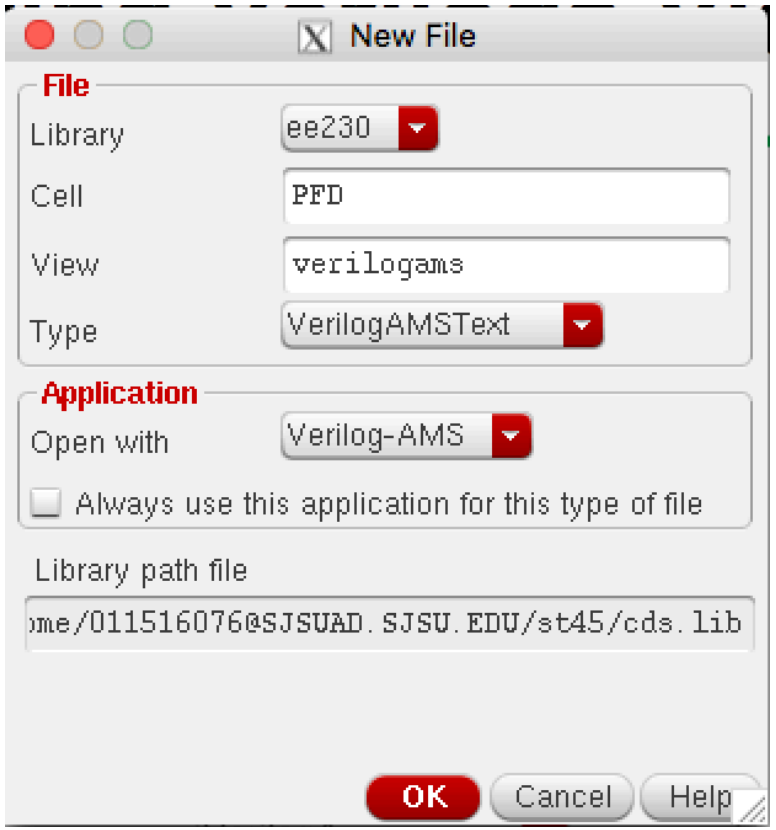
Set Text Editor

- In CIW window type:
  editor = “gedit”



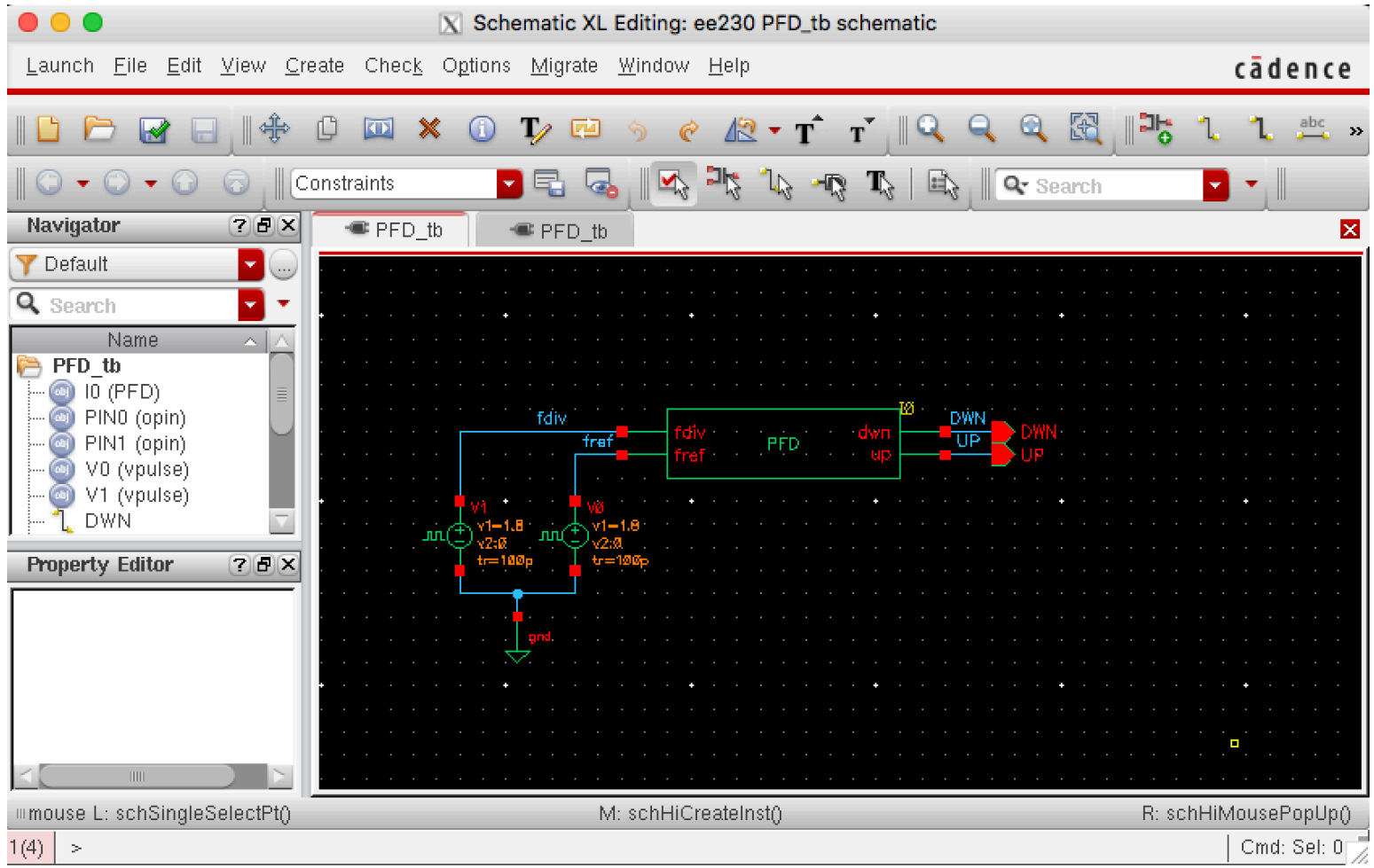
Create Verilog-AMS View

- From CIW window: File -> New -> Cellview
- Enter Verilog-AMS code into the verilog.vams file that opens
- Save and close the verilog.vams file. If there are no errors you will be prompted to create a symbol for your verilog-AMS block, select “Yes”



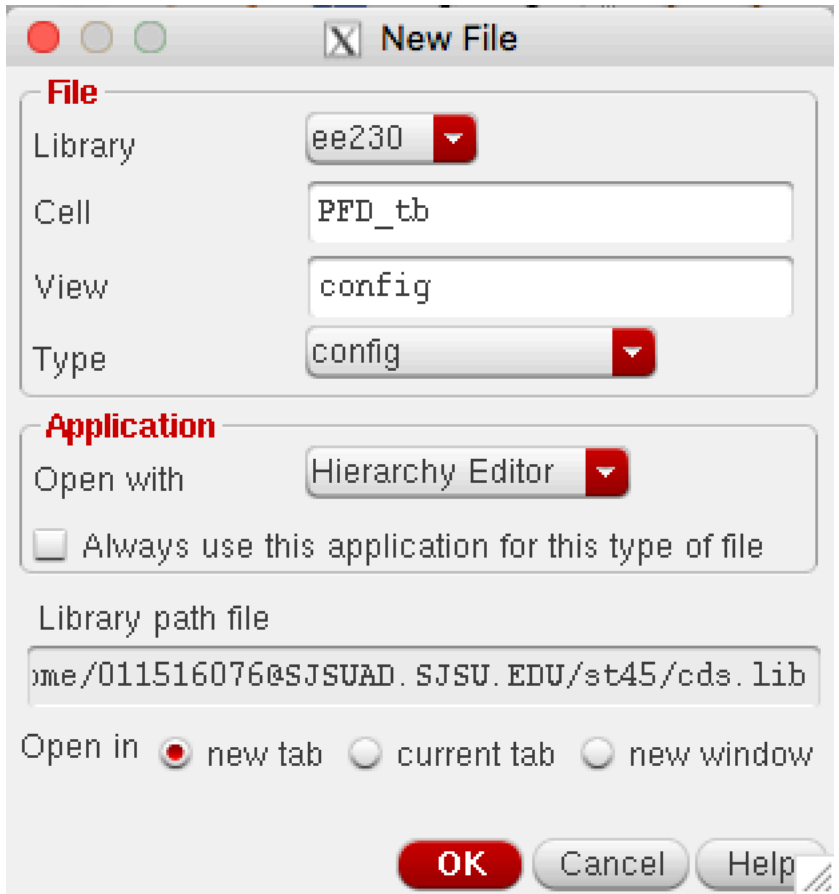
Create Test Bench

- Using the symbol that was just created, build a test bench schematic

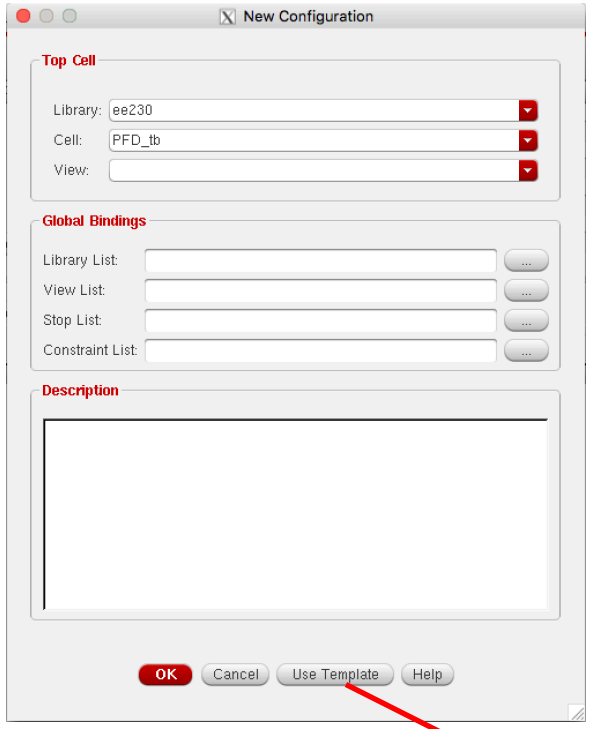


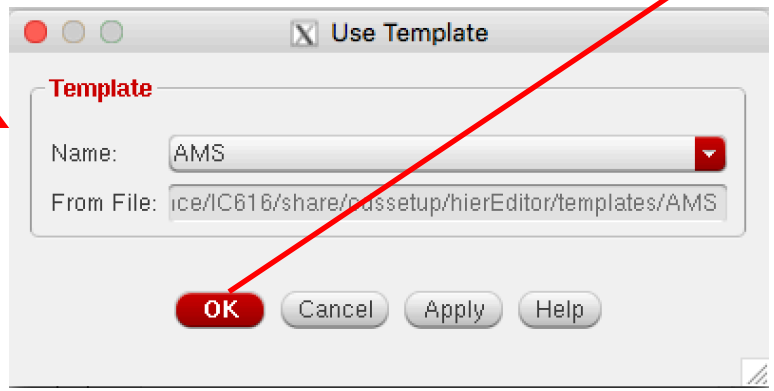
Create Config File

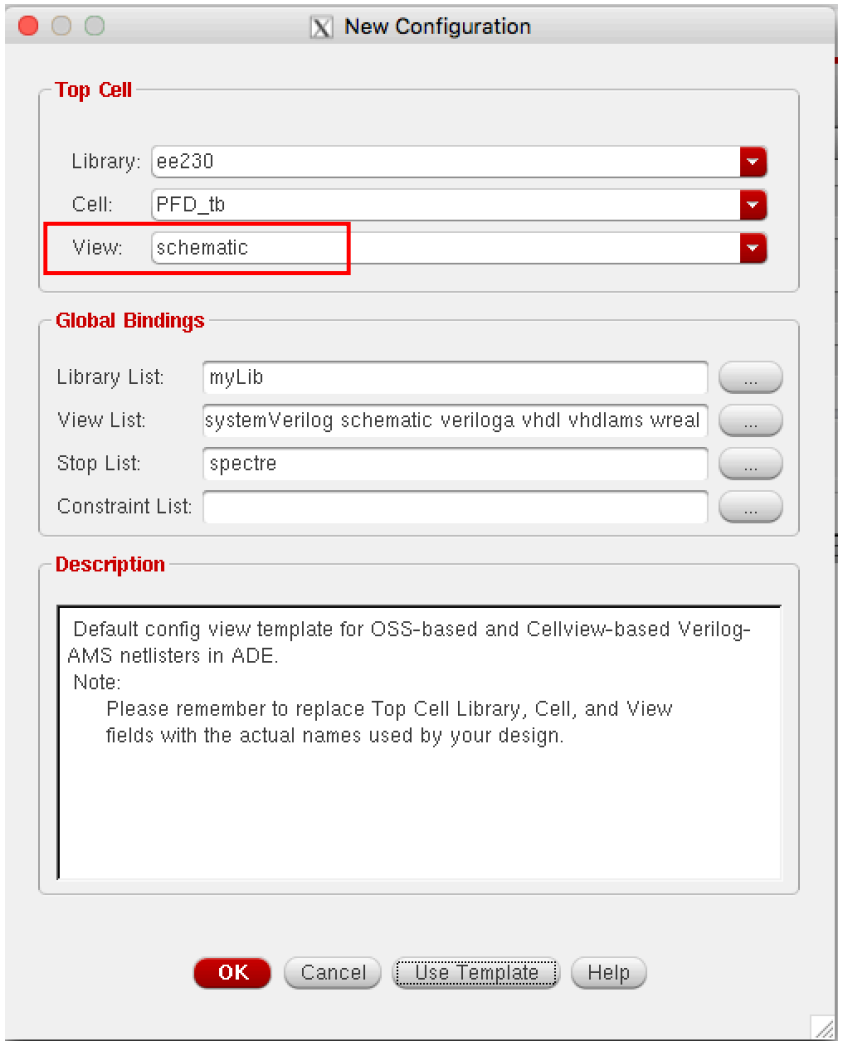
- Create a new config cellview with the same cell name (PFD_tb) as your test bench schematic



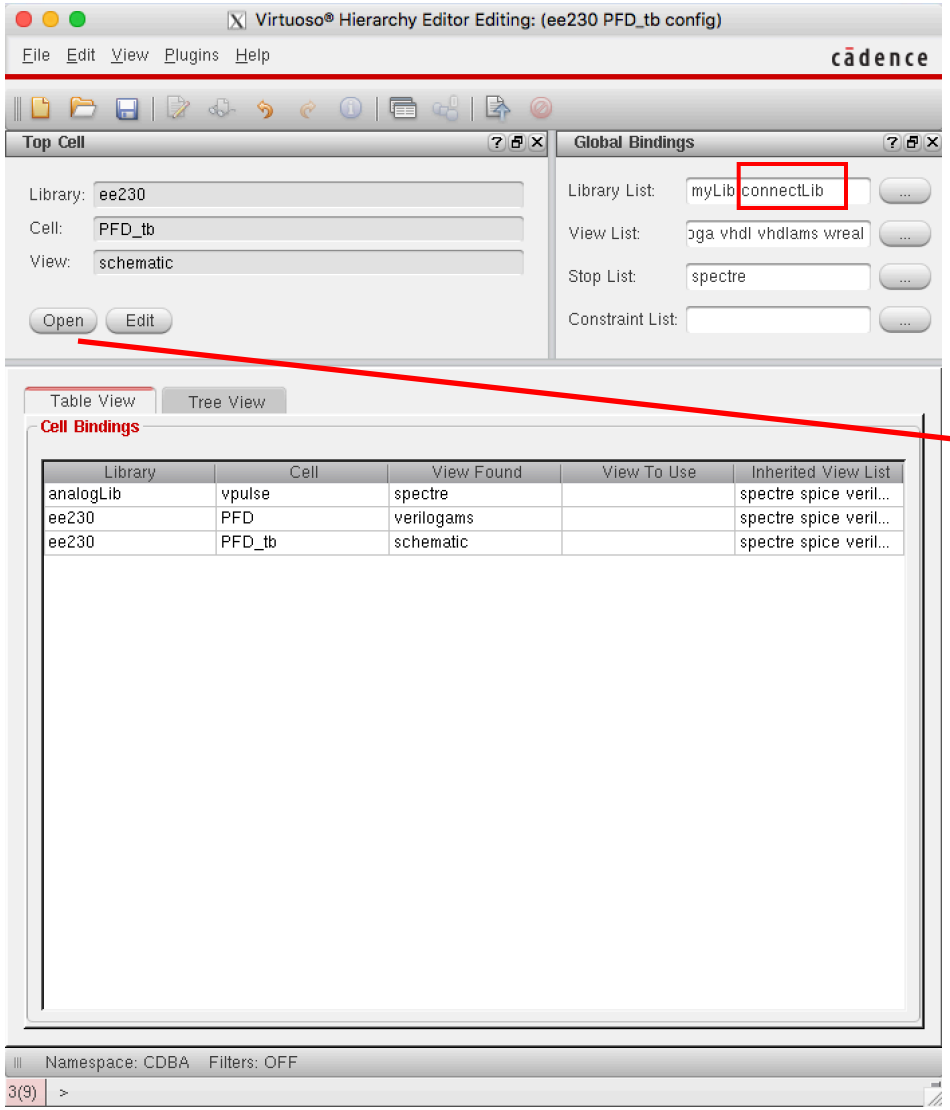
Create Config File

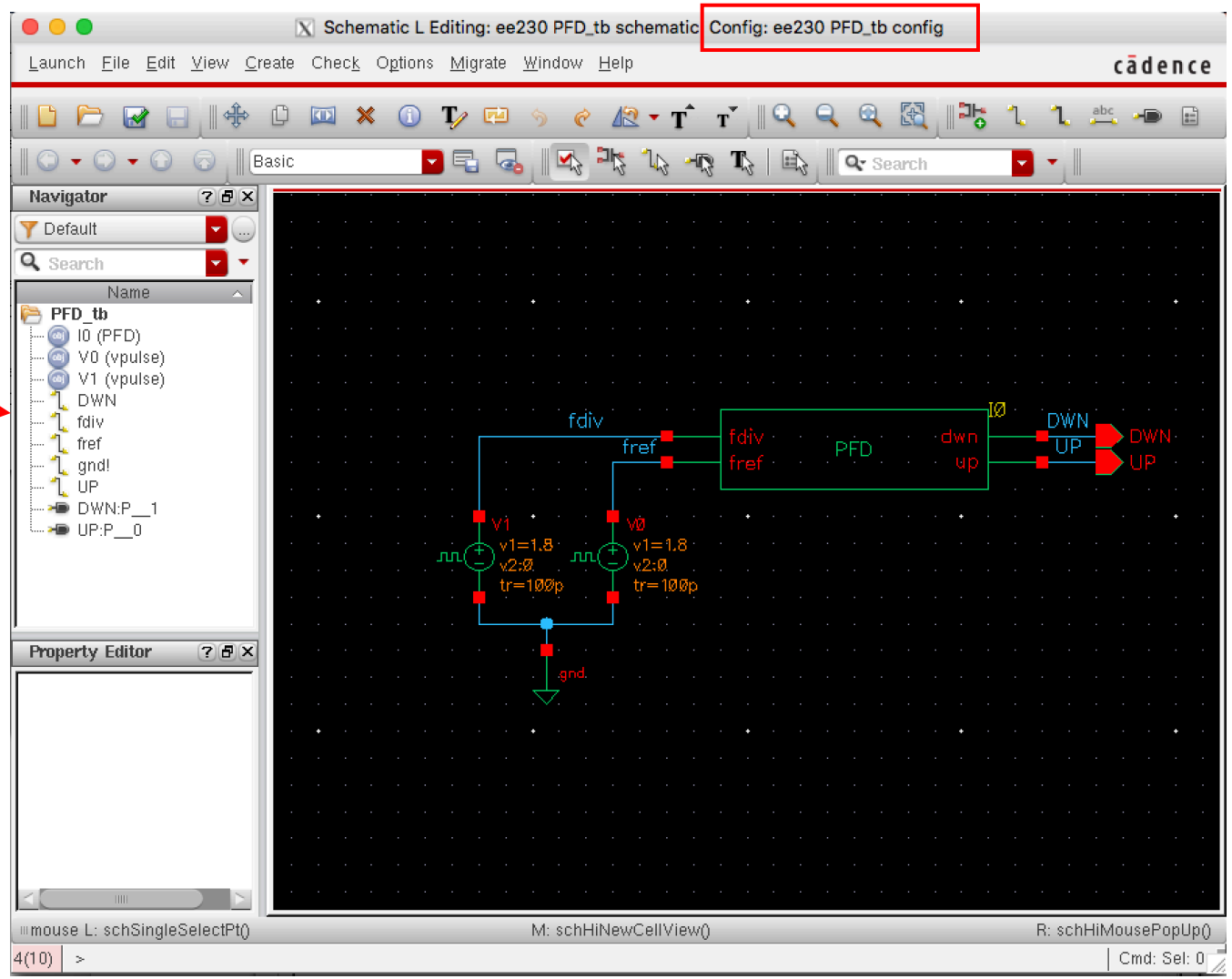






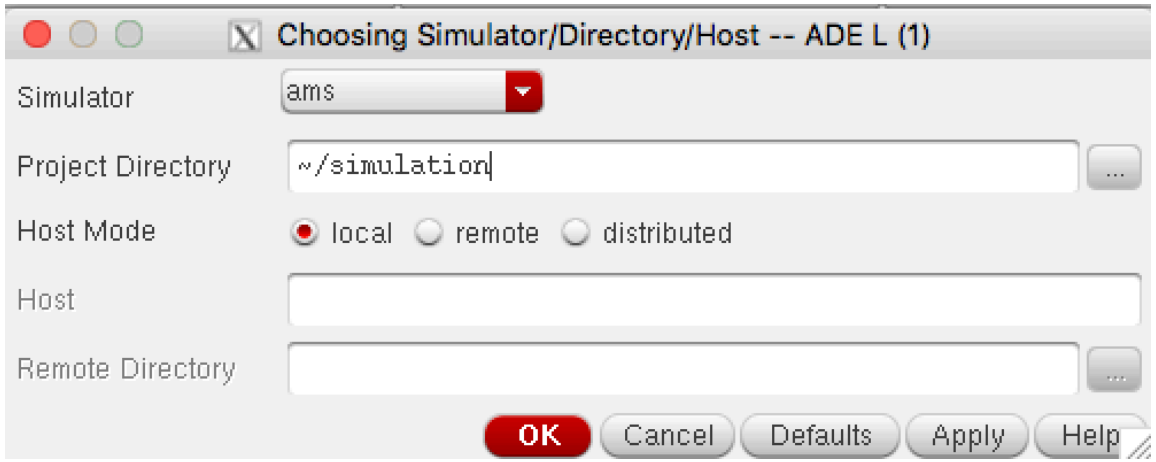
Create Config File





ADE Setup

- Open ADE L from config schematic
- From ADE L window: Setup -> Simulator/Directory/Host…



ADE Simulation

- Now able to simulate the Verilog-AMS block