A 1.92 GHz Charge Pump PLL using 45nm CMOS Technology

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***Abstract*—This paper proposes the design of a low-power frequency synthesizer PLL system that produces a 1.92 GHz signal with a reference input of 30 MHz. A standard PLL topology is used, with a comparison between using an LC VCO and using a Ring VCO.**

***Index Terms* — Phase Lock Loop, Voltage-Controlled Oscillator, Frequency Synthesizer, Divider.**

I. Introduction

The work provided in this paper analyzes the differences between the standard PLL topology with a ring oscillator versus that with an LC oscillator. System level simulations and extreme corner simulations are provided to verify the performance on the preferred version.

II. System Overview

The proposed PLL is a 2nd order Charge-Pump PLL system that produces a 1.92 GHz output signal. As shown in Fig. 1, the PLL is a closed-loop system with a divider of N=64 to ensure a desired output frequency of 1.92 GHz from the VCO while using a reference signal of 30 MHz.

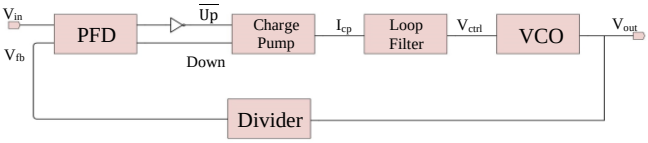


Fig. 1. PLL system block diagram

III. Phase Frequency Detector (PFD)

A. Circuit

The first block of the PLL system is the PFD, shown in Fig. 2. Its main function is to compare the phase and the frequency of the reference and the feedback signal coming from the divider, producing an "Up" or a "Down" signal depending on if the reference signal is leading or lagging. Since the PFD deals with relatively low frequencies, all the gates used in it are built using static CMOS logic.

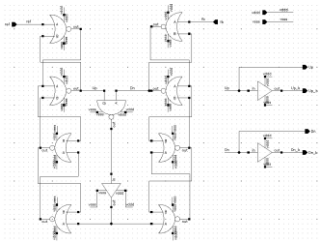


Fig. 2. Schematic of the PFD circuit

IV. Charge Pump (CP) & Loop Filter (LF)

A. Circuit

The CP receives the "Up" or "Down" signal from the PFD and charges or discharges the loop filter accordingly. An "Up" signal causes the upper switch to switch on, causing the upper current source to charge the LF. If a "Down" signal is high, the bottom switch turns on allowing the bottom current source to discharge the LF. The LF is a low-pass filter that serves the purpose of averaging out the phase-error signal generated from the PFD and generating a control voltage (V_{ctrl}) for the VCO.

Fig. 3 shows the proposed bootstrapped CP with the LF, where the lower switch and source are implemented using NMOS transistors, and the upper switch and source are implemented using PMOS. The CP opamp uses a typical single stage differential amplifier topology.

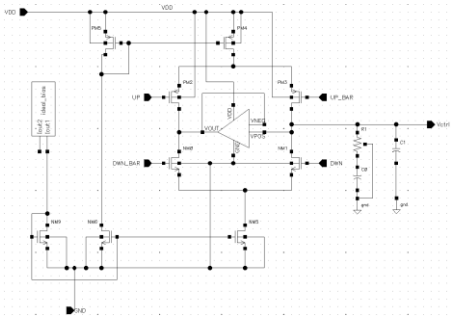


Fig. 3. Schematic of the Bootstrapped Charge Pump and the Loop Filter

B. Simulations

The differential opamp is connected in unity gain to provide equal voltage on either end of the current branches. Because the PM of the opamp is > 60 degrees and the GM is > 12dB, the opamp will avoid oscillation.

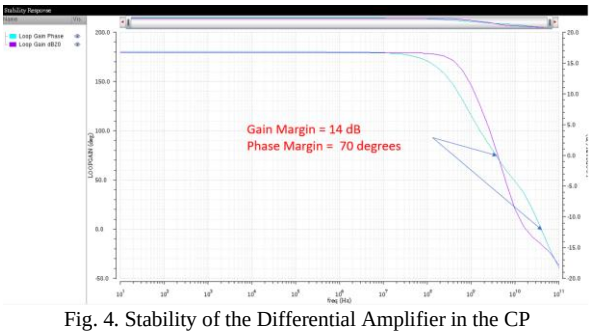
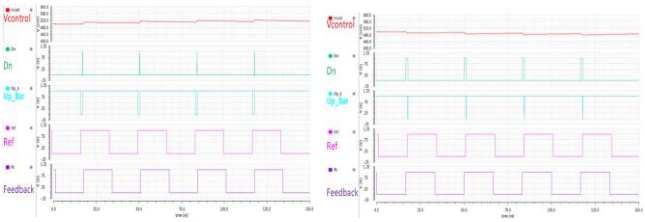


Fig. 4. Stability of the Differential Amplifier in the CP

The PFD, the CP, and the LF are connected and simulated together. Fig. 5 shows that when the reference signal leads the feedback signal, the "Up" switch turns on, increasing the control voltage, telling the oscillator to speed up. The opposite is true when the reference signal is lagging.



(a) (b)

Fig. 5. Output Waveforms when the reference signal (a) leads (b) lags

V. Voltage-Controlled Oscillator (VCO)

A. Ring VCO Circuit

There are two VCO topologies under investigation in this study. The first topology is a current-starved ring VCO, shown in Fig. 6. A 7-stage ring oscillator is used to improve V_{ctrl}'s tuning range and additional inter-stage capacitors are added to slow the VCO down. The V_{ctrl} is applied as a gate voltage to the lower NMOS transistors in each stage to control the charging or the discharging currents, controlling the delays and thus controlling the output frequency.

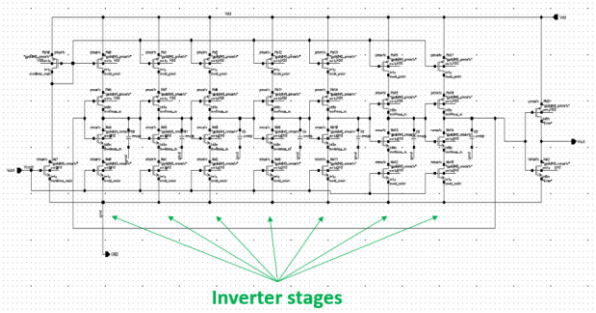


Fig. 6. Schematic of the current-starved ring VCO

B. LC VCO Circuit

The second oscillator topology used is an LC VCO, as shown in Fig. 7. Here, V_{ctrl} tunes the varactor to resonate with the inductors. NMOS transistors are used to build the varactors to get an increasing output frequency as V_{ctrl} increases. The cross-coupled transistors were designed to provide a negative resistance that cancels with the inductor's resistance.

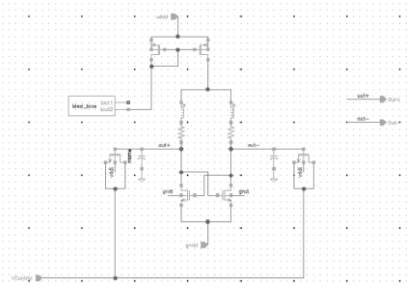


Fig. 7. Schematic of the LC VCO

C. Simulations

Both VCOs are designed to give a 1.9 GHz output at V_{ctrl} = 0.5v. Fig. 8 shows the ring VCO's output waveform and its frequency at V_{ctrl} = 0.5v. Sweeping the V_{ctrl} value from 0 to V_{DD}, it is shown in Fig. 9 that the wide tuning range of the ring oscillator results in a K_{VCO} of 9.65 GHz/V, and in Fig. 10, the phase noise is seen to be -85dBc/Hz at a 0.5v V_{ctrl}.

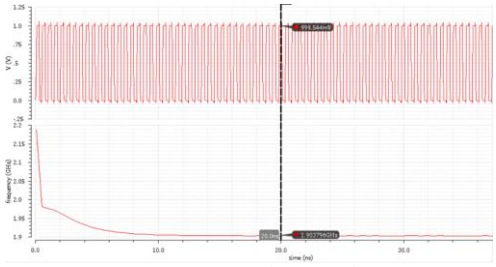


Fig. 8. Ring Oscillator - Output waveform and frequency at V_{ctrl} = 0.5v

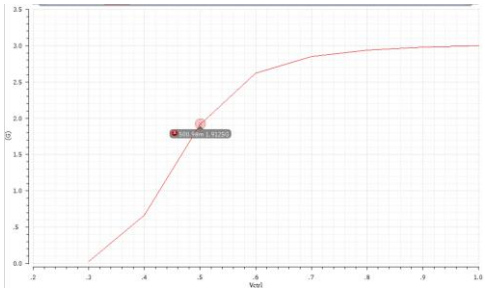


Fig. 9. Ring Oscillator - Oscillation frequency vs V_{ctrl}

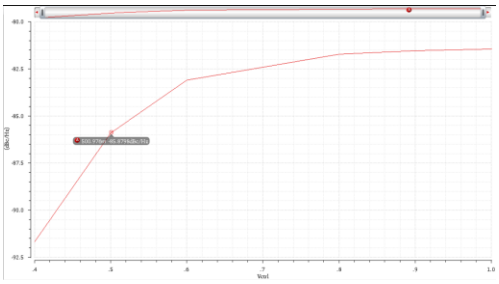


Fig. 10. Ring Oscillator – Phase Noise vs V_{ctrl}

In the case of the LC VCO, the output waveform (seen in Fig. 11) takes a longer time to turn on and does not give a rail-to-rail square output as in the ring VCO. Fig. 12 and Fig. 13 show the output frequency and the phase noise against V_{ctrl}, respectively. The LC VCO has a much tighter tuning range with a K_{VCO} of 600MHz/V, but a better phase noise performance of -113dBc/Hz at a 0.5v V_{ctrl}.

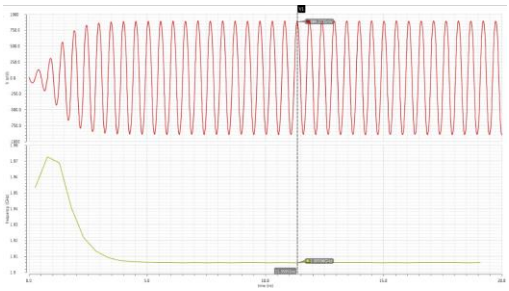


Fig. 11. LC Oscillator - Output waveform and frequency of at V_{ctrl} = 0.5v

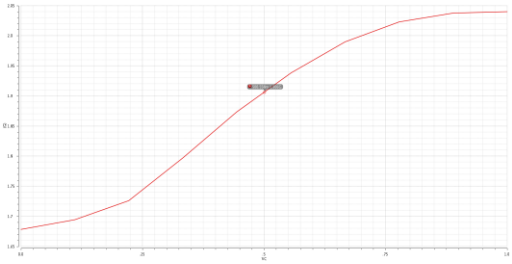


Fig. 12. LC Oscillator - Oscillation frequency vs V_{ctrl}

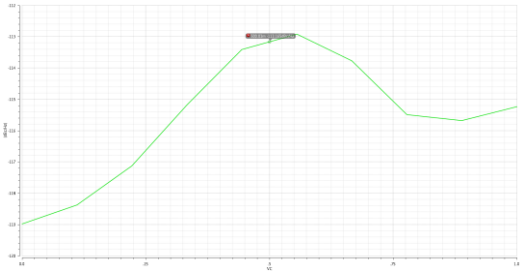


Fig. 13. LC Oscillator – Phase Noise vs V_{ctrl}

VI. Divider

With a reference signal of 30MHz and the output of the VCO being 1.9GHz, a divider of multiple 64 is needed. The divider consists of 6 divide-by-2 stages. The first two are true-single-phase-clock (TSPC) flipflops, since they operate at relatively high frequencies, and the remaining four are static CMOS flipflops.

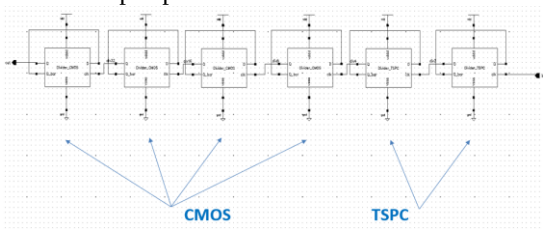
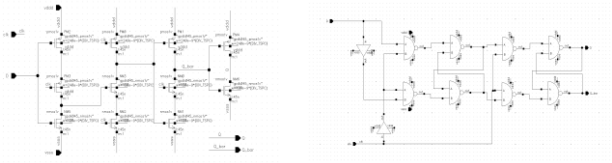


Fig. 14. Divide-by-64 Top Level Circuit



(a) (b)

Fig. 15. Flipflops (a) TSPC (b) Static CMOS

VII. System Simulations

A. Transient & Jitter Simulations

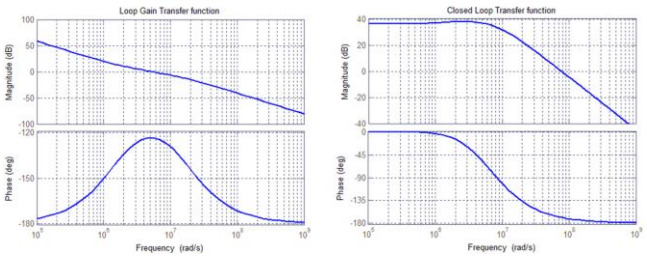
Table I shows the circuit parameters chosen based on the system's stability. From the open-loop and the closed-loop transfer functions, given by equations (1) and (2), and their bode plots in Fig. 16, a phase margin of 56.36^{O} and a closed-loop bandwidth of 1.4 MHz are achieved.

$$H_{OL}(s) = \frac{I_{cp}\,K_{VCO}}{2\pi N}\,\frac{s\,R_1C_1 + 1}{s^2(s\,R_1C_1C_2 + (C_1 + C_2))} \quad (1)$$

$$H_{CL}(s) = \frac{I_{cp}\,K_{VCO}}{2\pi}\,\frac{s\,R_1C_1 + 1}{s^3R_1C_1C_2 + s^2(C_1 + C_2) + s\,R_1C_1\frac{I_{cp}\,K_{VCO}}{2\pi N} + \frac{I_{cp}\,K_{VCO}}{2\pi N}} \quad (2)$$

TABLE I. Circuit Parameters Used

Parameter		Value
Supply Voltage	V_{DD}	1 v
Reference frequency	f_{ref}	30 MHz
Output frequency	f_{out}	1.92 GHz
Divider	N	64
CP Current	I_{CP}	100 uA
VCO Gain	K_{VCO}	600 MHz/V
Loop Filter Components	R_P	6.5 KΩ
	C_P	100 pF
	C_2	10 pF



(a) (b)

Fig. 16. (a) Open-loop response. (b) Closed-loop response.

Using the testbench in Fig. 17, the whole PLL system was simulated using the 2 different VCOs. From the transient simulations, both the lock time and the power dissipation are obtained, while the RMS and the peak-to-peak jitters are calculated from the pss and pnoise analyses. Both jitters were integrated within 1KHz and 1GHz offset range. Table II shows a comparison in performance between the PLL using the ring VCO and the PLL with the LC VCO.

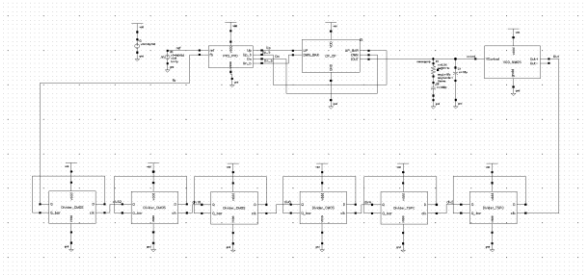


Fig. 17. Testbench for the whole PLL system

TABLE II. Performance Comparison Between PLL with LC VCO & PLL with Ring VCO

Parameter	LCVCO	Current Starved Ring VCO
VCO Gain (K_{VCO})	600 MHz/v	9.65 GHz/v
Tuning Range	1.68 GHz – 2.02 GHz	0.5 GHz – 3 GHz
Locking Time	~ 2 us	~ 1.5 us
P Dissipation	1.26175 mW	1.21701 mW
RMS Jitter	1.5421 ps	18.9632 ps
FOM	**-235.23 dB**	**-213.43dB**

Using the figure-of-merit (FOM) defined by equation (3), it is clear that the LC VCO achieves a much better performance than the ring VCO in terms of RMS jitter (at similar power dissipation) due to its small K_{VCO}. Also, using the LC VCO results in less ringing in V_{ctrl}, as seen in Fig. 18. Yet, the ring VCO offers a large tuning range and takes a shorter time to reach the lock state (Fig. 20).

$$FOM = 10\,log\left(Jitter^2.\ \frac{Power}{1\,mW}\right) \qquad (3)$$

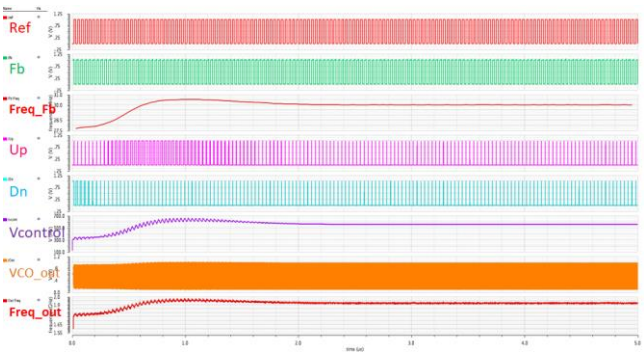
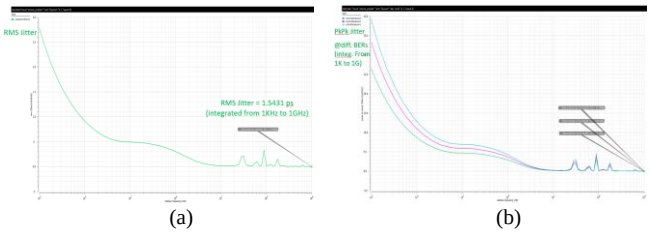


Fig. 18. Transient Simulation Results for PLL with LCVCO



(a) (b)

Fig. 19. Jitter Simulation for PLL with LCVCO
(a) RMS Jitter (b) Pk-to-Pk Jitter at different BERs

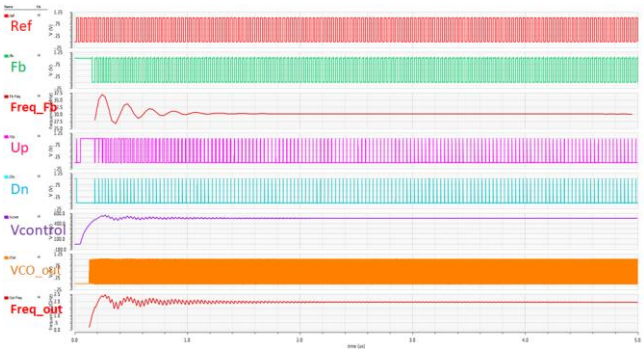
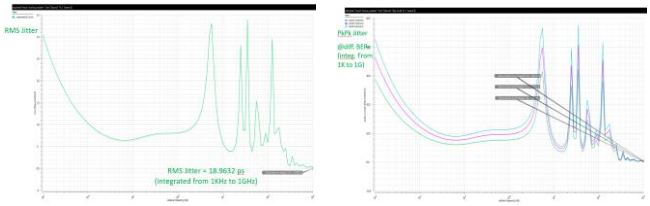


Fig. 20. Transient Simulation Results for PLL with Ring Oscillator



(a) (b)

Fig. 21. Jitter Simulation for PLL with Ring VCO
(a) RMS Jitter (b) Pk-to-Pk Jitter at different BERs

B. Corner Simulations

Because of the preferred jitter results that the LC VCO PLL circuit provides, this topology is used for the extreme corner simulations. As shown by Fig. 22, corner simulations show a VCO output frequency range from 1.916GHz – 1.946 GHz and a feedback frequency range from 29.95MHz – 30.16MHz

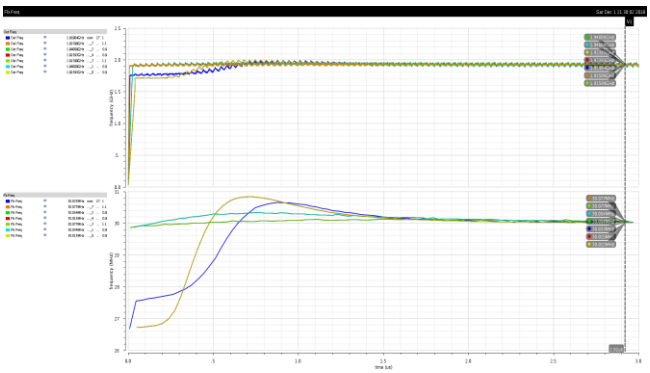


Fig. 22. Corner Simulation Results for PLL with LC VCO

VIII. CONCLUSION

The design of a 1.92 GHz 2nd order Charge-Pump PLL using CMOS 45nm technology at 1V is presented, along with a comparison between using an LC VCO and using a Ring VCO. The LC VCO showed a better jitter and power performance, while with the ring VCO, a larger tuning range and a shorter lock time were achieved. Using the LC VCO, measured RMS jitter integrated over a range of 1KHz to 1GHz offset is 1.5421 ps while consuming 1.26175mW, resulting in an FOM of **-235.23 dB**.

Many improvements can still be applied to the design, like reducing power consumption by investigating other LC VCO and charge pump topologies. Also, using synchronous counters and CML flipflops in the divider can help reduce the accumulated jitter in the divider path.

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