EE230 – Final Project

1.9 GHz CP PLL Design

(using 45nm CMOS Technology)

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Overview

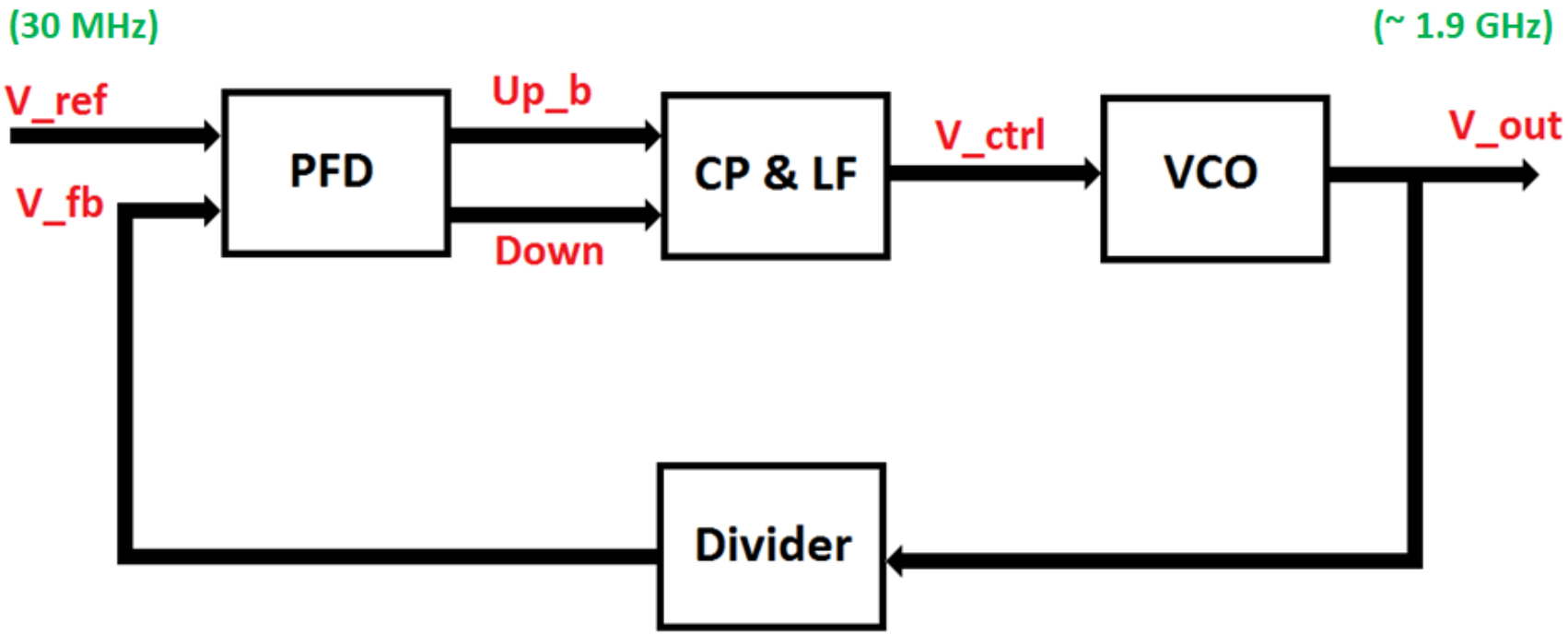
1) Project Target
2) Matlab Simulations
3) VerilogA Simulations
4) PLL Circuits
    a. PFD
    b. Charge Pump
    c. Loop Filter
    d. VCO
        i. LC tank
        ii. Current-Starved Ring
    e. Divider
5) System Simulations
6) Corner Simulations
7) Summary

(1)
Project Target

Target

$$FOM = 10\log\left(Jitter^2.\frac{Power}{1\,mW}\right) \qquad < -220\,dB$$

PLL Block Diagram

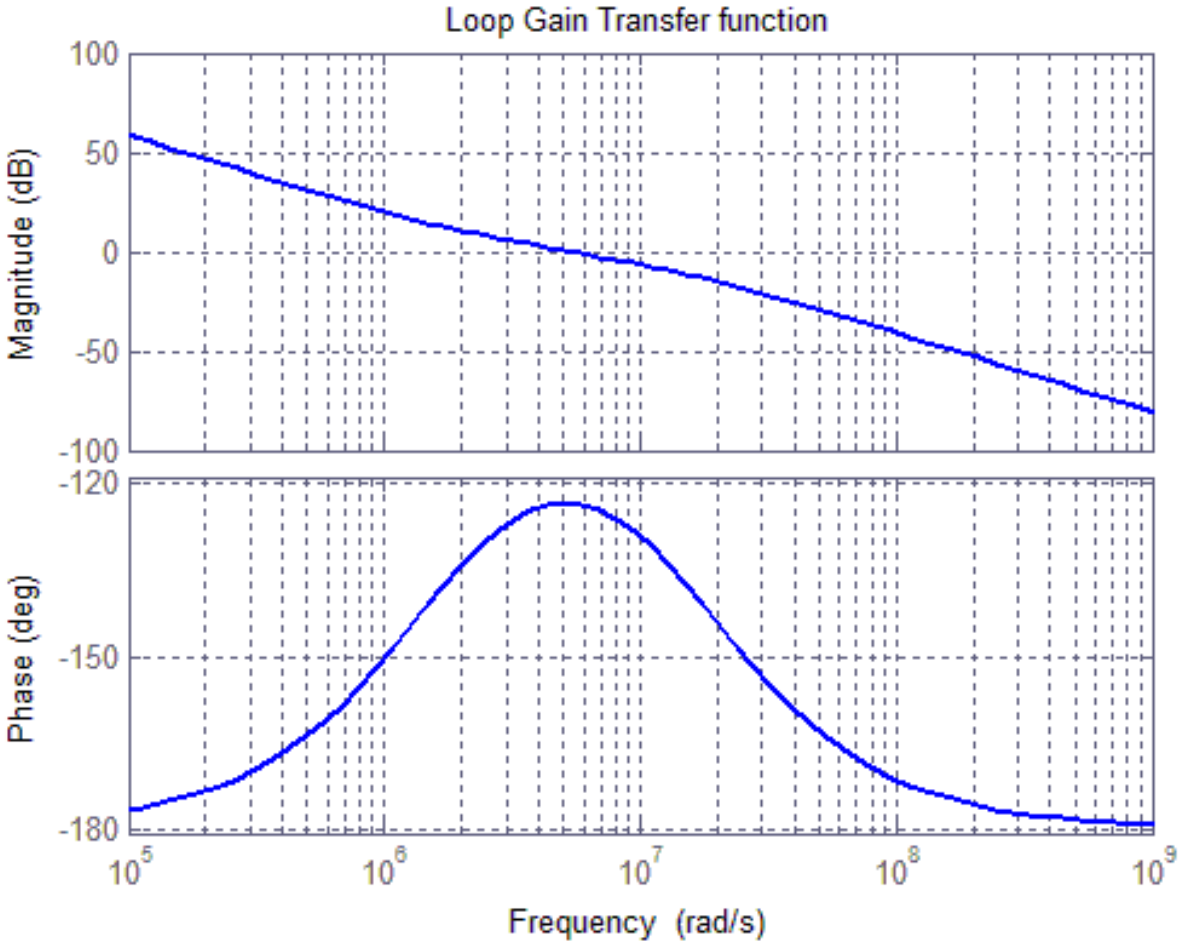


(2)
Matlab Simulations

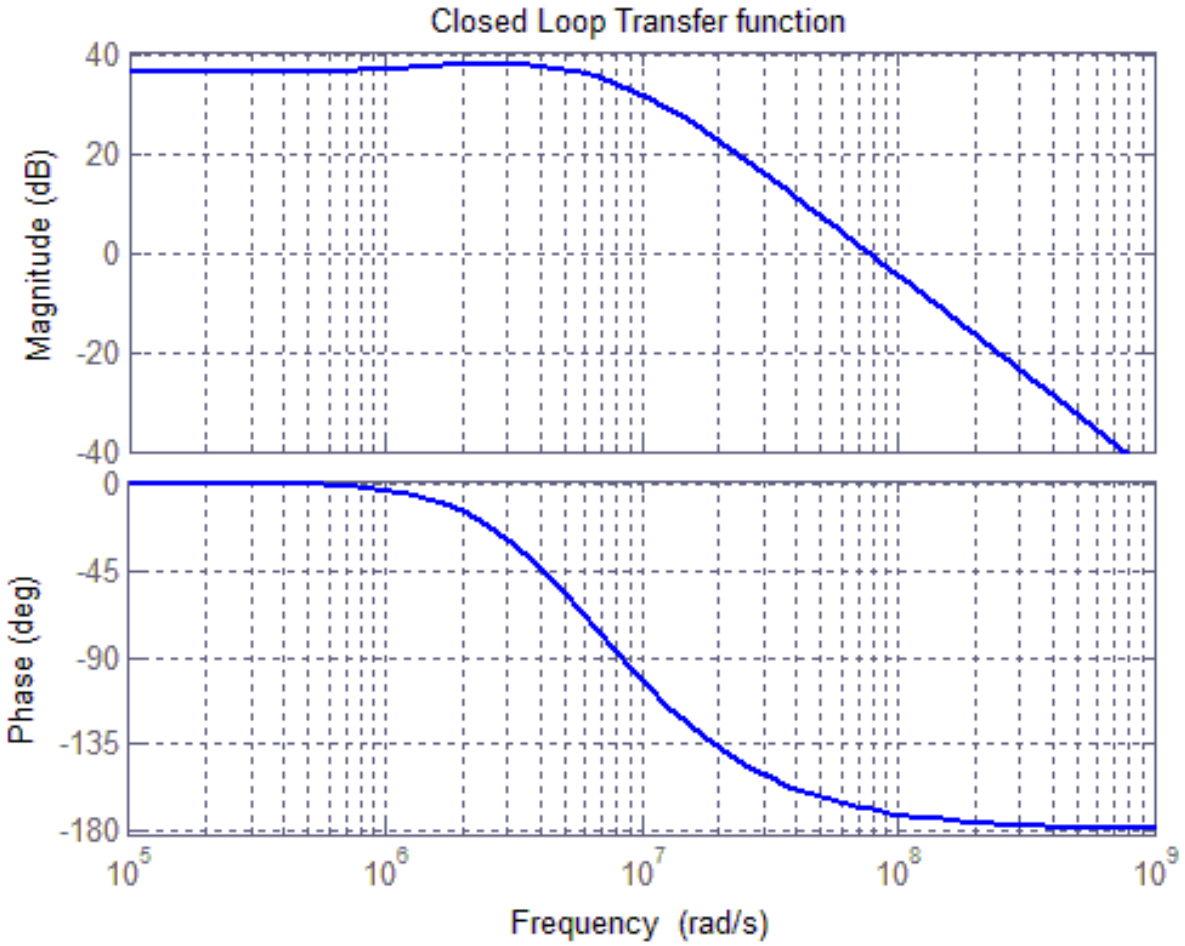
System Parameters

Parameter	Value
F_{REF}	30 MHz
F_{OUT}	1.9 GHz
$M_{Divider}$	64
I_{CP}	100 uA
K_{VCO}	600 MHz/V
R_P	6.5 KΩ
C_P	100 fF
C_2	10 fF

Open-Loop Bode Plots



Closed-Loop Bode Plots

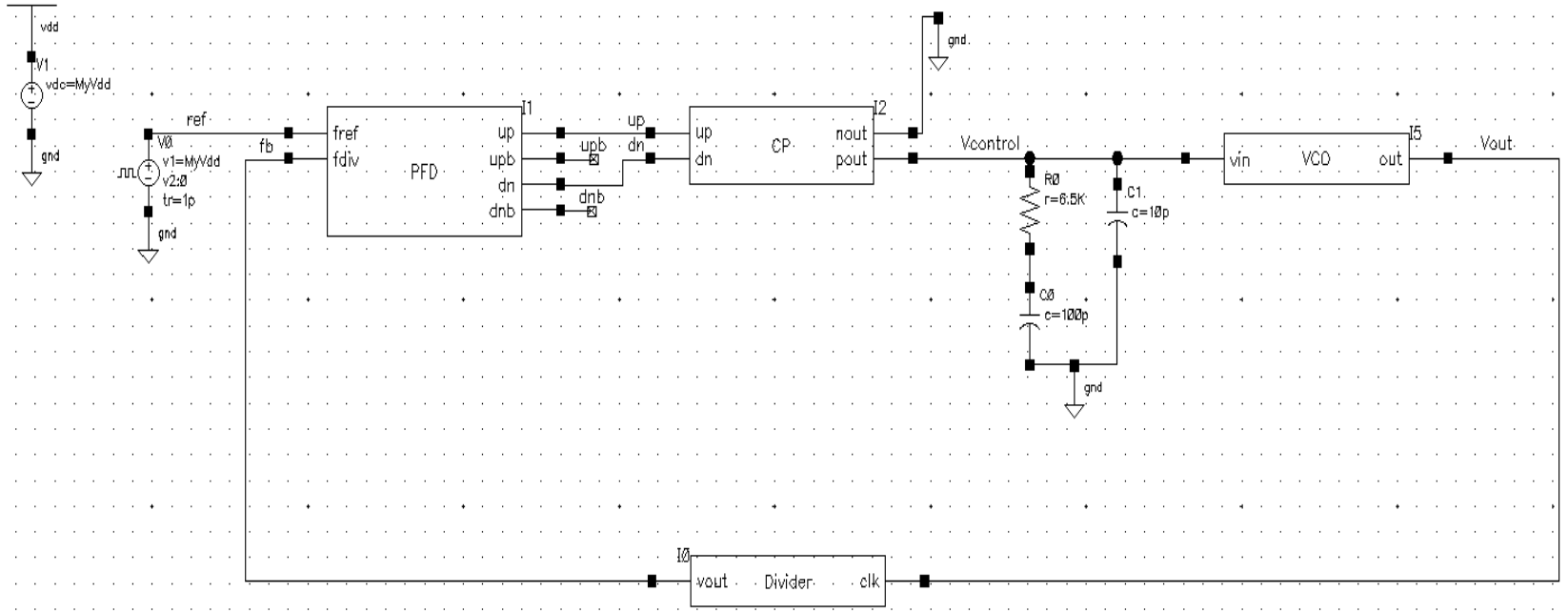


Bode Plot Parameters

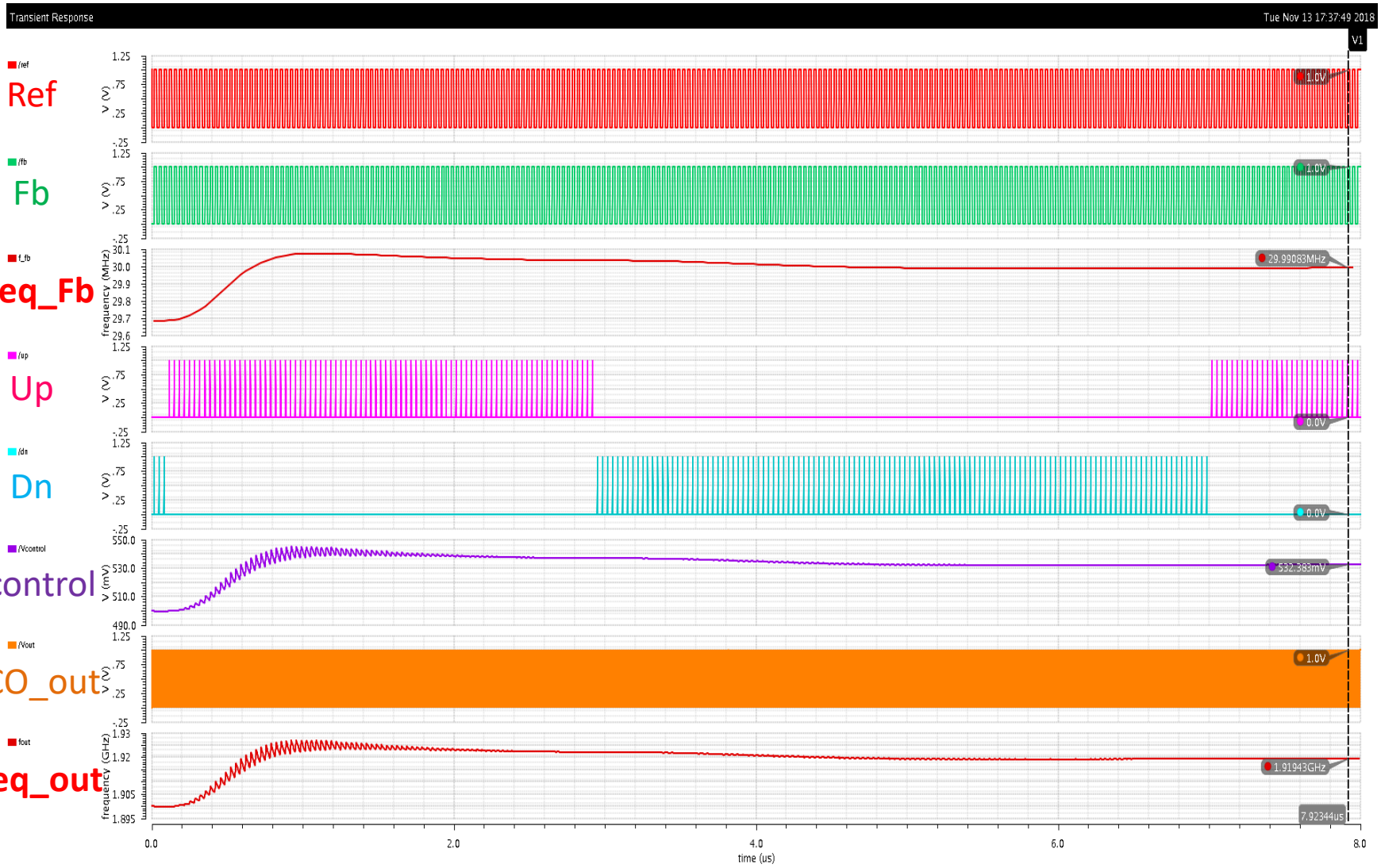
Parameter		Value
Zero	f_z	0.245 MHz
Unity-Gain BW	f_{ugb}	0.871 MHz
Pole	f_{p3}	2.693 MHz
Max Phase Margin	PM_{Max}	56.44°
Phase Margin	PM	56.38°
Closed-Loop BW	BW	1.41 MHz

(3)
VerilogA Simulations

Test Bench

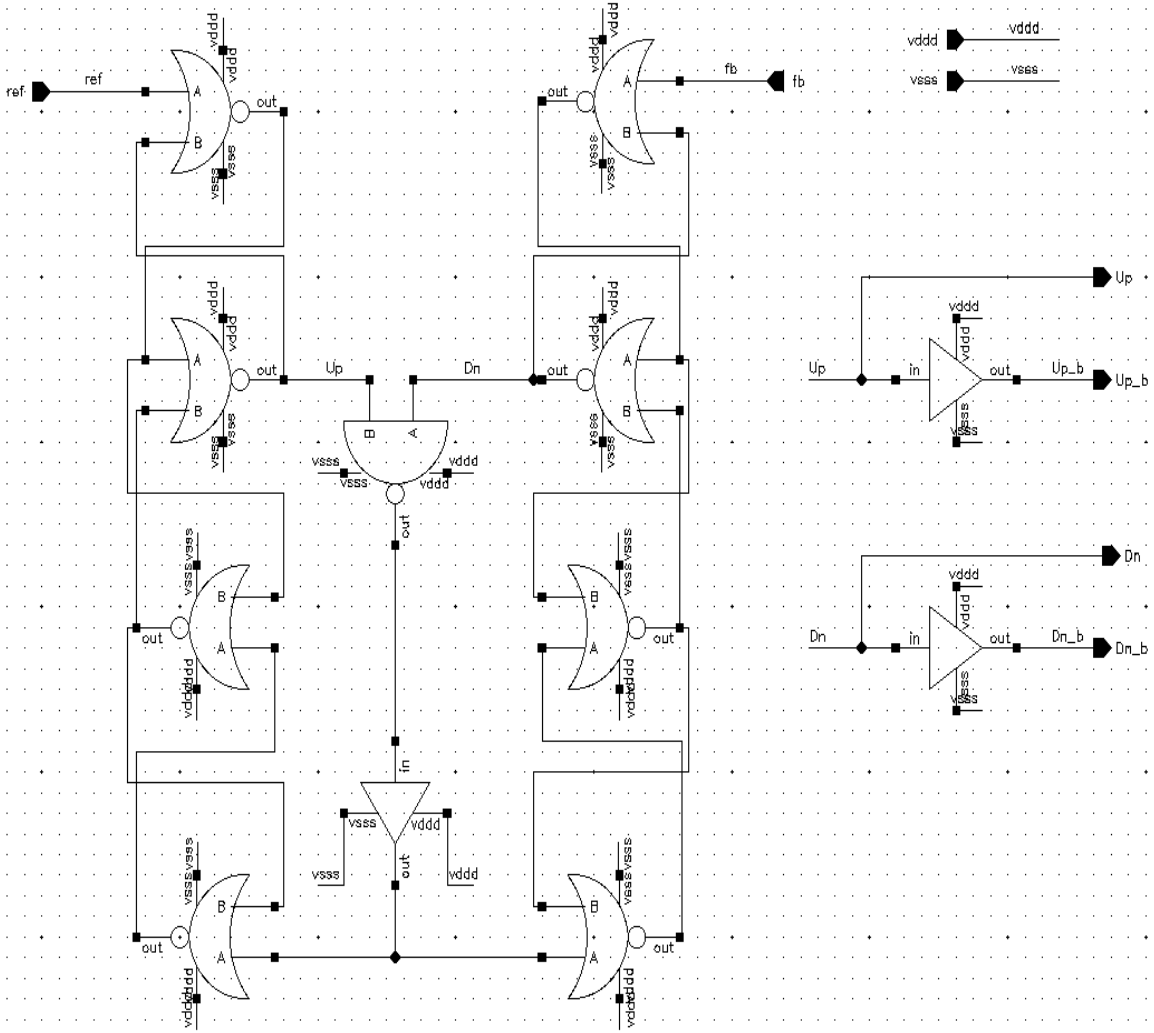

vdd
V1
vdc=MyVdd
gnd
ref
V0
v1=MyVdd
v2:0
tr=1p
gnd
fb
fref
fdiv
PFD
I1
up
upb
dn
dnb
upb
dnb
up
dn
up
dn
CP
I2
nout
pout
gnd
Vcontrol
R0
r=6.5K
C1
c=10p
C0
c=100p
gnd
vin
VCO
out
I5
Vout
I0
vout
Divider
clk

Waveforms

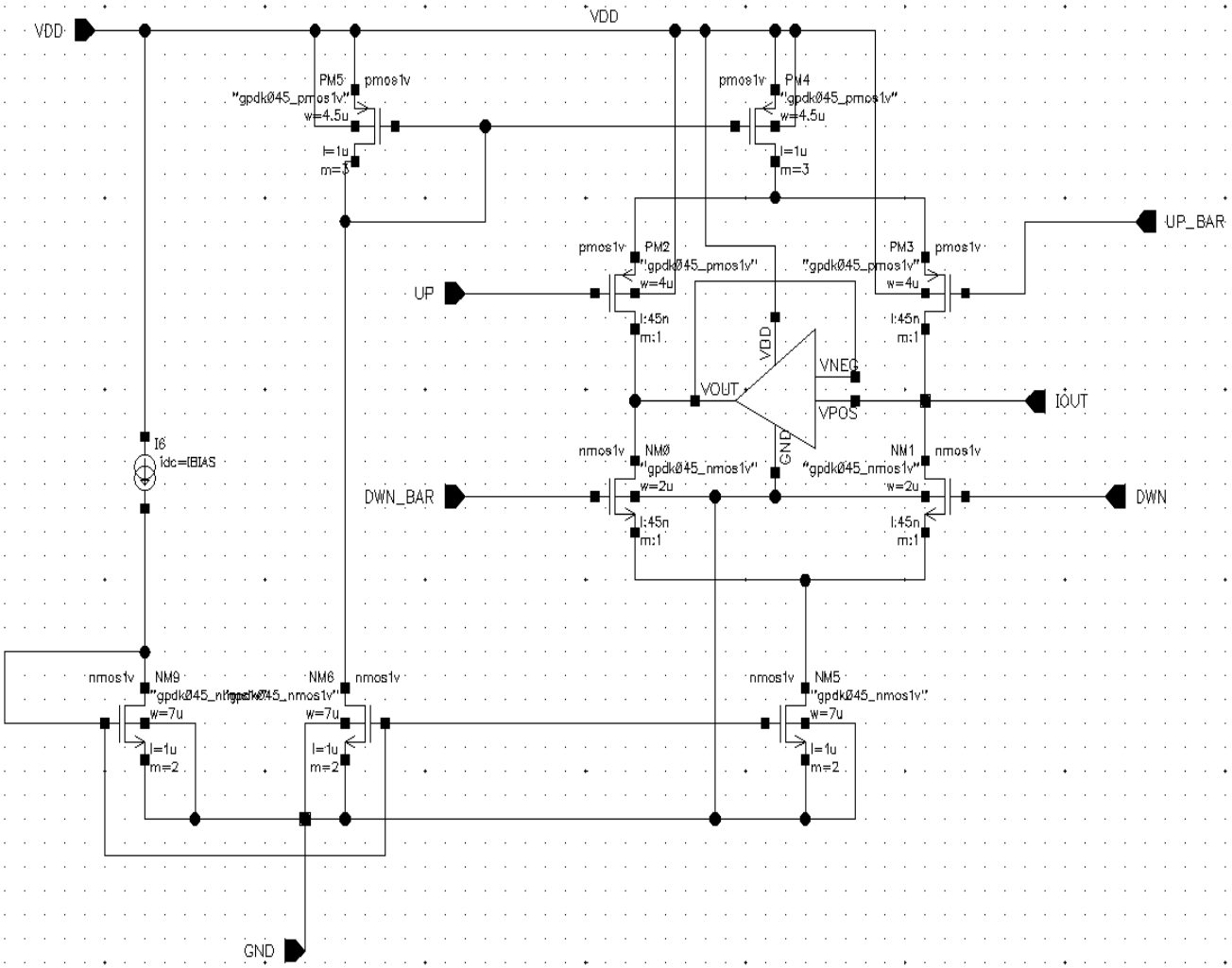

Transient Response
Tue Nov 13 17:37:49 2018
V1
/ref
Ref
/fb
Fb
f_fb
Freq_Fb
/up
Up
/dn
Dn
/Vcontrol
Vcontrol
/Vout
VCO_out
fout
Freq_out
V (V)
frequency (MHz)
V (mV)
frequency (GHz)
1.0V
29.99083MHz
0.0V
532.383mV
1.91943GHz
7.92344us
time (us)
0.0
2.0
4.0
6.0
8.0

(4)
PLL Circuits

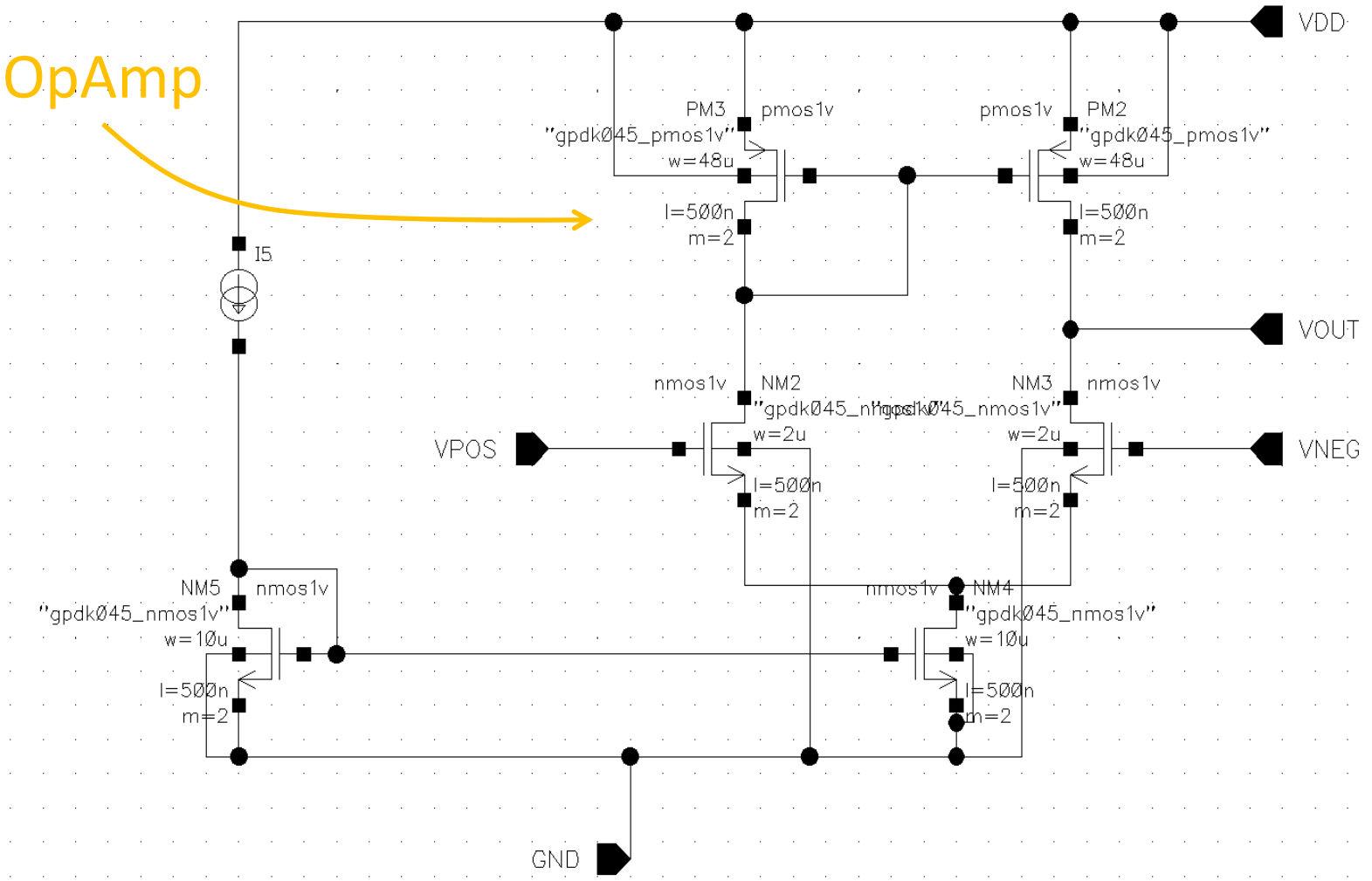
1- PFD



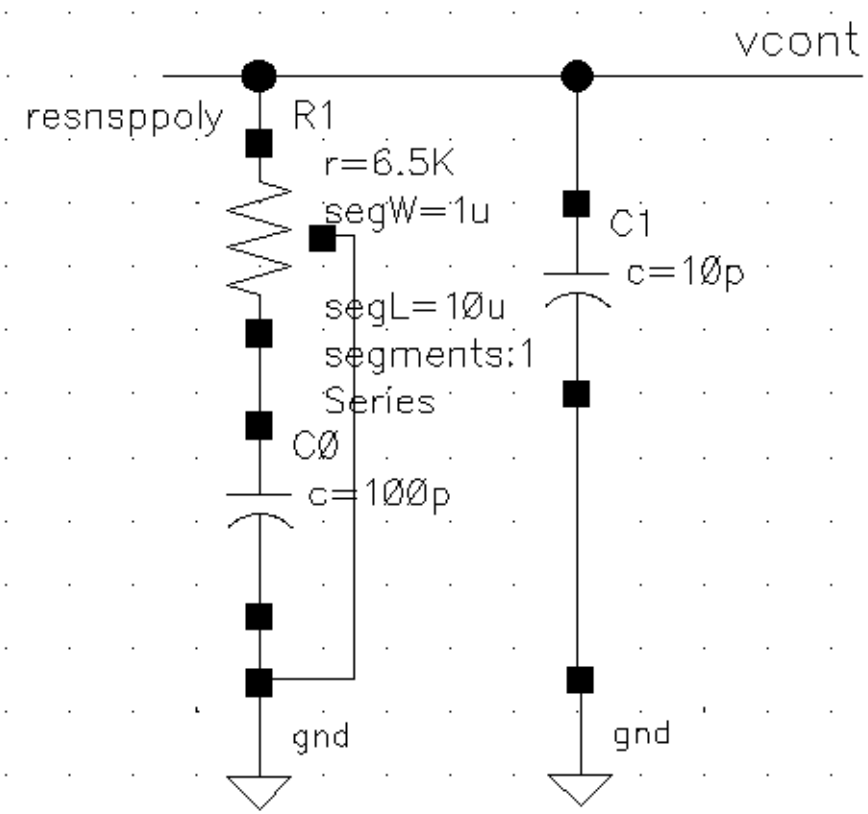
2- Charge Pump



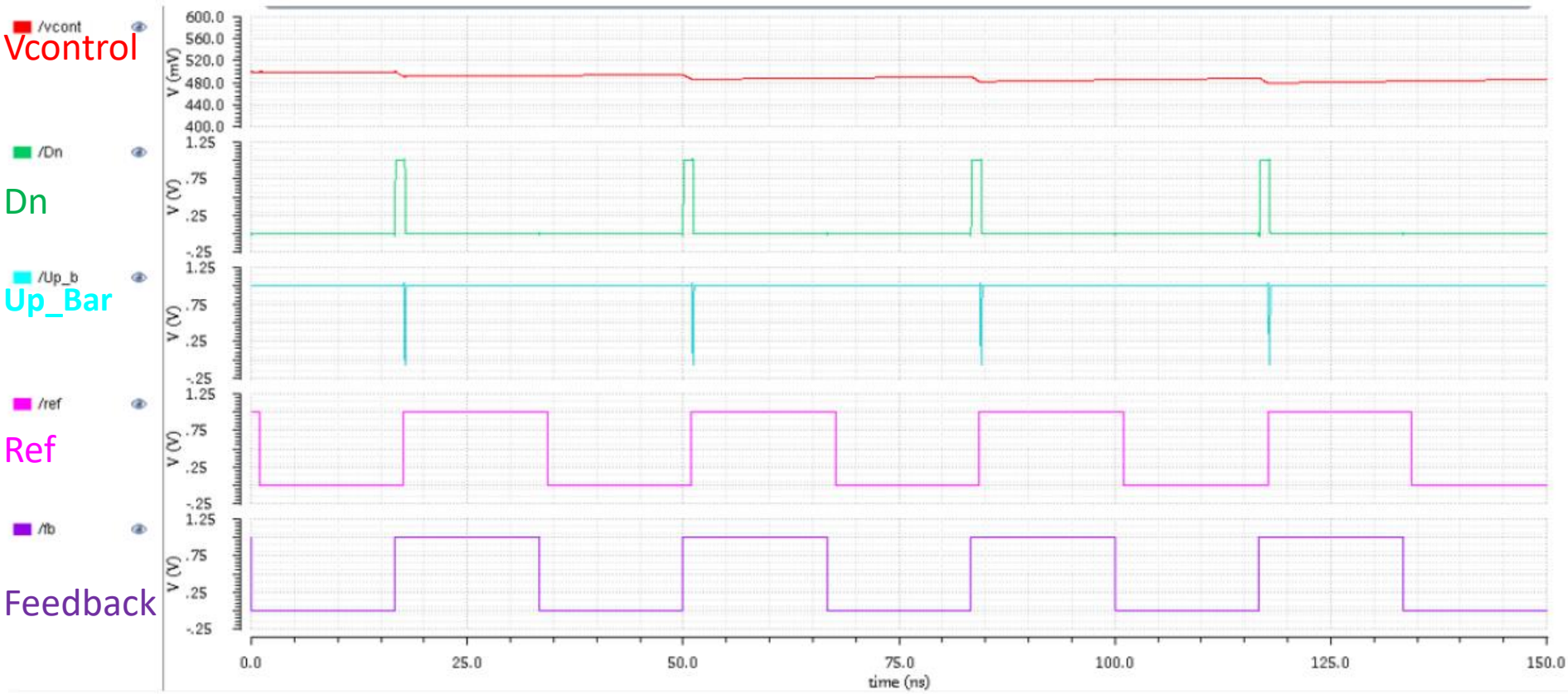
2- Charge Pump



3- Loop Filter

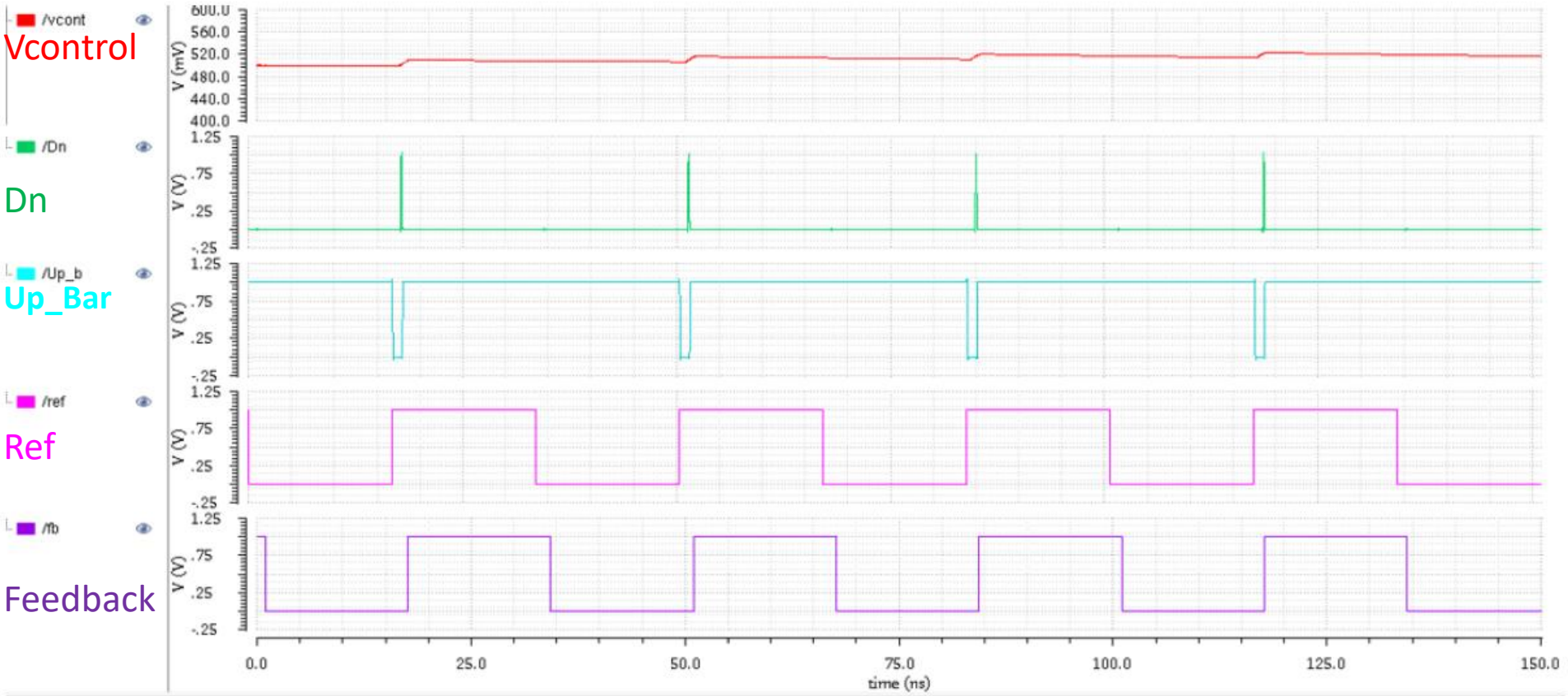


PFD/CP



Reference lagging by 1ns

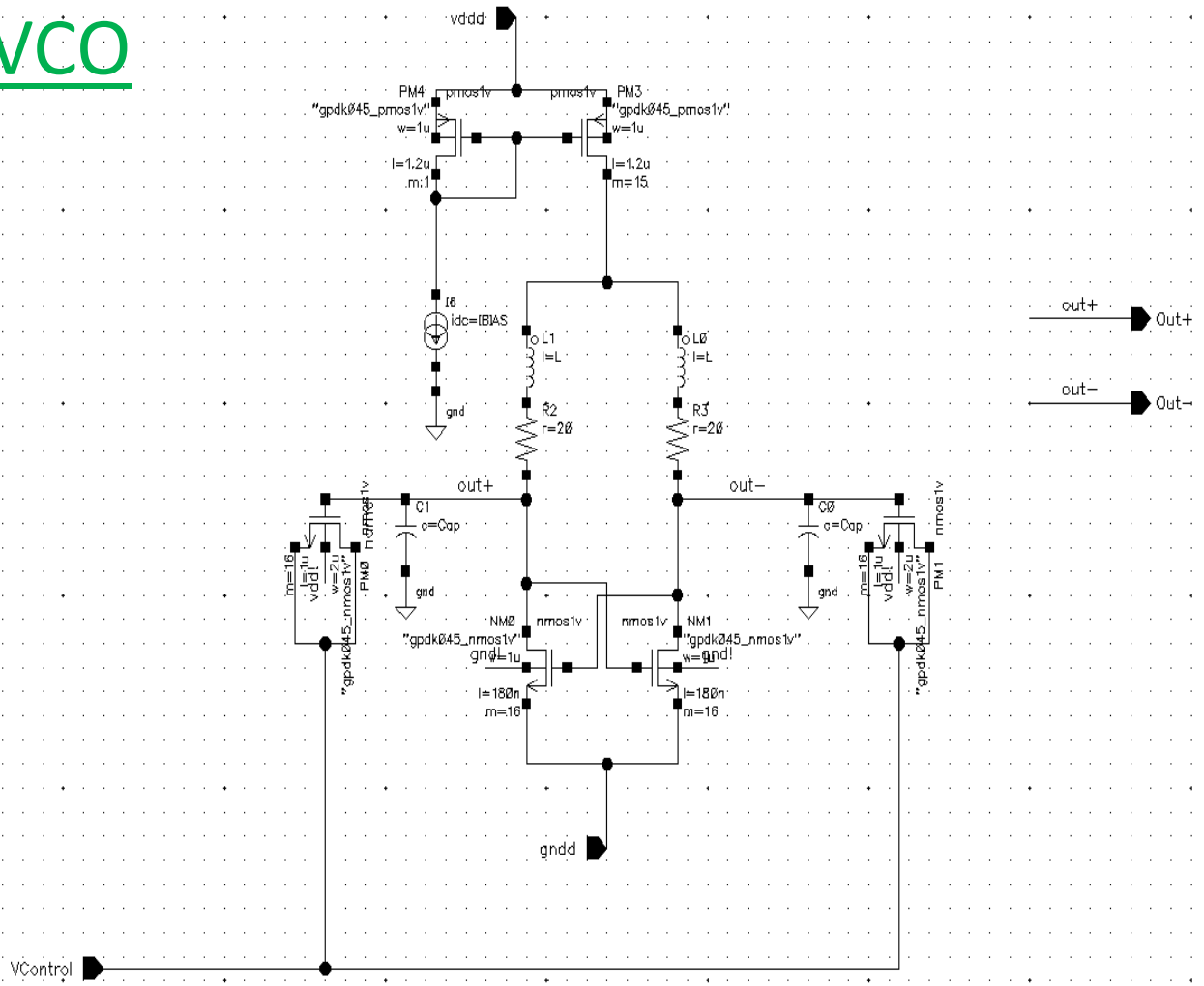
PFD/CP



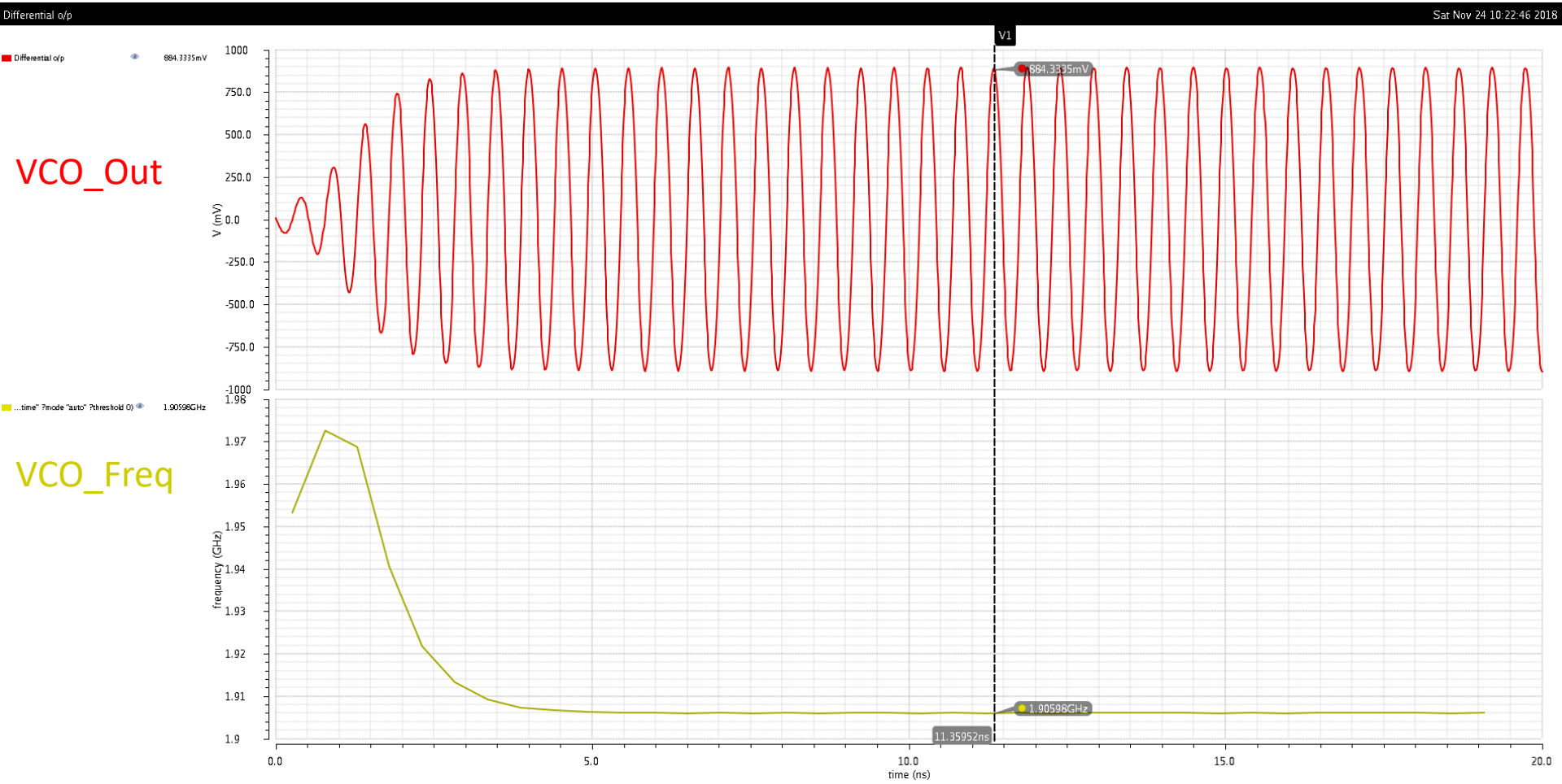
Reference leading by 1ns

4- VCO

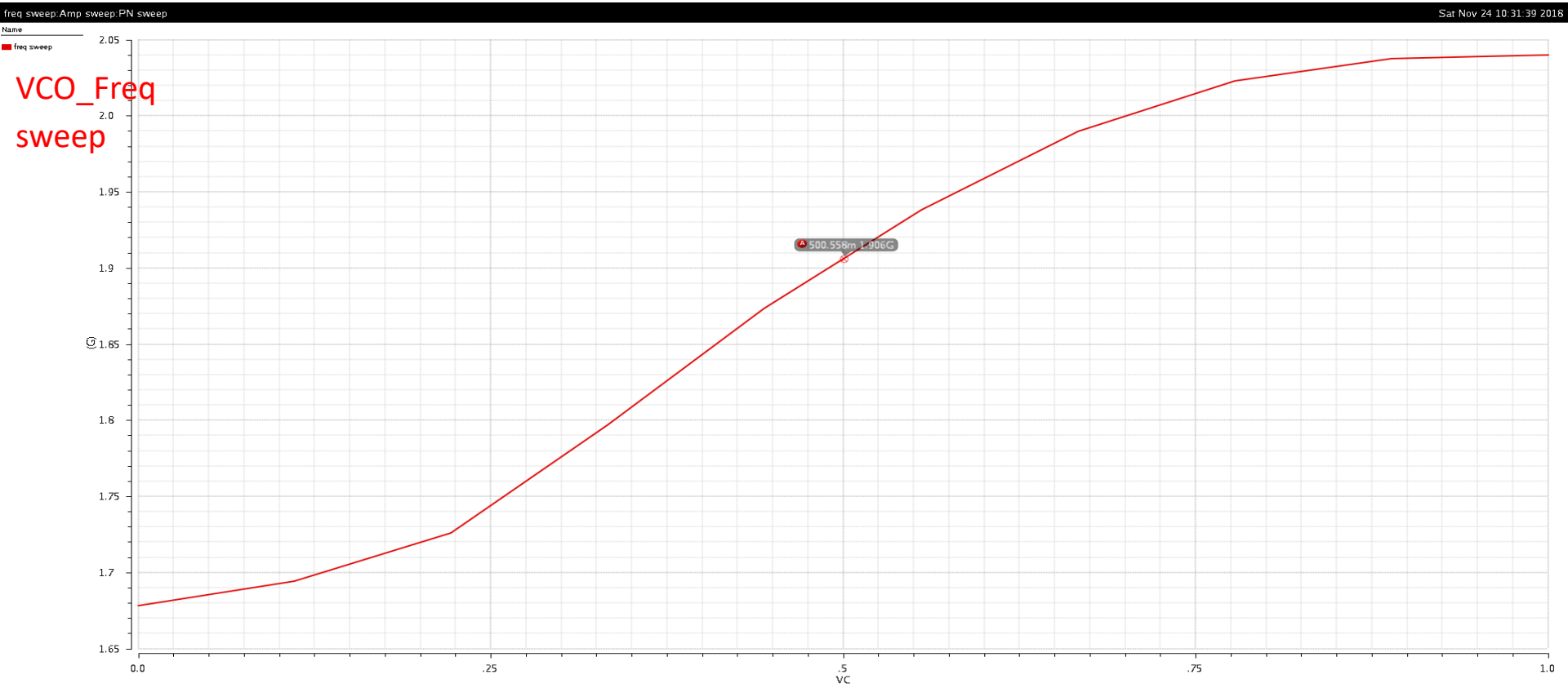
a) LC VCO


vddd
PM4
"gpdk045_pmos1v"
w=1u
l=1.2u
m=1
PM3
"gpdk045_pmos1v"
w=1u
l=1.2u
m=15
I8
idc=IBIAS
gnd
L1
l=L
L0
l=L
R2
r=20
R3
r=20
out+
out-
C1
c=Cap
C0
c=Cap
PM0
"gpdk045_nmos1v"
m=16
l=1u
w=2u
PM1
NM0
"gpdk045_nmos1v"
l=180n
m=16
NM1
"gpdk045_nmos1v"
l=180n
m=16
gndd
VControl
out+
Out+
out-
Out-

LC Oscillator

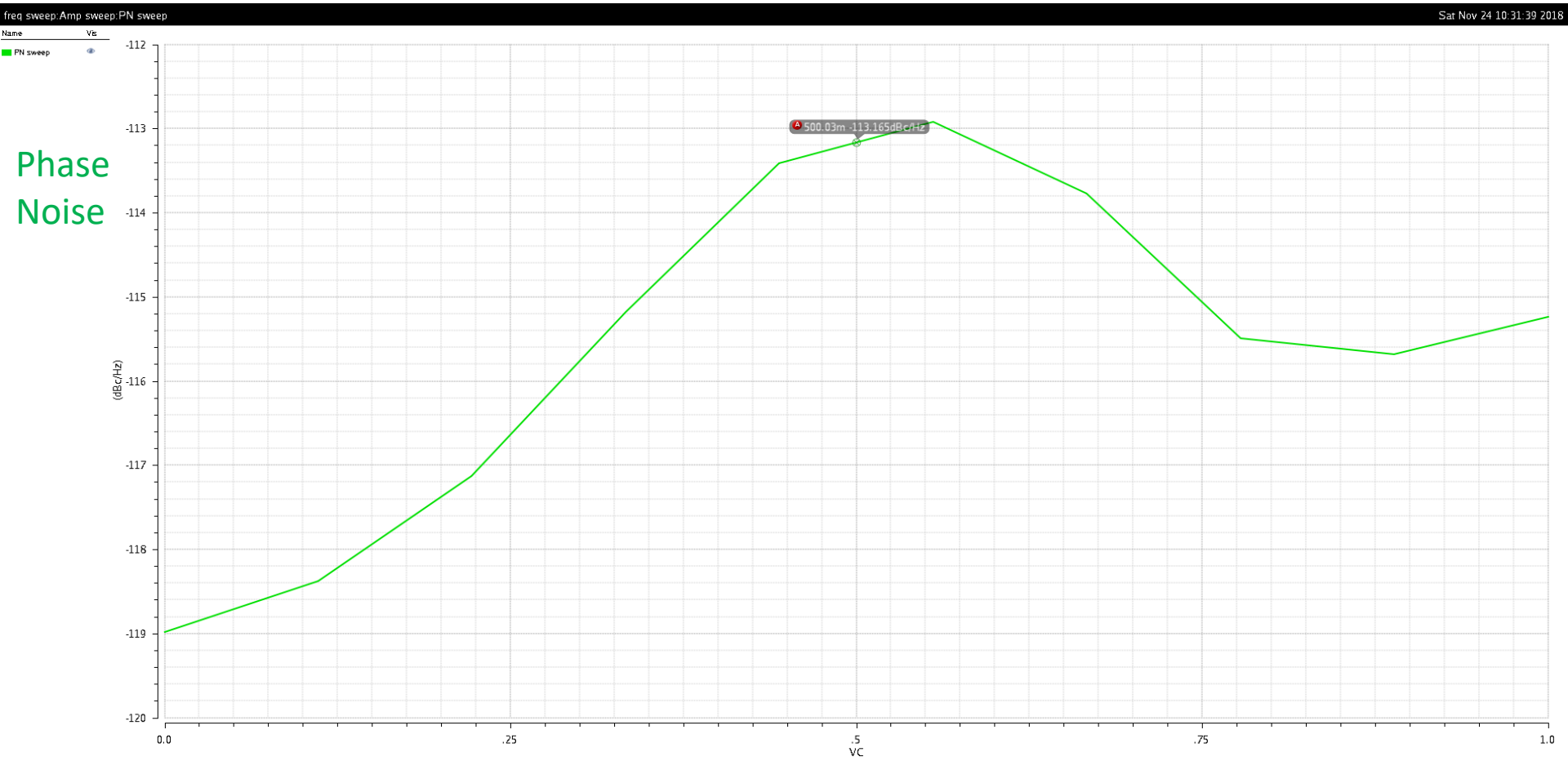


LC Oscillator



Vcontrol Tuning Range

LC Oscillator

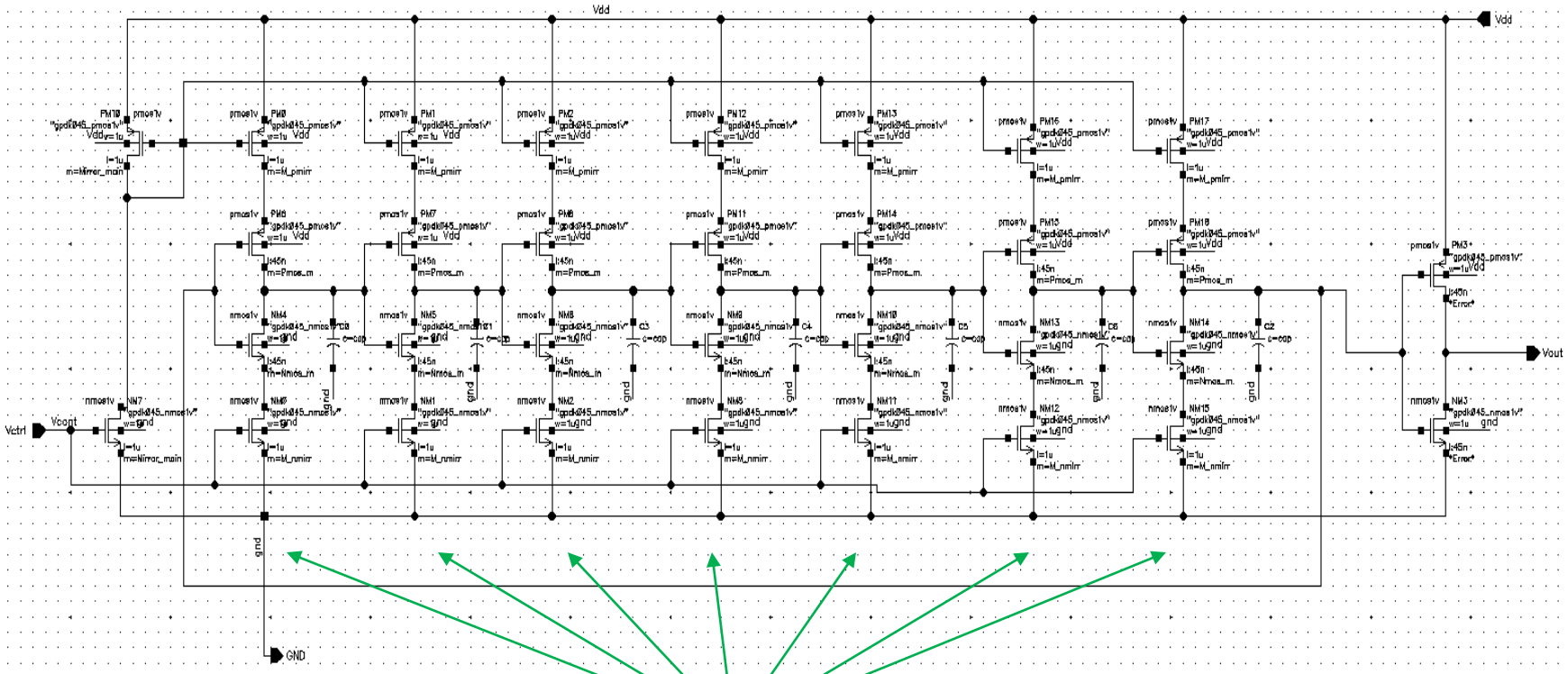


Phase Noise

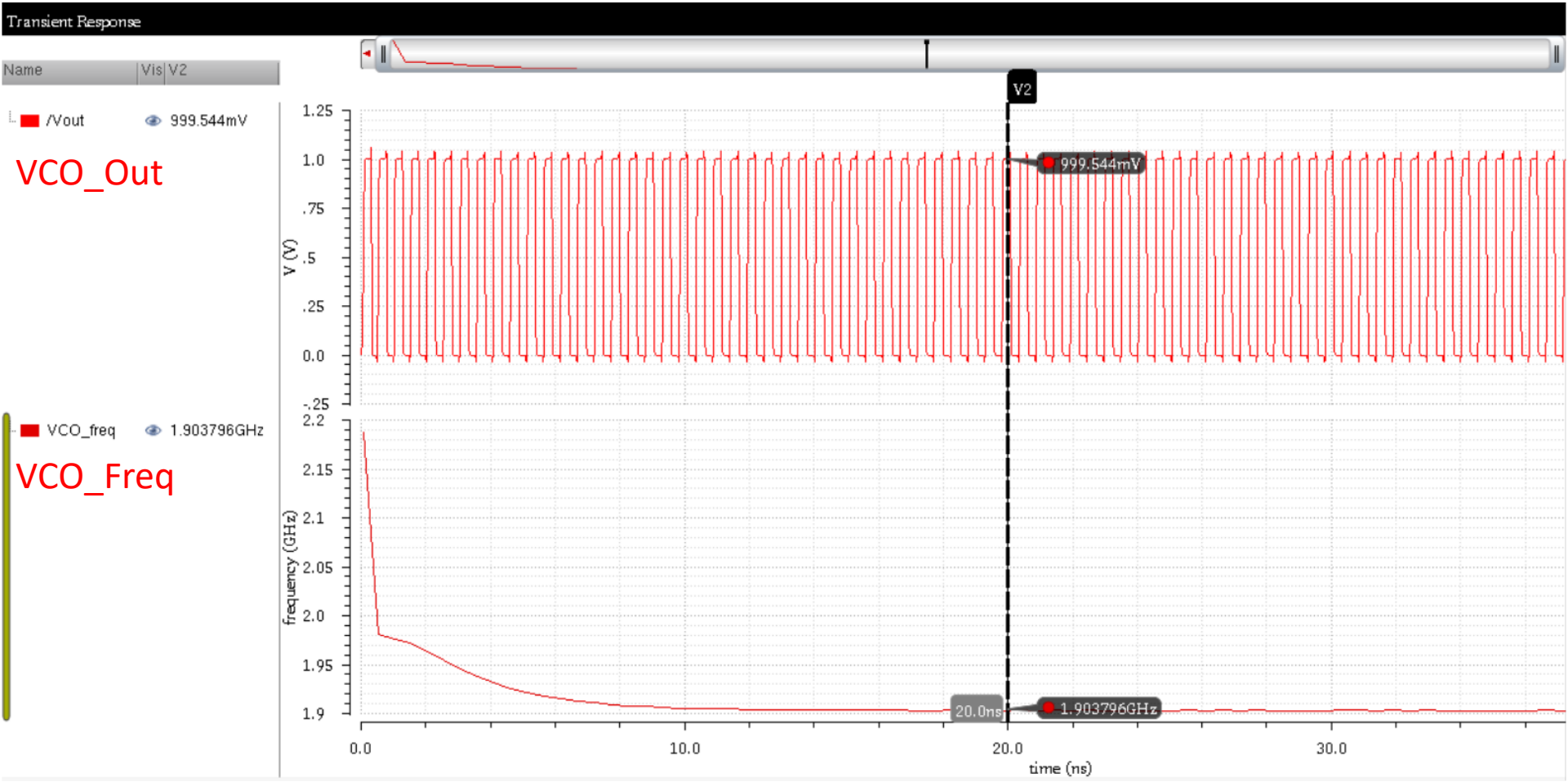
Phase Noise at 1MHz Offset

4- VCO

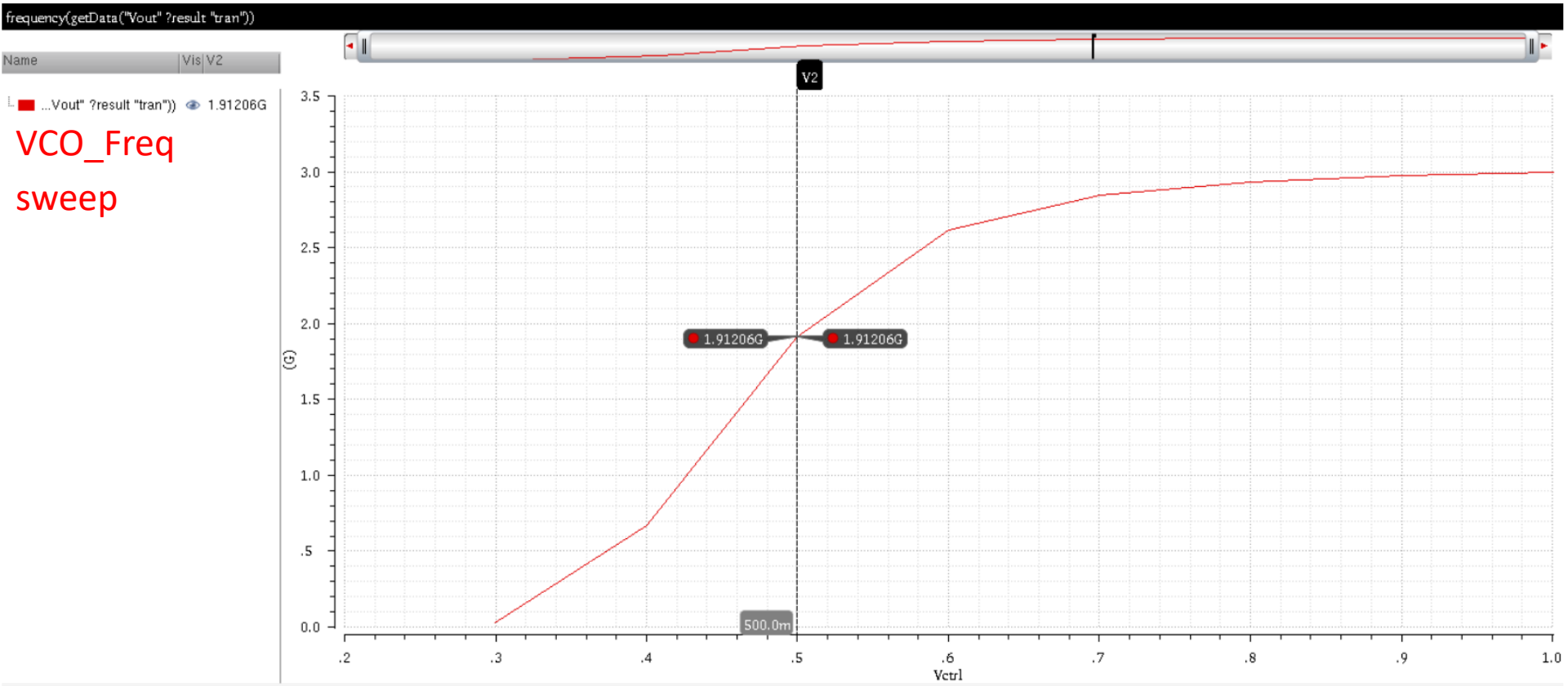
b) Current Starved Ring VCO



Current Starved Ring Oscillator

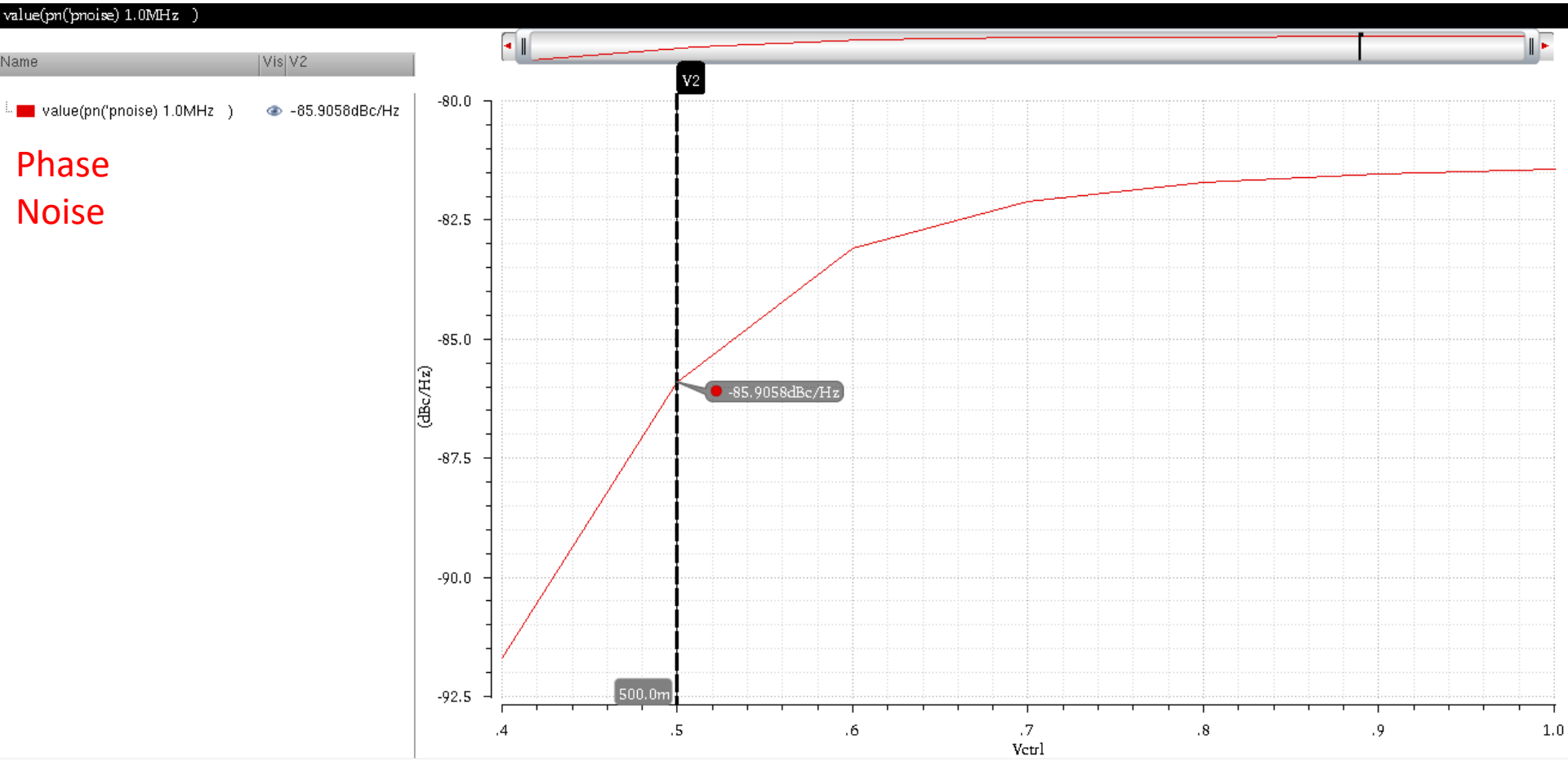


Current Starved Ring Oscillator



Vcontrol Tuning Range

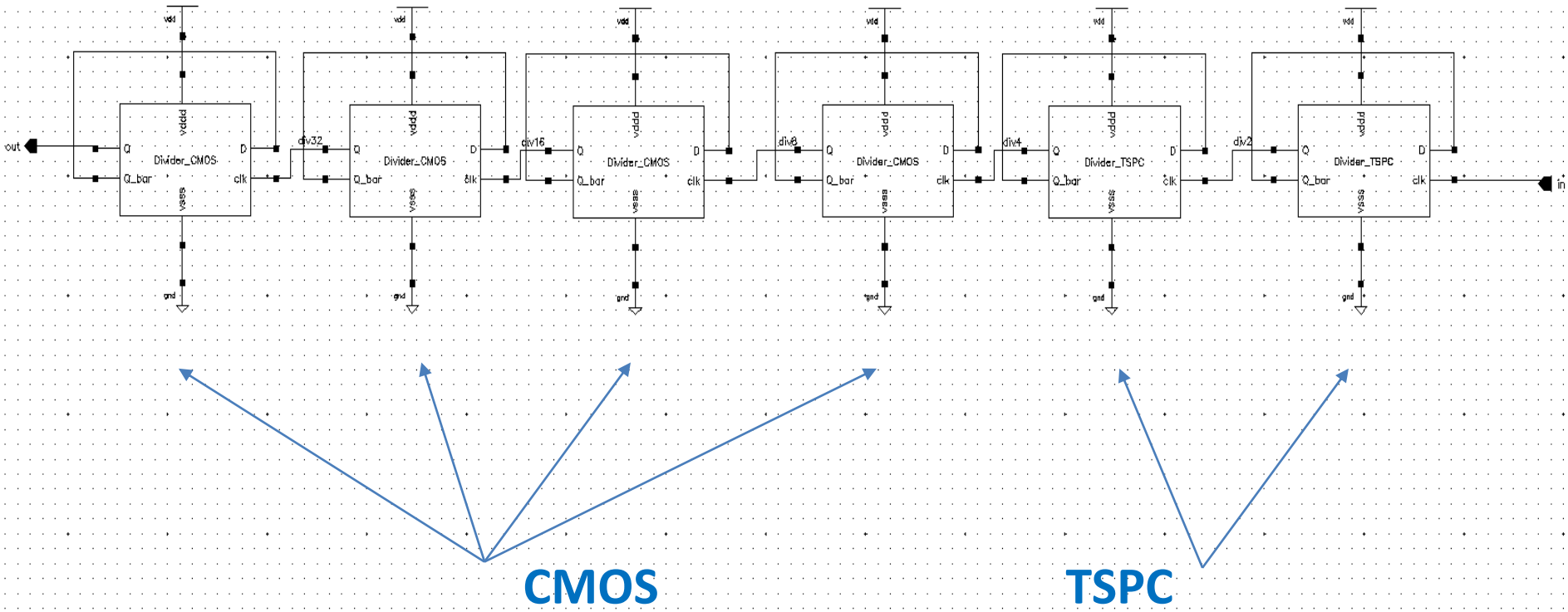
Current Starved Ring Oscillator



Phase Noise at 1MHz Offset

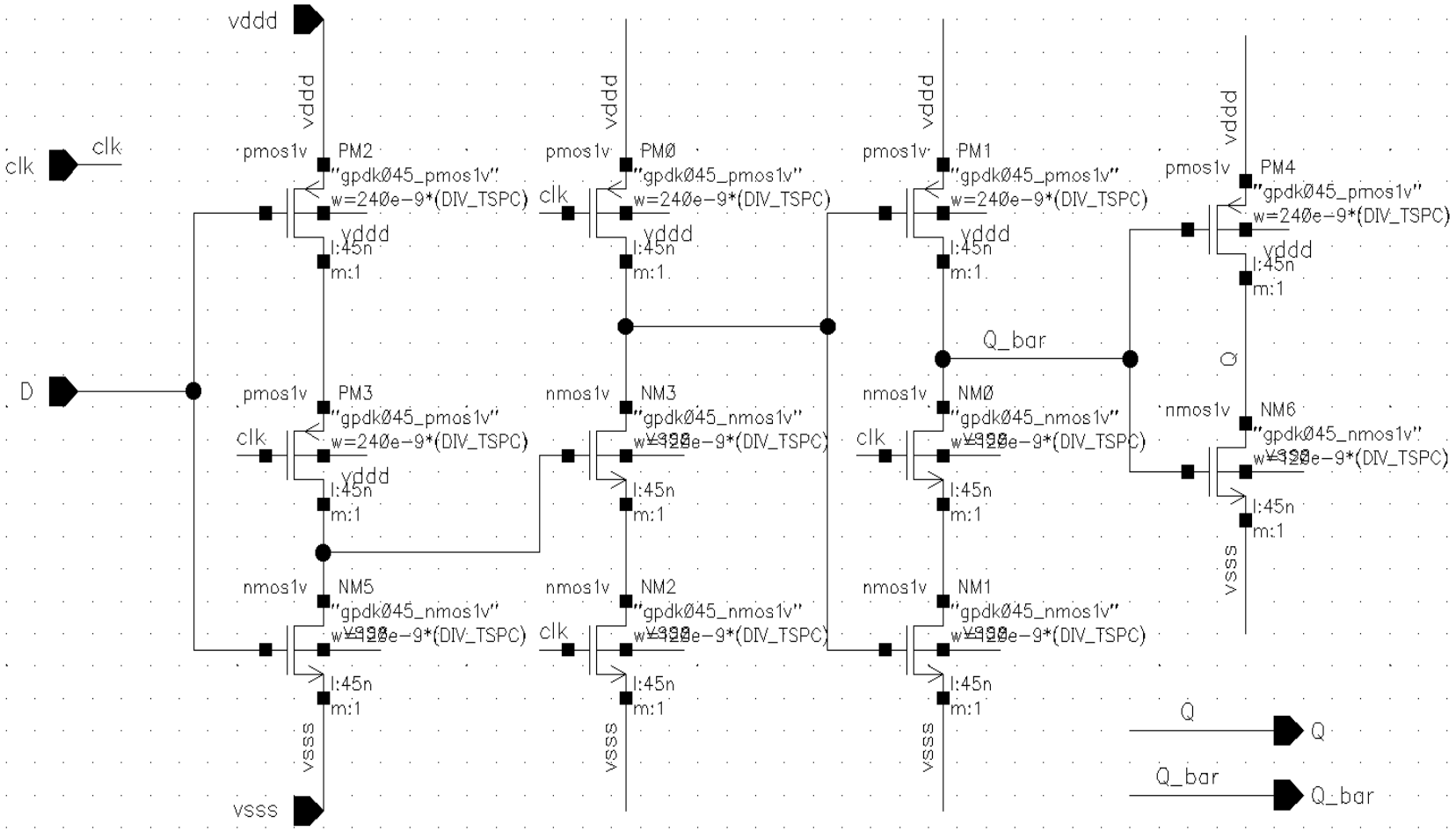
5- Divider

- Divide-by-64
  (6 Divide-by-2 blocks)



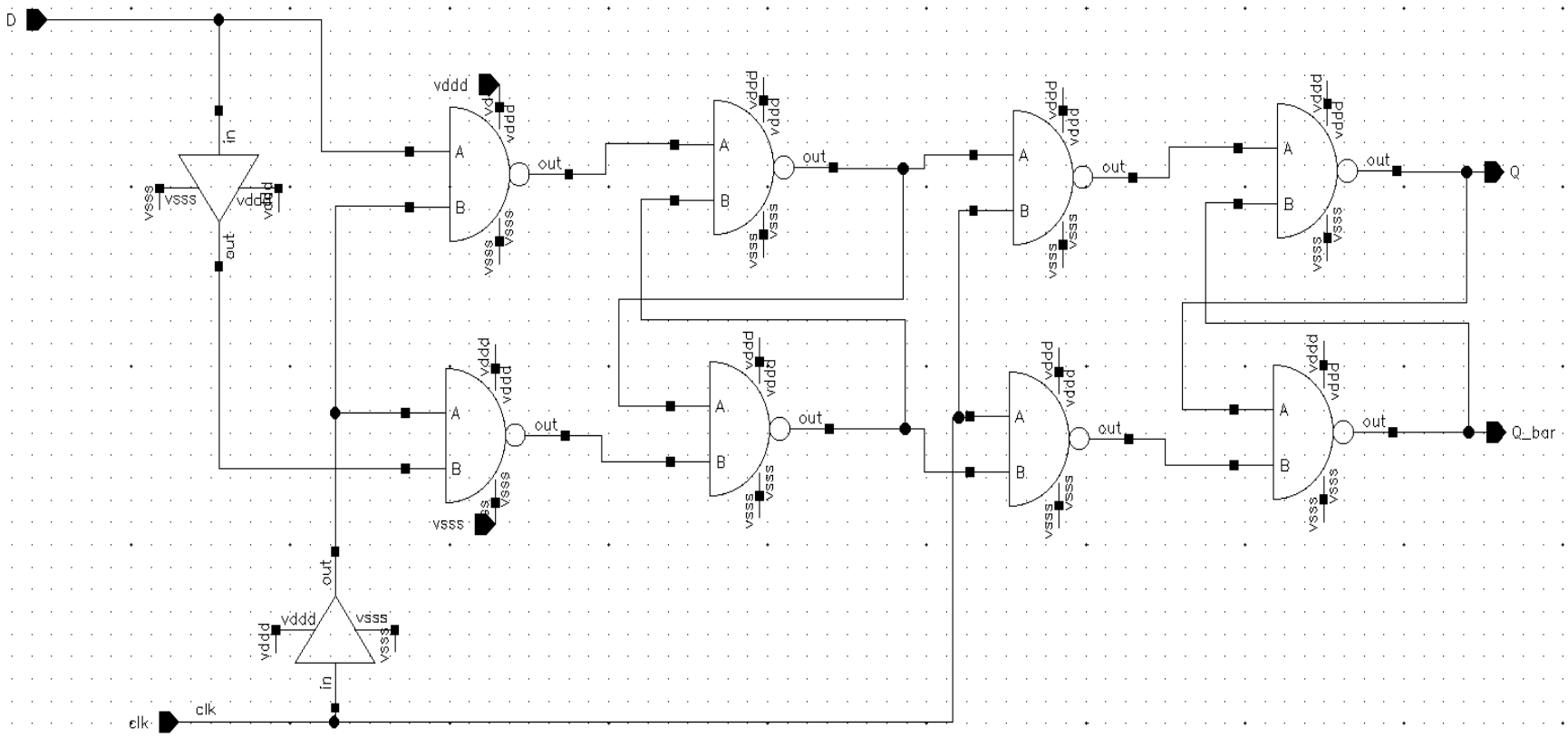
5- Divider

a) TSPC Flipflop



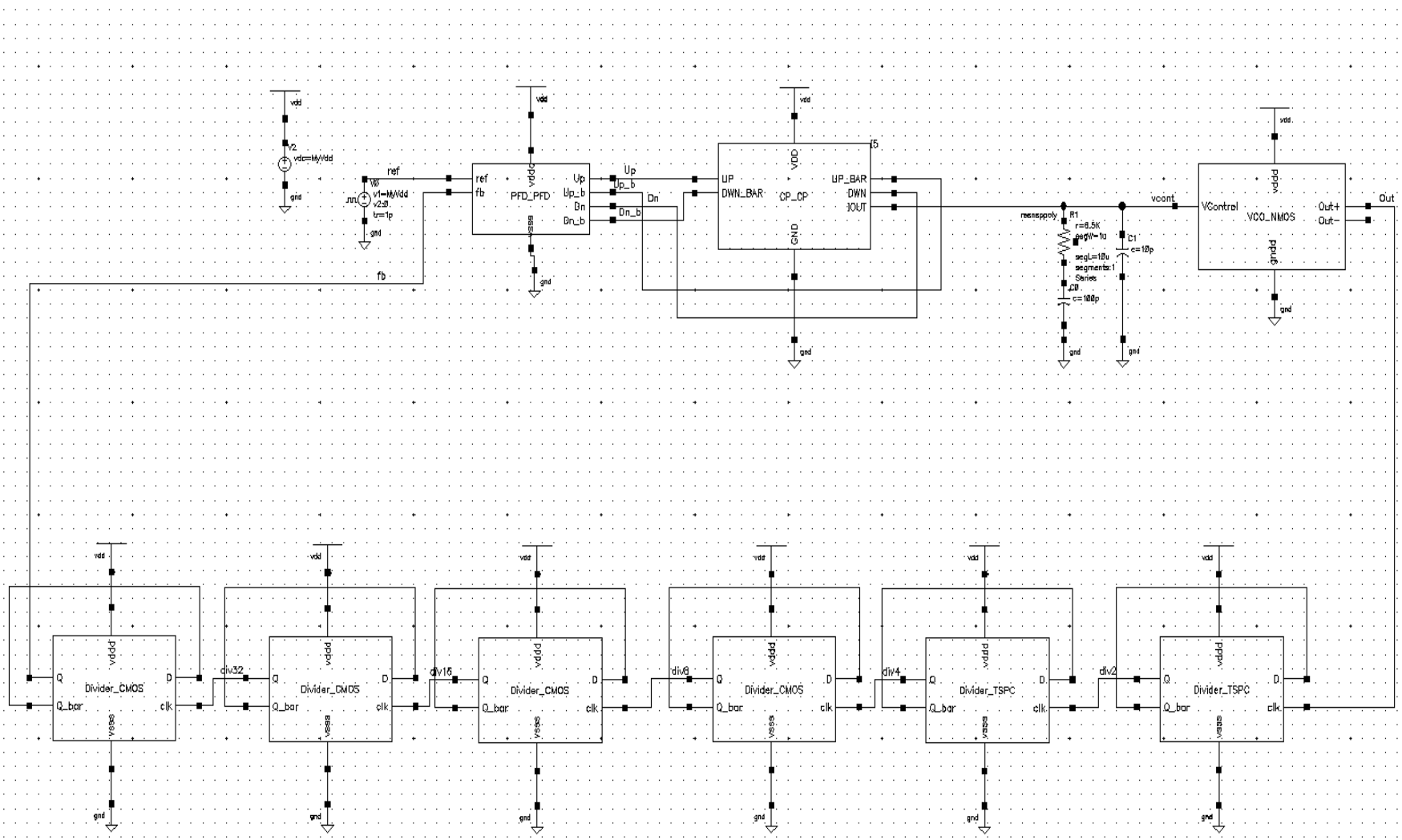
5- Divider

b) CMOS Flipflop



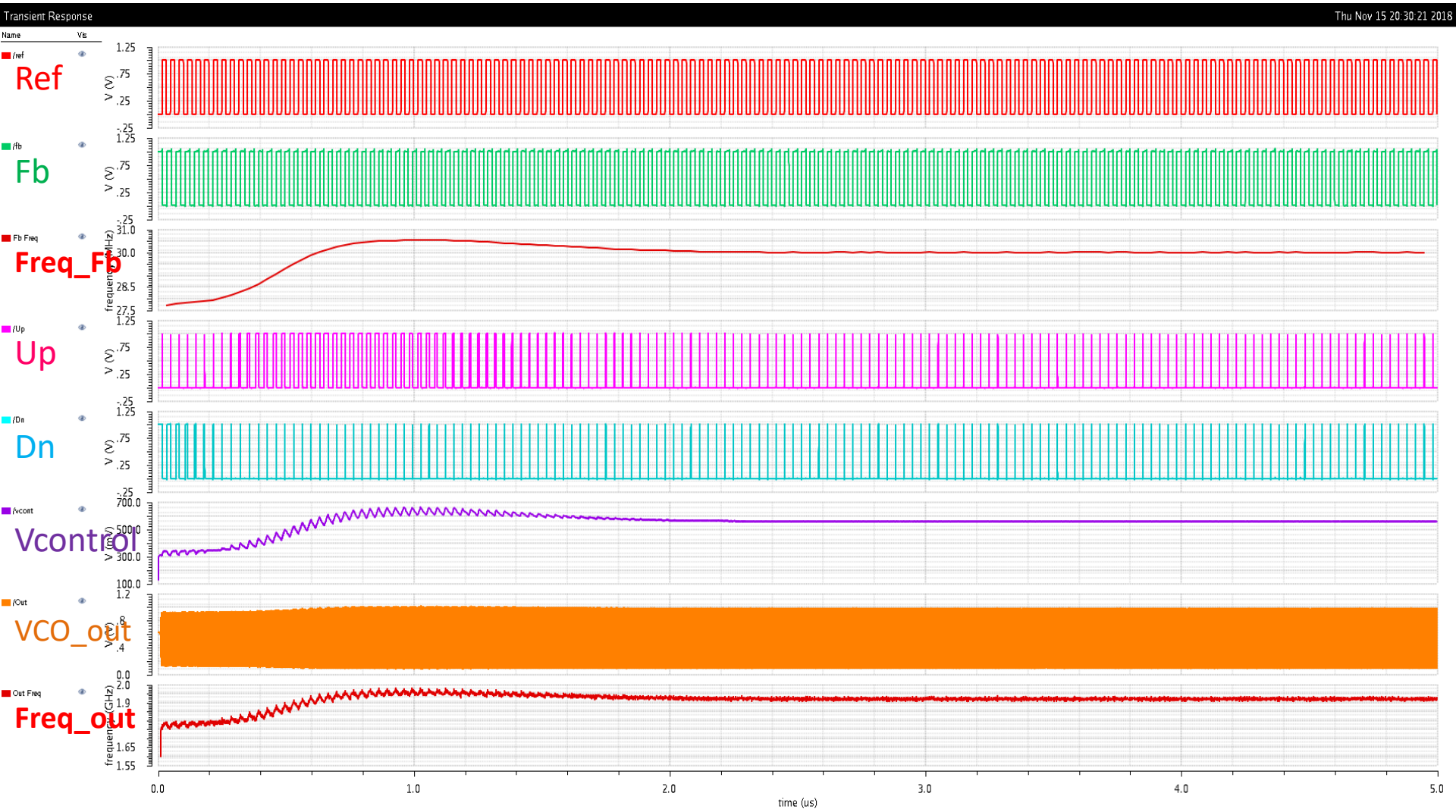
(5)
PLL System Simulations

Test Bench

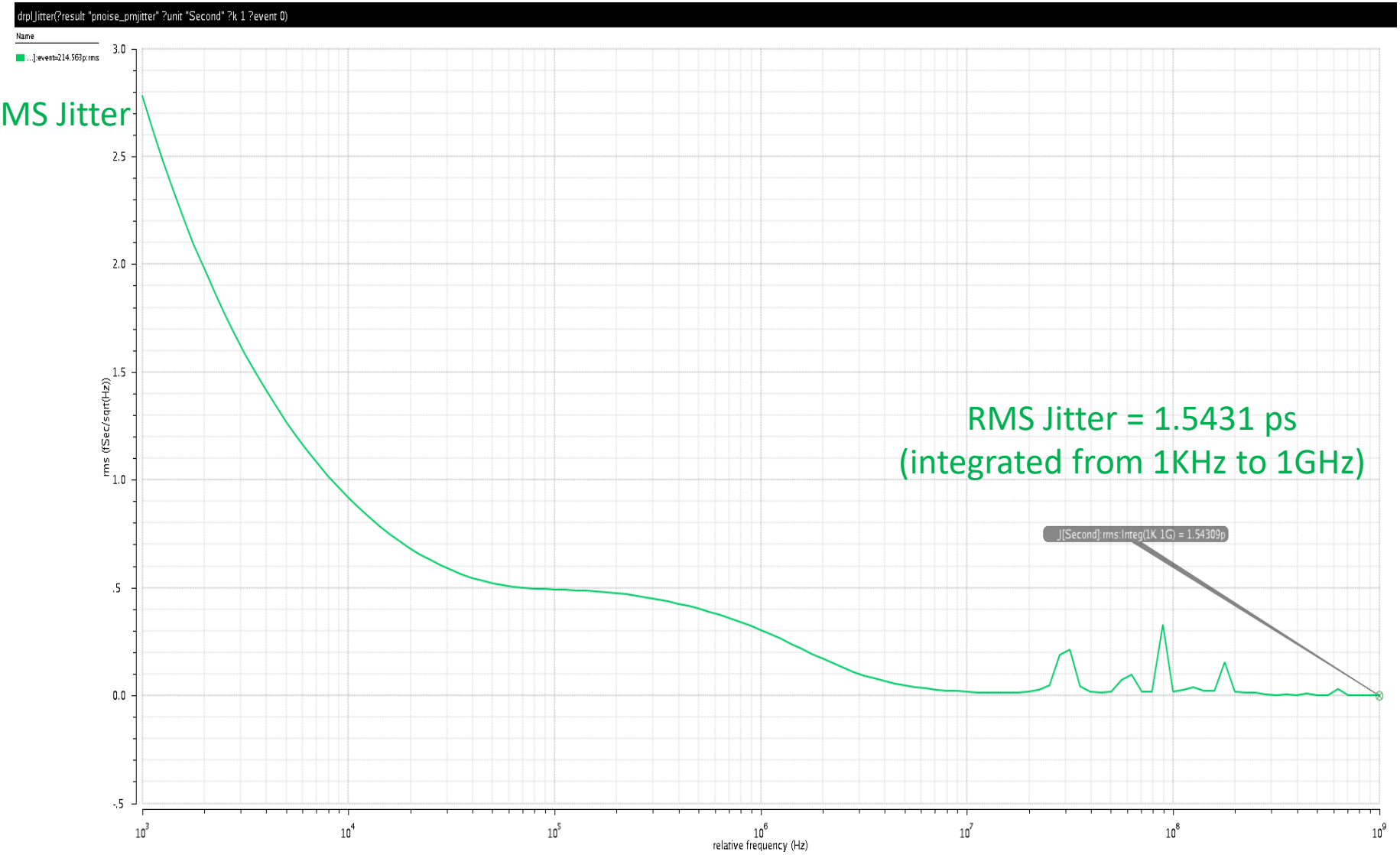

vdd
V2
vdc=MyVdd
gnd
ref
V0
v1=MyVdd
v2=0
tr=1p
fb
PFD_PFD
vddd
vssa
Up
Up_b
Dn
Dn_b
UP
DWN_BAR
CP_CP
GND
VDD
I5
UP_BAR
DWN
IOUT
resnppoly
R1
r=6.5K
segW=1u
segL=10u
segments=1
Series
C0
c=100p
C1
c=10p
vcont
VControl
VCO_NMOS
vddd
Out+
Out-
Out
Divider_CMOS
Divider_TSPC
Q
Q_bar
D
clk
div32
div16
div8
div4
div2

A. Using LC VCO

Waveforms


Transient Response
Thu Nov 15 20:30:21 2018
Name
Vis
/ref
Ref
/fb
Fb
Fb Freq
Freq_Fb
/Up
Up
/Dn
Dn
/vcont
Vcontrol
/Out
VCO_out
Out Freq
Freq_out
V (V)
frequency (MHz)
frequency (GHz)
time (us)
0.0
1.0
2.0
3.0
4.0
5.0

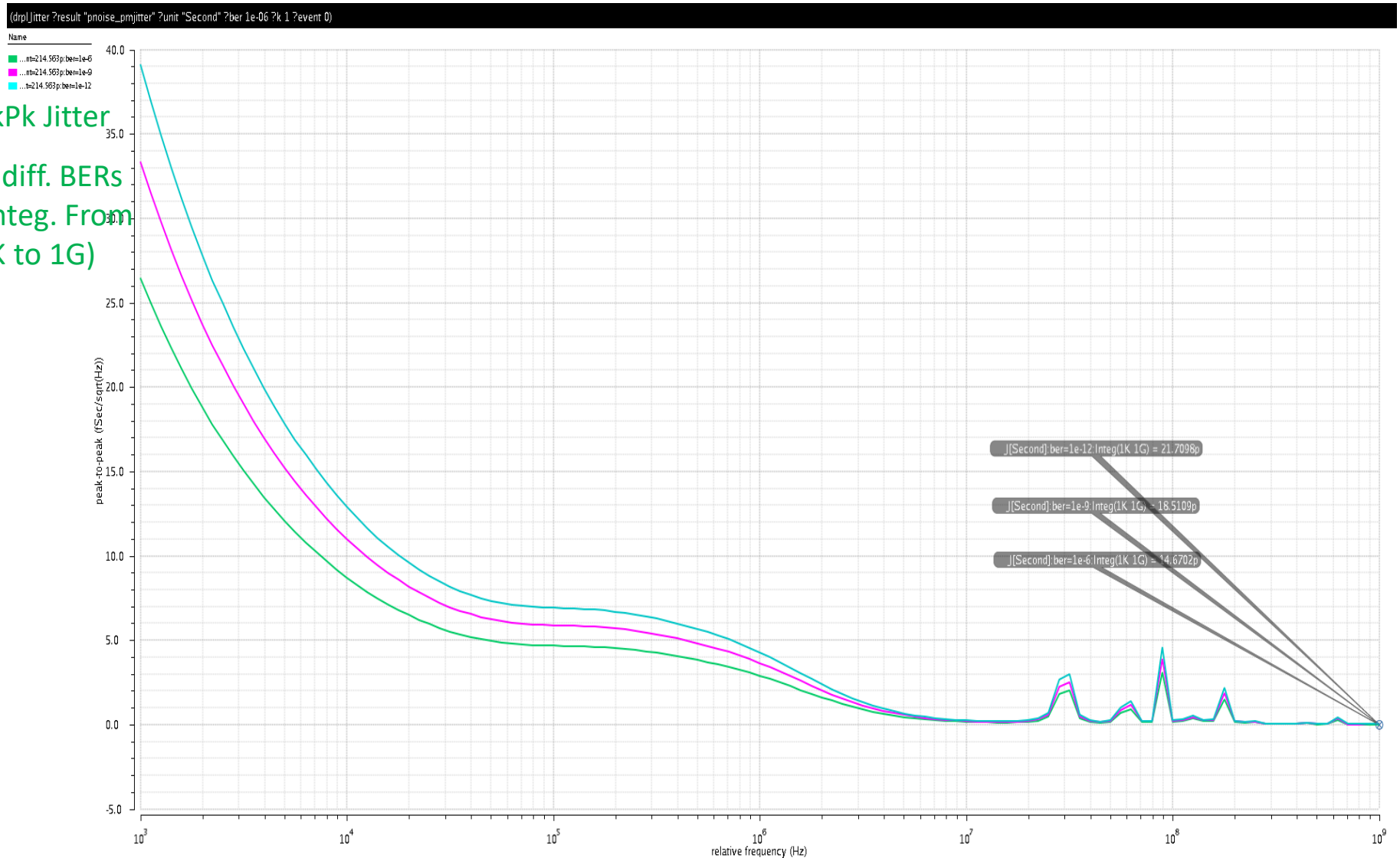
RMS Jitter


drpJitter(?result "pnoise_pmjitter" ?unit "Second" ?k 1 ?event 0)
Name
...]:event=214.563p:rms
RMS Jitter
3.0
2.5
2.0
1.5
1.0
.5
0.0
-.5
rms (fSec/sqrt(Hz))
10^3
10^4
10^5
10^6
10^7
10^8
10^9
relative frequency (Hz)
RMS Jitter = 1.5431 ps
(integrated from 1KHz to 1GHz)
_J[Second]:rms:Integ(1K 1G) = 1.54309p

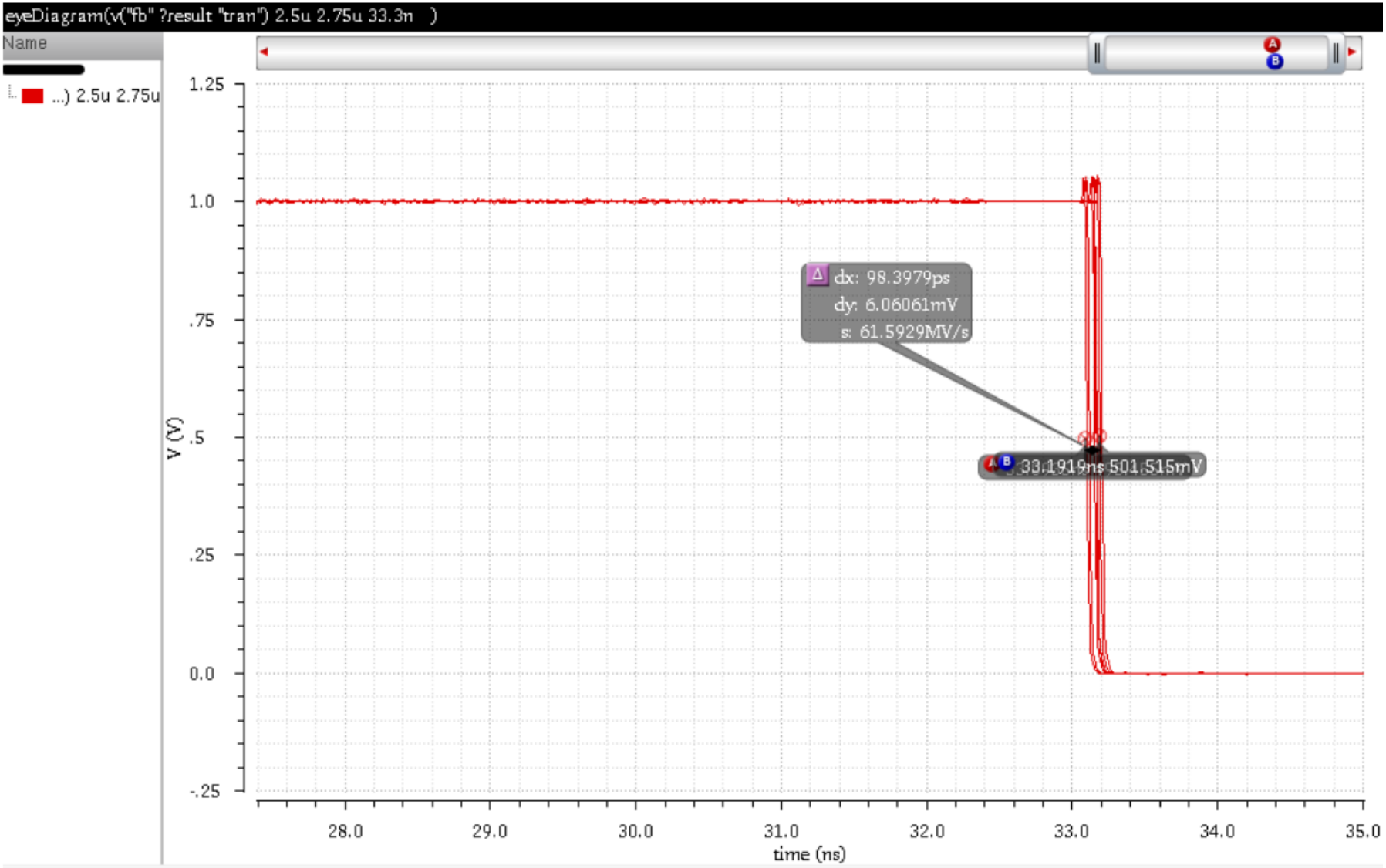
Pk-Pk Jitter

PkPk Jitter

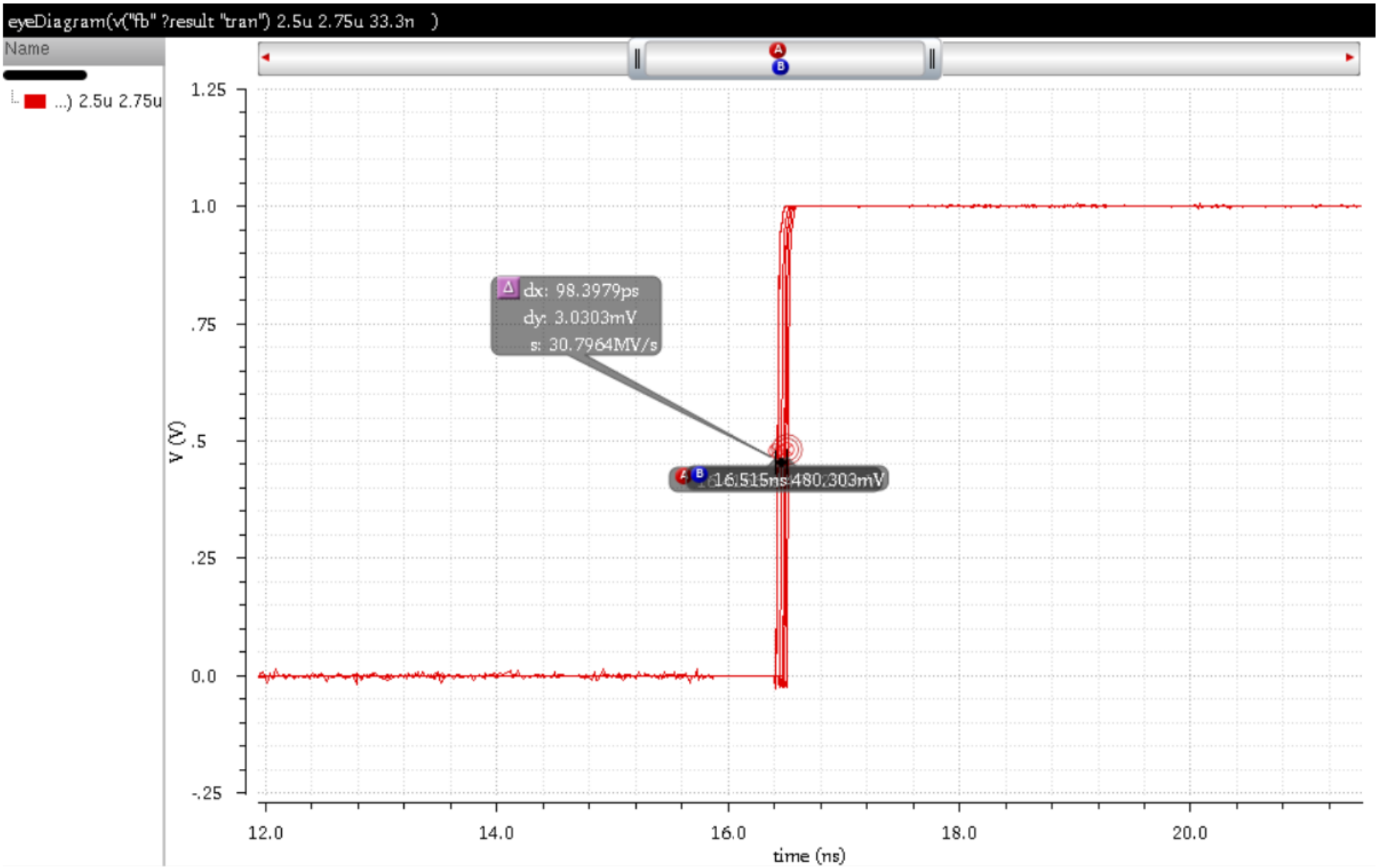
@diff. BERs (integ. From 1K to 1G)



Eye Diagram Jitter

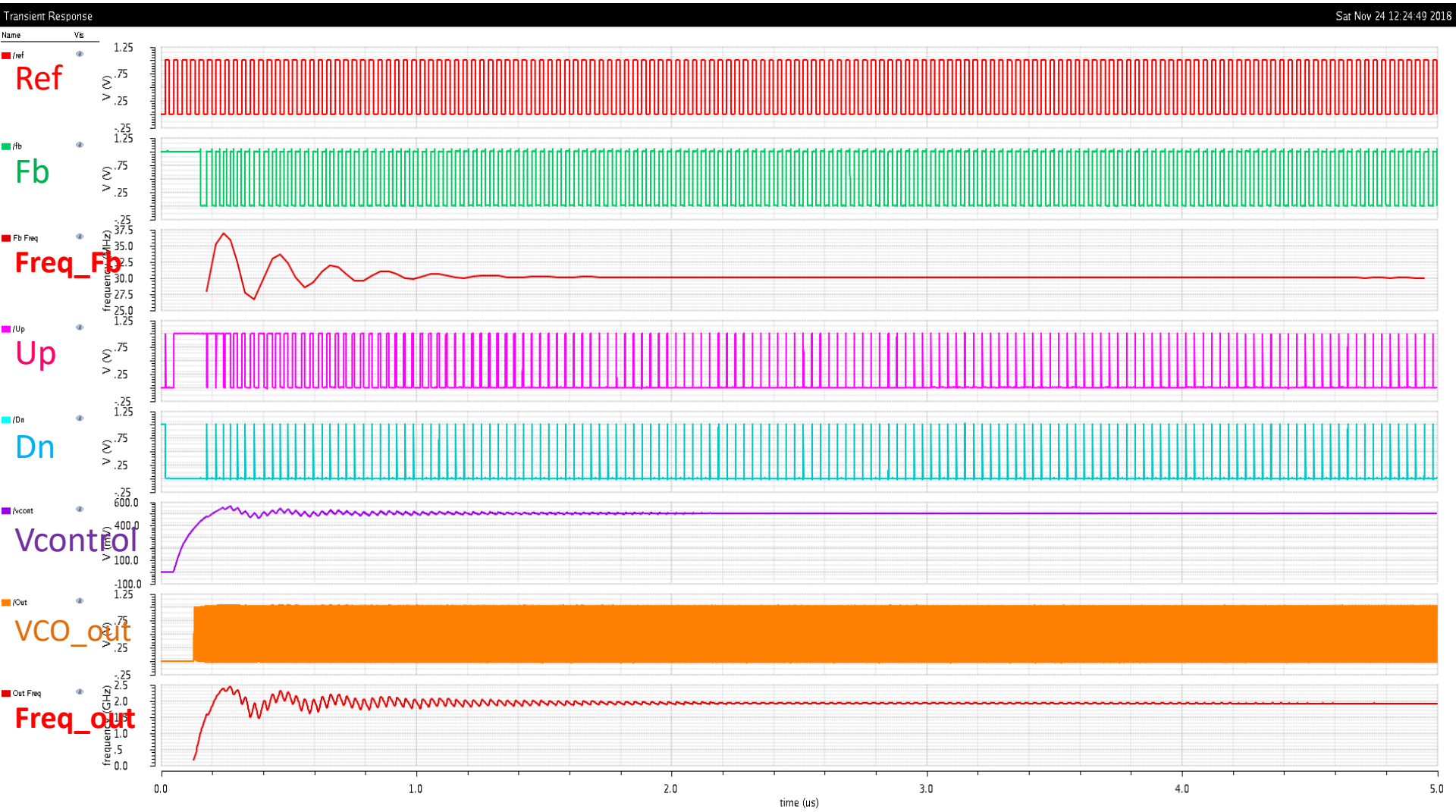


Eye Diagram Jitter

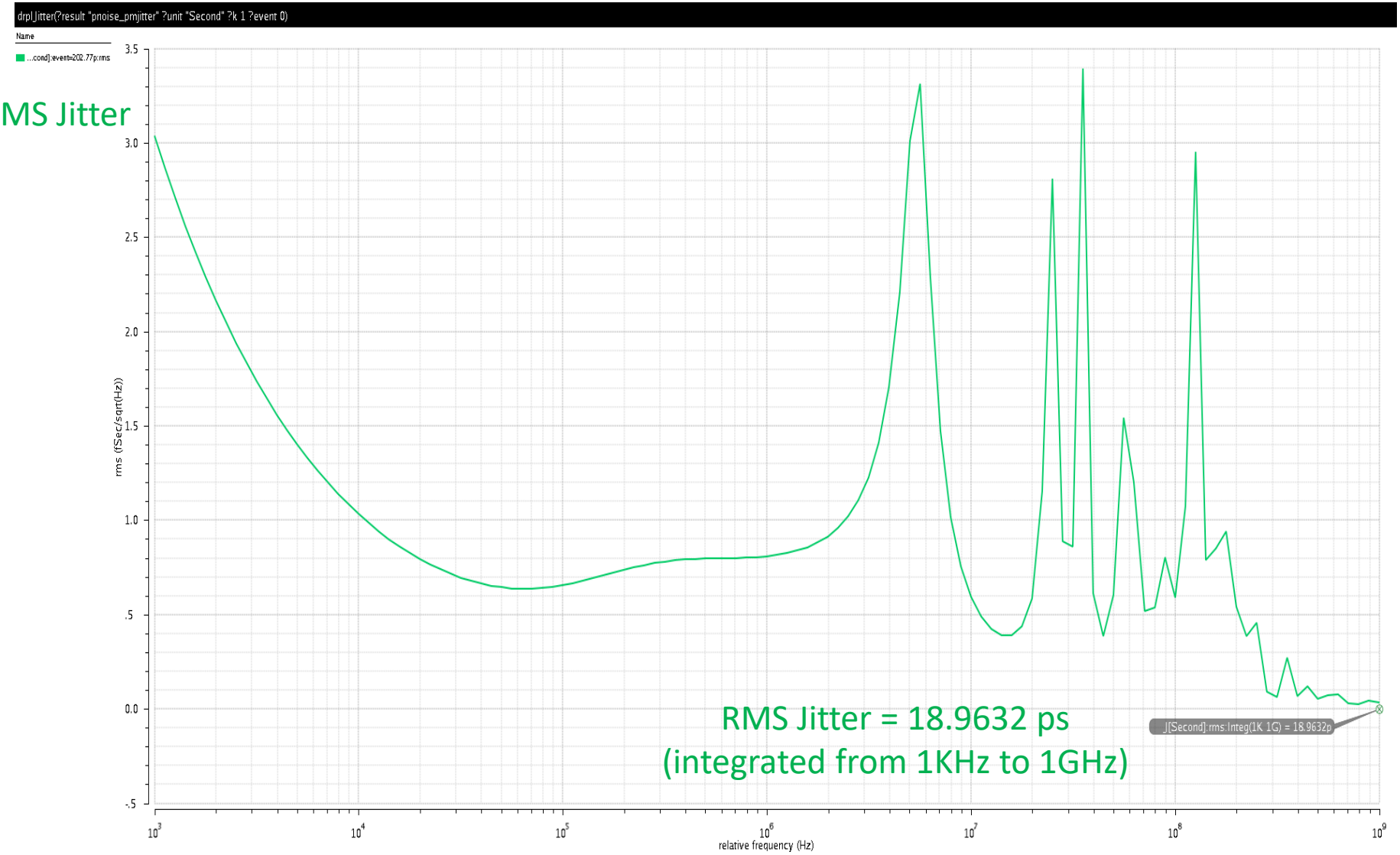


B. Using Current-Starved Ring VCO

Waveforms


Transient Response
Sat Nov 24 12:24:49 2018
Name
Vis
/ref
Ref
/fb
Fb
Fb Freq
Freq_Fb
/Up
Up
/Dn
Dn
/vcont
Vcontrol
/Out
VCO_out
Out Freq
Freq_out
V (V)
frequency (MHz)
V (mV)
frequency (GHz)
time (us)
0.0
1.0
2.0
3.0
4.0
5.0

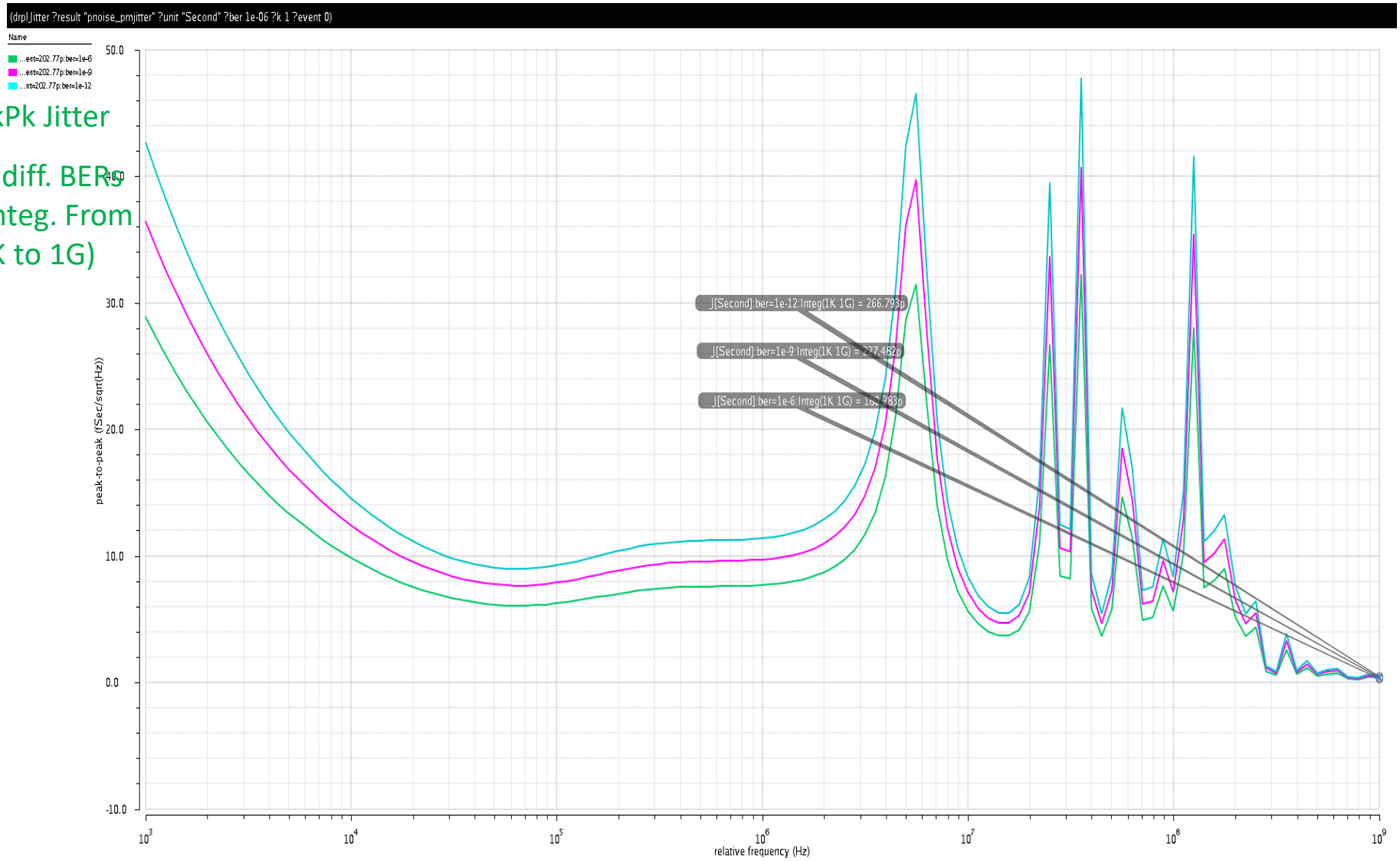
RMS Jitter


drpJitter(?result "pnoise_pmjitter" ?unit "Second" ?k 1 ?event 0)
Name
...cond]:event=202.77p:rms
RMS Jitter
rms (fSec/sqrt(Hz))
relative frequency (Hz)
RMS Jitter = 18.9632 ps
(integrated from 1KHz to 1GHz)
_J[Second]:rms:Integ(1K 1G) = 18.9632p

Pk-Pk Jitter

PkPk Jitter

@diff. BERs (integ. From 1K to 1G)

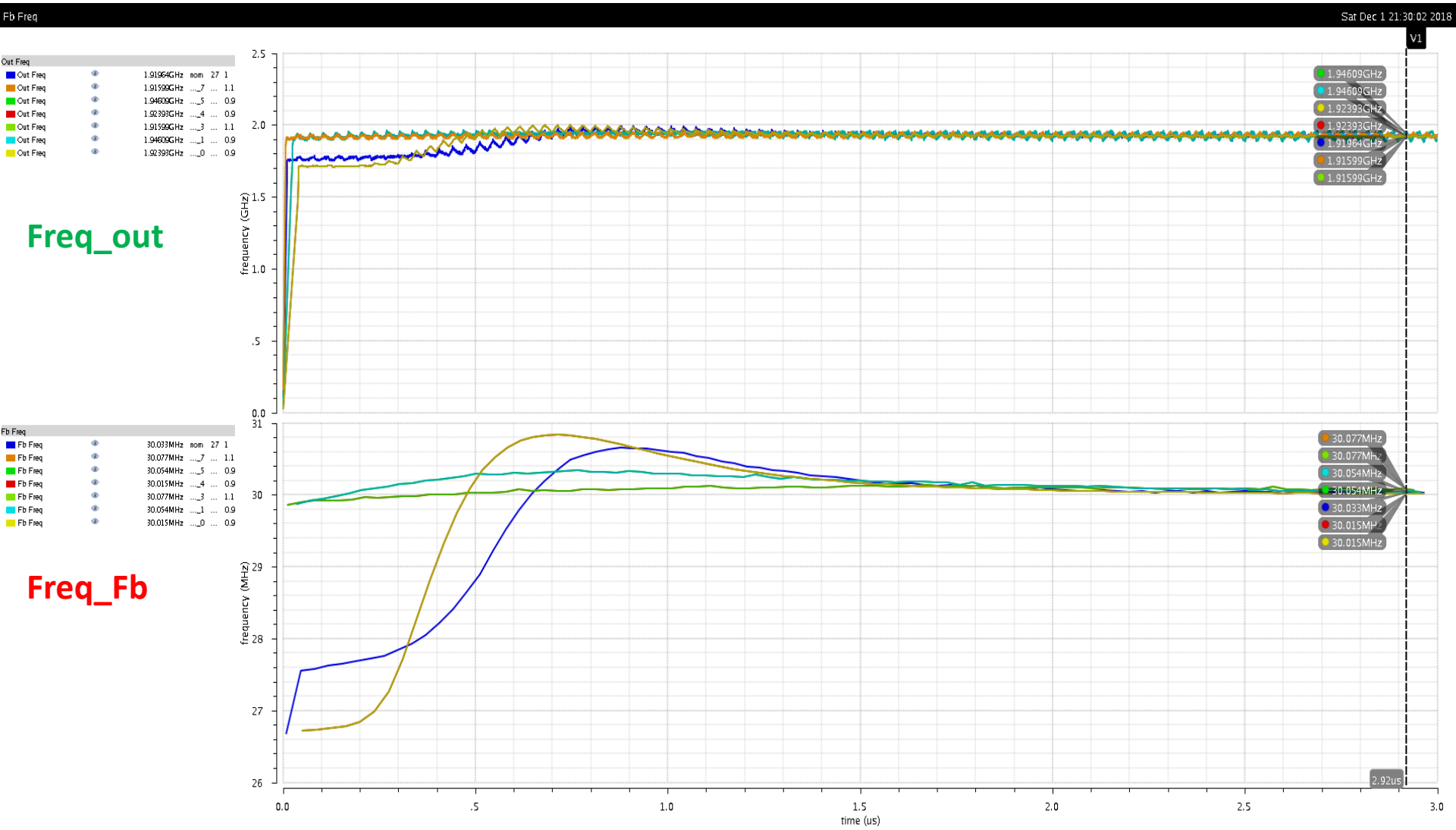


Comparison

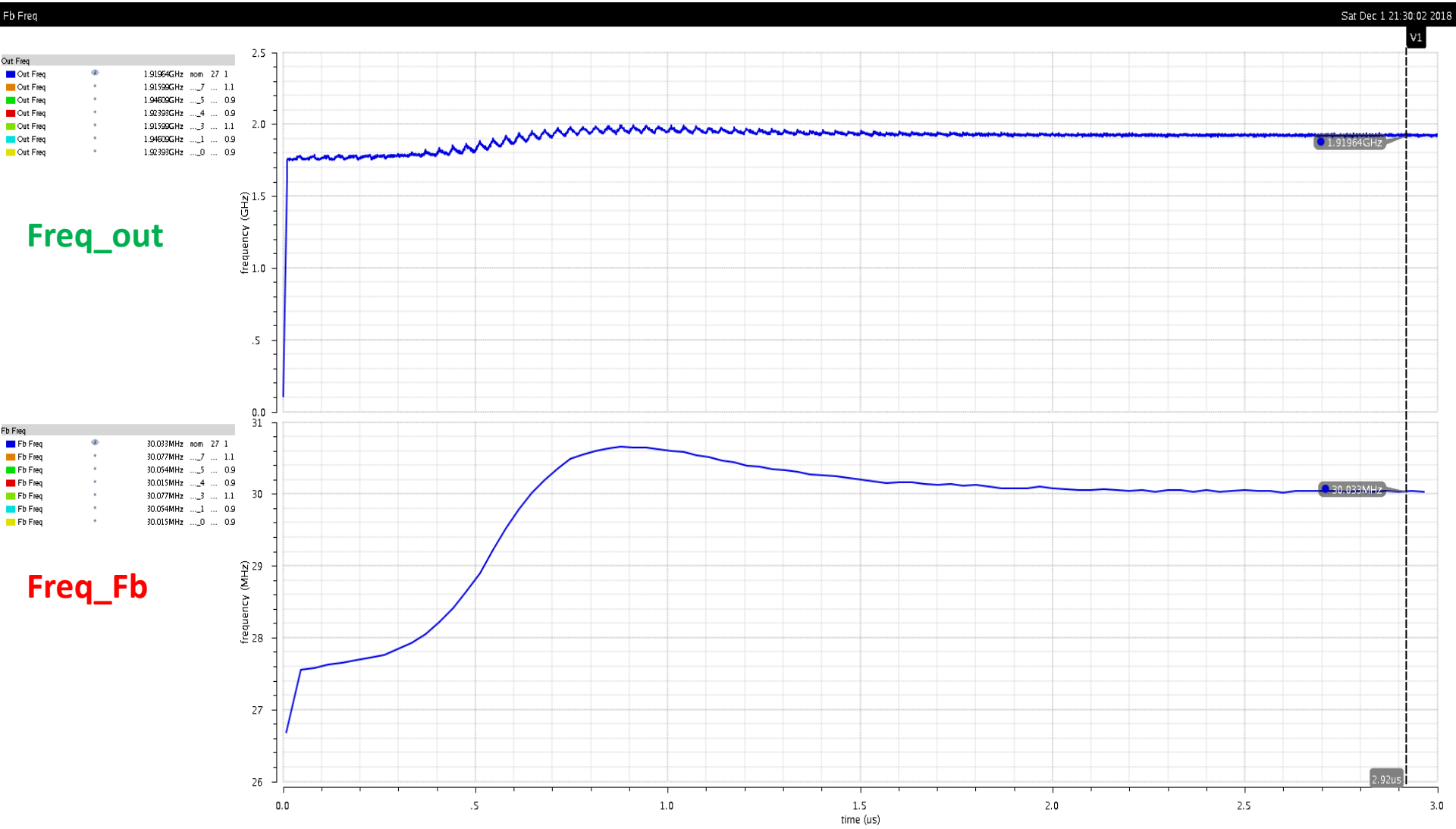
	PLL with LC VCO	PLL with Ring VCO
Tuning Range	1.68 GHz – 2.02 GHz	0.5 GHz – 3 GHz
Locking Time	< 2.1 us	< 1.5 us
P dissipation	1.26175 mW	1.21701 mW
RMS Jitter	1.5421 ps	18.9632 ps
FOM	**-235.23 dB**	**-213.59 dB**

(6)
Corner Simulations

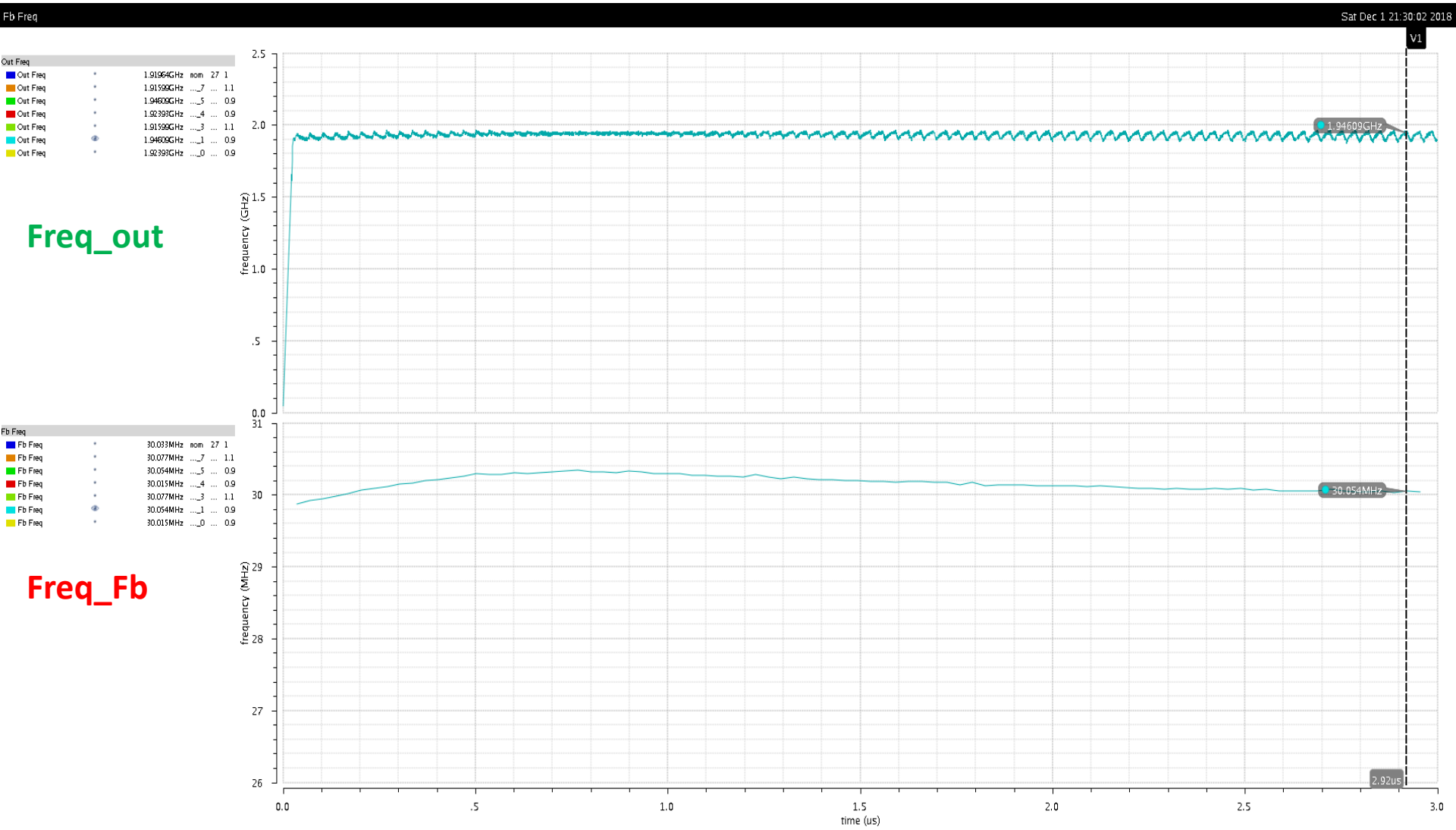
All Corners


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
frequency (GHz)
2.5
2.0
1.5
1.0
.5
0.0
1.94609GHz
1.94609GHz
1.92393GHz
1.92393GHz
1.91964GHz
1.91599GHz
1.91599GHz
Fb Freq
Fb Freq 30.033MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (MHz)
31
30
29
28
27
26
30.077MHz
30.077MHz
30.054MHz
30.054MHz
30.033MHz
30.015MHz
30.015MHz
2.92us
0.0
.5
1.0
1.5
2.0
2.5
3.0
time (us)

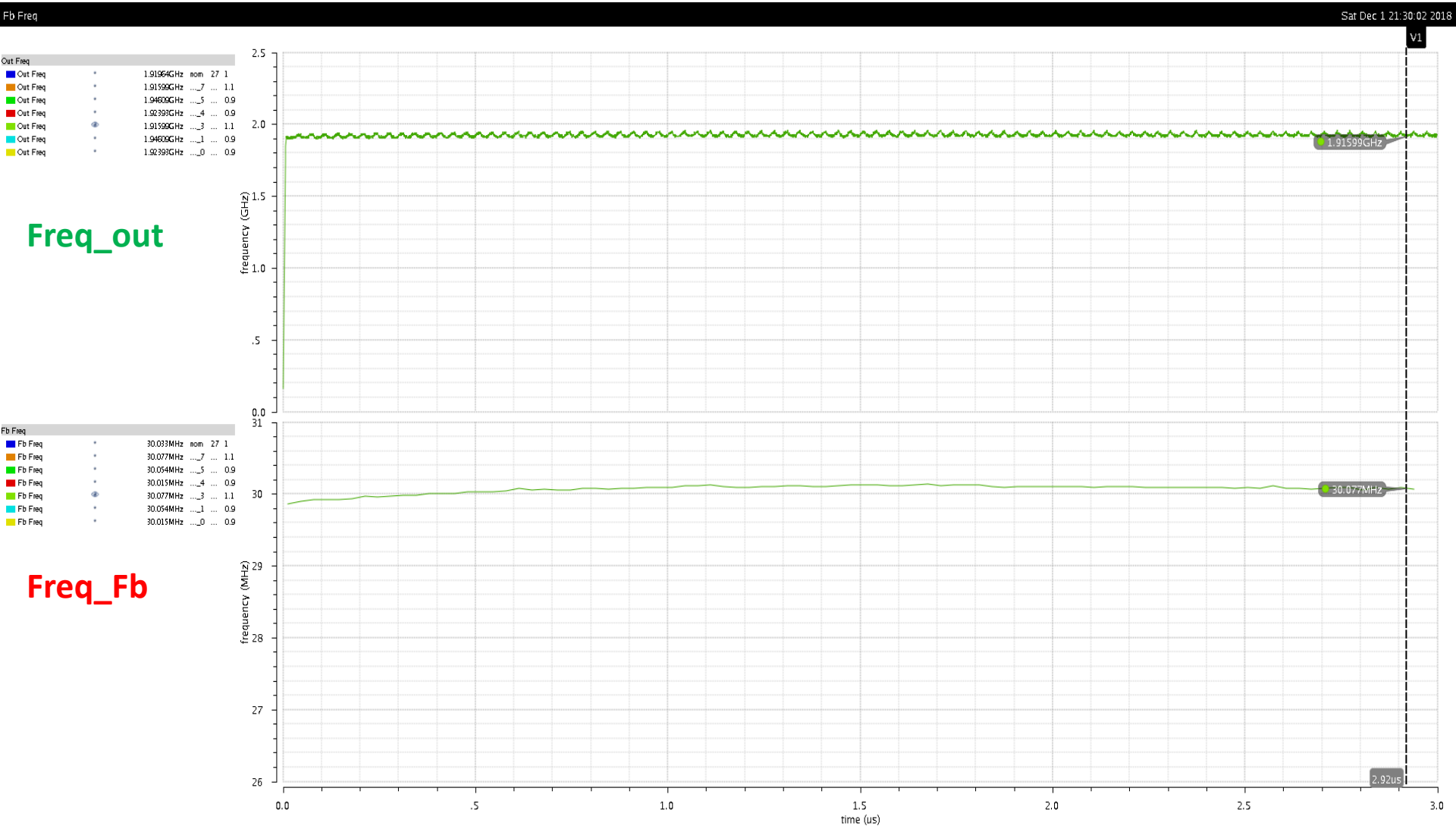
Nominal
TT, 27°, 1 V_{DD}



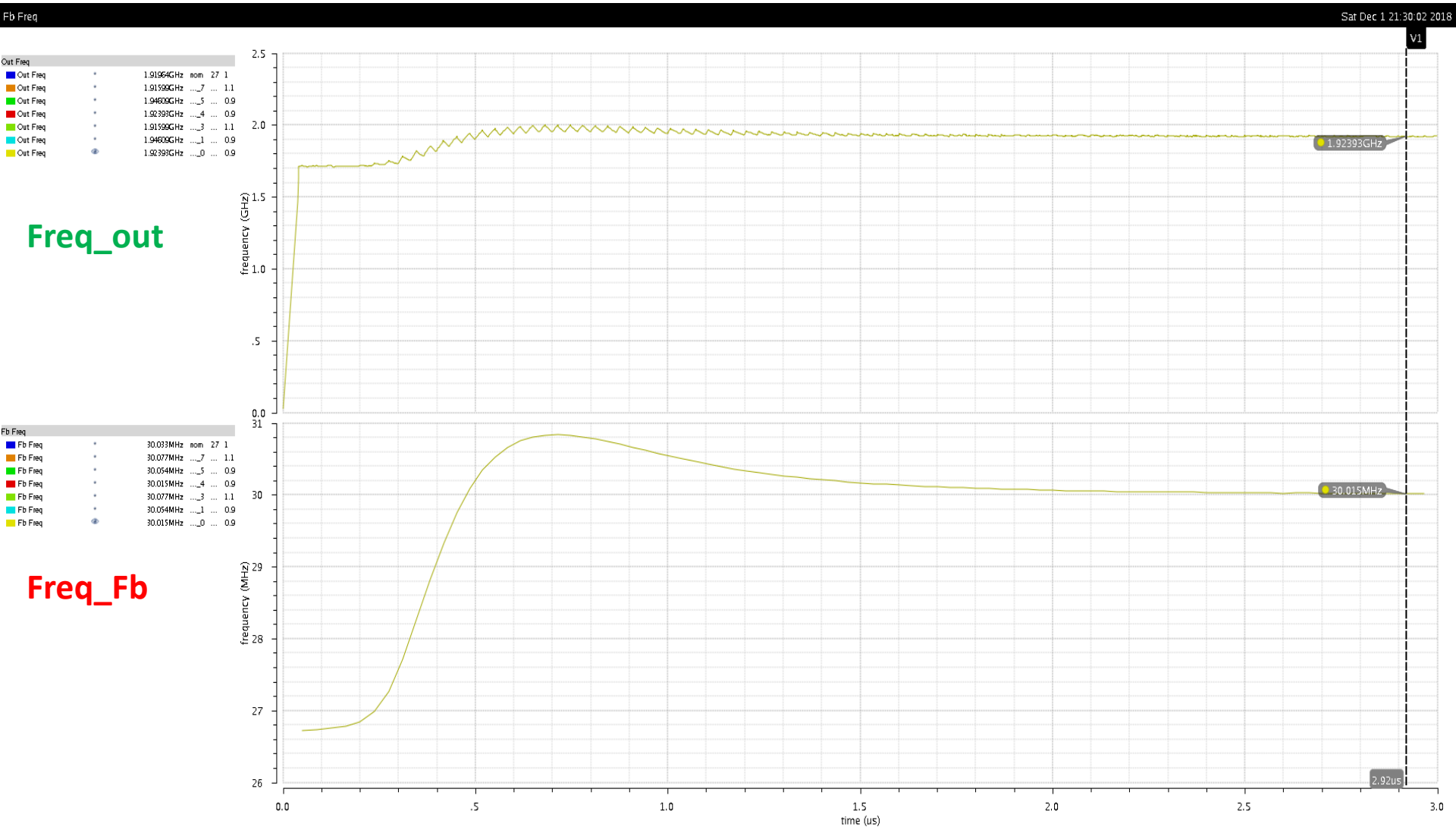
FF, 125°, 0.9 V_{DD}


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
Fb Freq
Fb Freq 30.083MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (GHz)
2.5
2.0
1.5
1.0
.5
0.0
1.94609GHz
frequency (MHz)
31
30
29
28
27
26
30.054MHz
2.92us
0.0
.5
1.0
1.5
2.0
2.5
3.0
time (us)

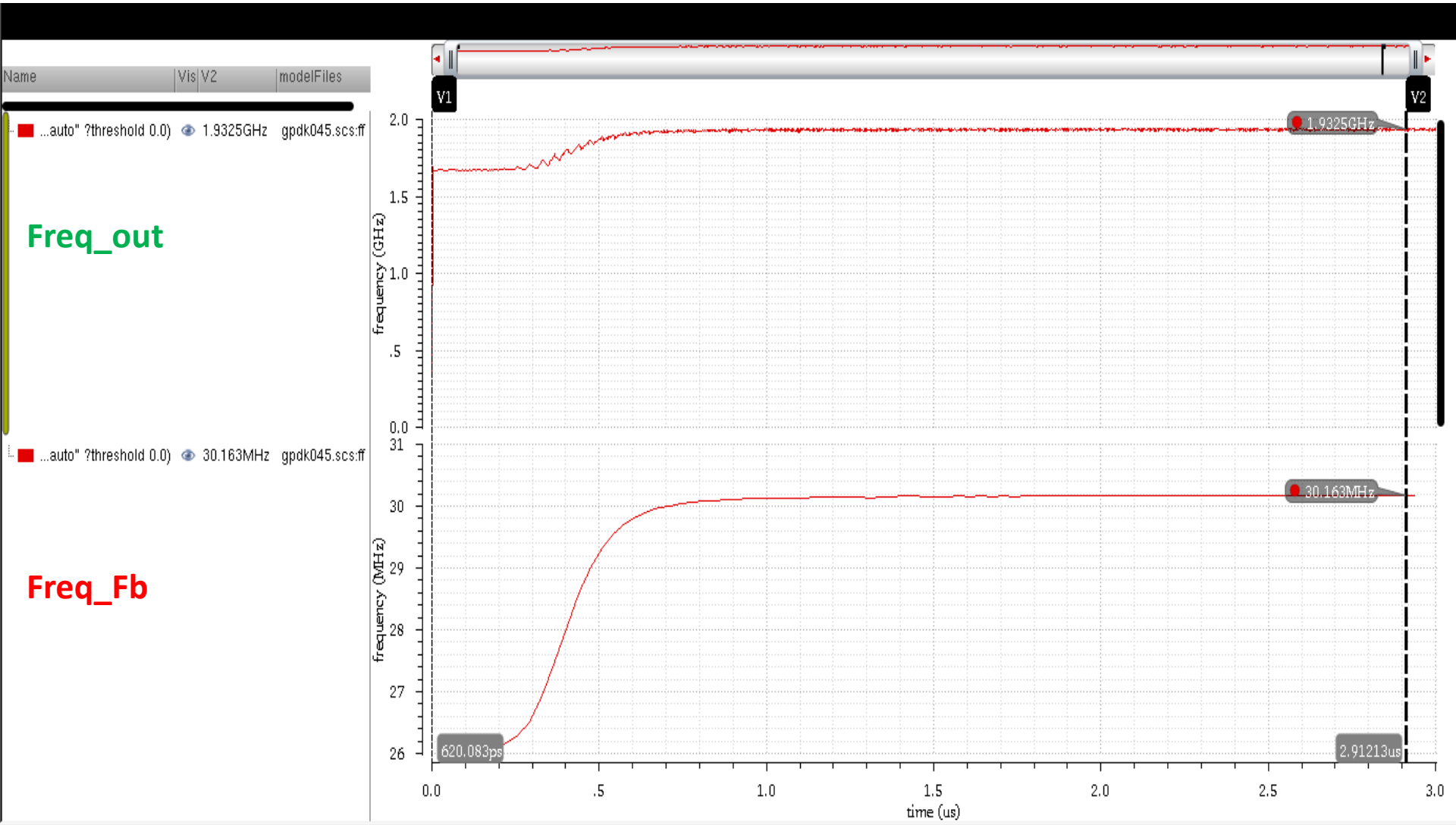
FF, 125°, 1.1 V_{DD}


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
Fb Freq
Fb Freq 30.033MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (GHz)
2.5
2.0
1.5
1.0
.5
0.0
1.91599GHz
frequency (MHz)
31
30
29
28
27
26
30.077MHz
2.92us
0.0
.5
1.0
1.5
2.0
2.5
3.0
time (us)

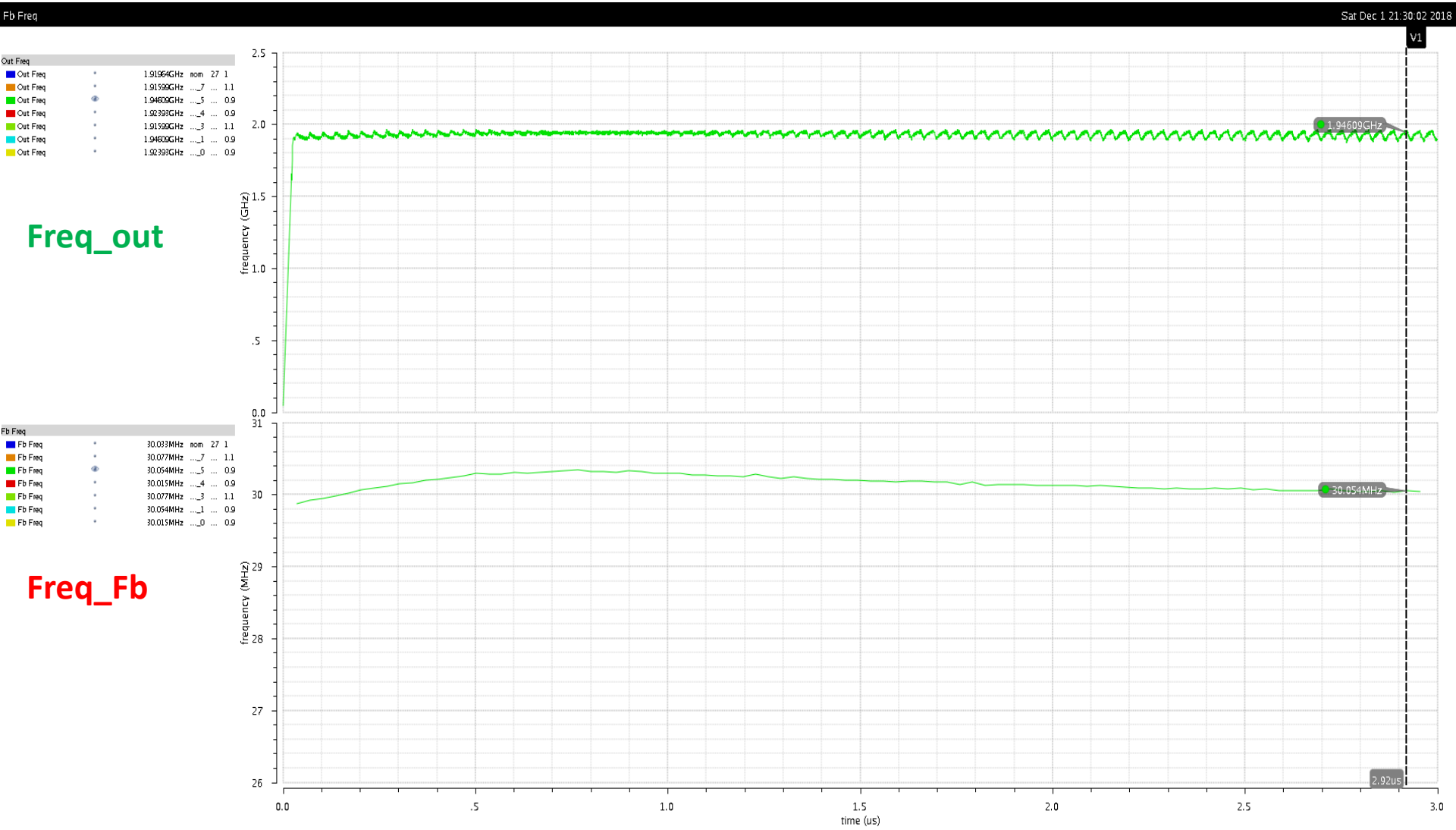
FF, -40°, 0.9 V_{DD}


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
Fb Freq
Fb Freq 30.033MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (GHz)
2.5
2.0
1.5
1.0
.5
0.0
1.92393GHz
frequency (MHz)
31
30
29
28
27
26
30.015MHz
2.92us
0.0
.5
1.0
1.5
2.0
2.5
3.0
time (us)

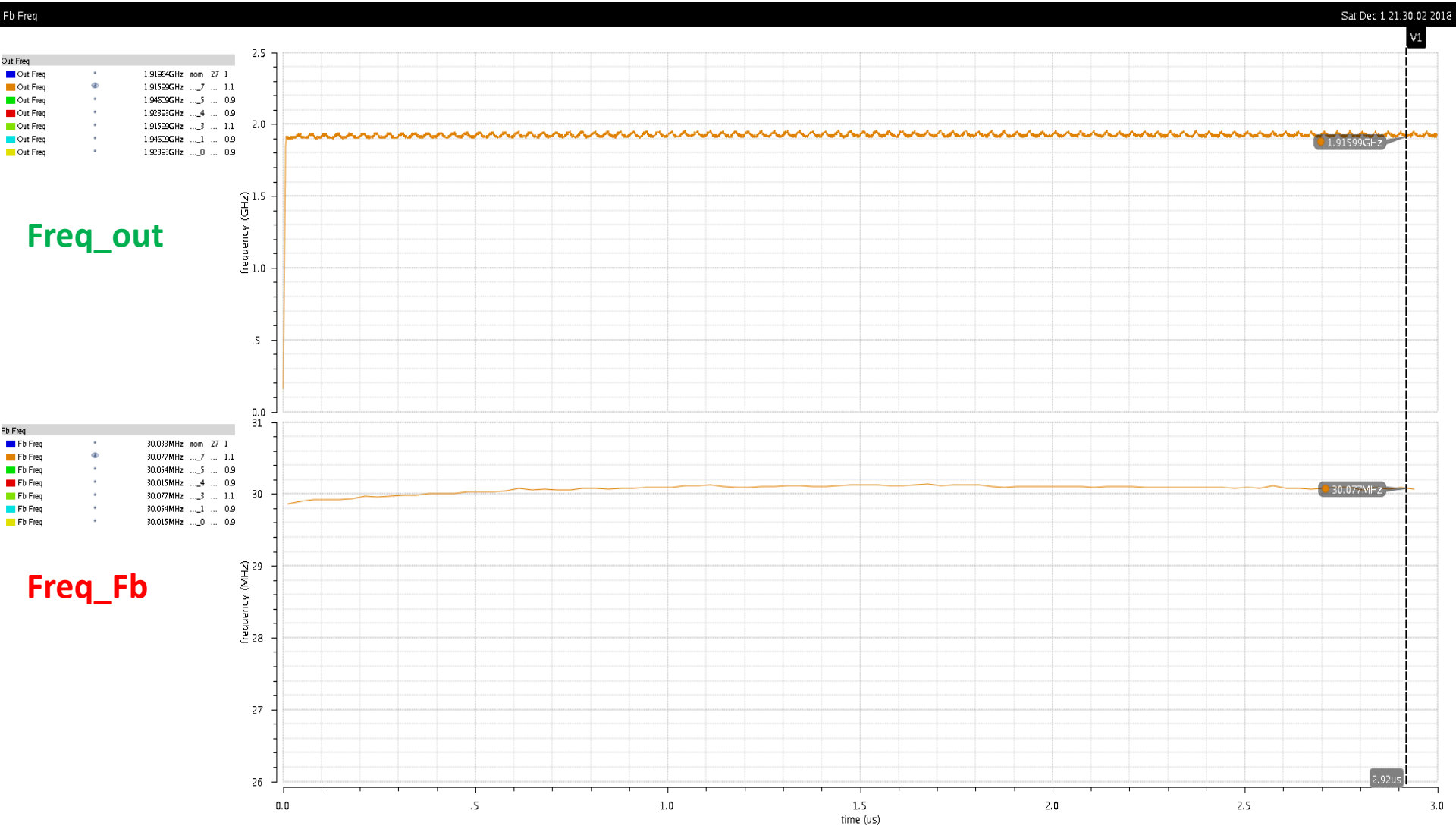
FF, -40°, 1.1 V_{DD}


Name
Vis
V2
modelFiles
...auto" ?threshold 0.0) 1.9325GHz gpdk045.scs:ff
Freq_out
...auto" ?threshold 0.0) 30.163MHz gpdk045.scs:ff
Freq_Fb
V1
V2
1.9325GHz
30.163MHz
620.083ps
2.91213us
frequency (GHz)
frequency (MHz)
time (us)
0.0
.5
1.0
1.5
2.0
2.5
3.0
26
27
28
29
30
31

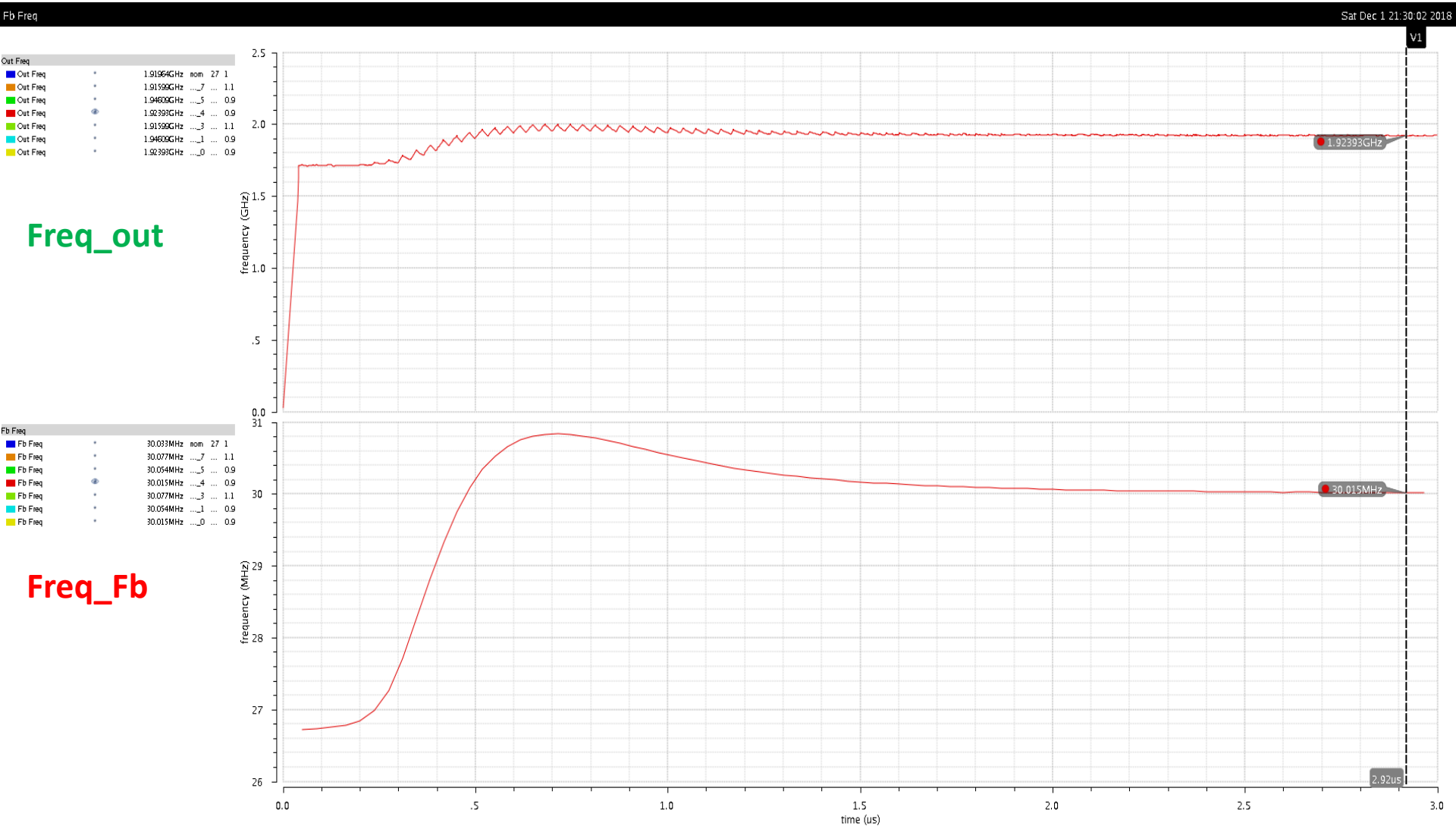
SS, 125°, 0.9 V_{DD}


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
Fb Freq
Fb Freq 30.083MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (GHz)
1.94609GHz
frequency (MHz)
30.054MHz
2.92us
time (us)

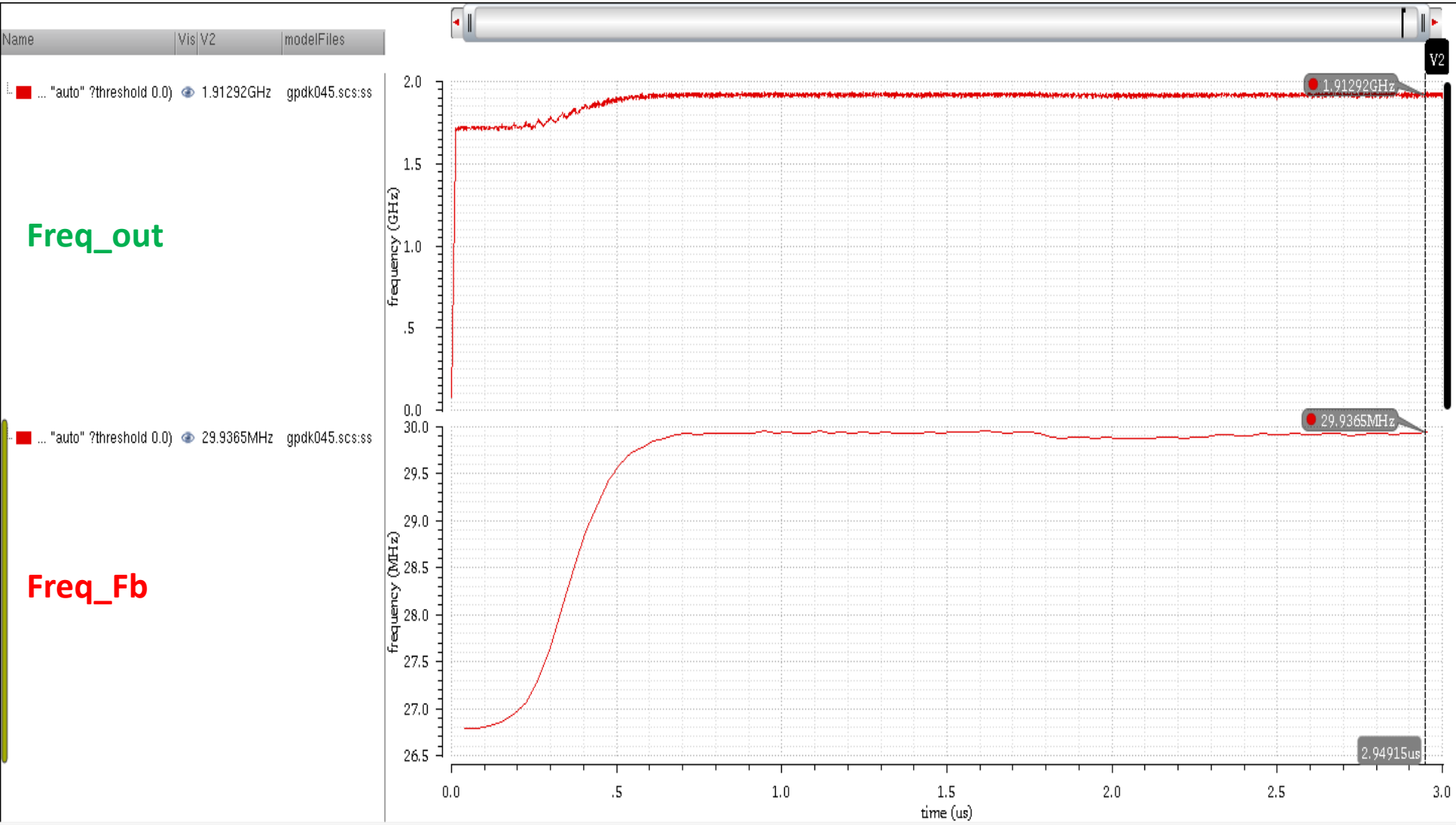
SS, 125°, 1.1 V_{DD}


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
Fb Freq
Fb Freq 30.033MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (GHz)
2.5
2.0
1.5
1.0
.5
0.0
1.91599GHz
frequency (MHz)
31
30
29
28
27
26
30.077MHz
2.92us
0.0
.5
1.0
1.5
2.0
2.5
3.0
time (us)

SS, -40°, 0.9 V_{DD}


Fb Freq
Sat Dec 1 21:30:02 2018
V1
Out Freq
Out Freq 1.91964GHz nom 27 1
Out Freq 1.91599GHz ..._7 ... 1.1
Out Freq 1.94609GHz ..._5 ... 0.9
Out Freq 1.92393GHz ..._4 ... 0.9
Out Freq 1.91599GHz ..._3 ... 1.1
Out Freq 1.94609GHz ..._1 ... 0.9
Out Freq 1.92393GHz ..._0 ... 0.9
Freq_out
Fb Freq
Fb Freq 30.033MHz nom 27 1
Fb Freq 30.077MHz ..._7 ... 1.1
Fb Freq 30.054MHz ..._5 ... 0.9
Fb Freq 30.015MHz ..._4 ... 0.9
Fb Freq 30.077MHz ..._3 ... 1.1
Fb Freq 30.054MHz ..._1 ... 0.9
Fb Freq 30.015MHz ..._0 ... 0.9
Freq_Fb
frequency (GHz)
2.5
2.0
1.5
1.0
.5
0.0
1.92393GHz
frequency (MHz)
31
30
29
28
27
26
30.015MHz
2.92us
0.0
.5
1.0
1.5
2.0
2.5
3.0
time (us)

SS, -40°, 1.1 V_{DD}


Name
Vis
V2
modelFiles
... "auto" ?threshold 0.0)
1.91292GHz
gpdk045.scs:ss
Freq_out
... "auto" ?threshold 0.0)
29.9365MHz
gpdk045.scs:ss
Freq_Fb
V2
1.91292GHz
29.9365MHz
2.94915us
frequency (GHz)
frequency (MHz)
time (us)
2.0
1.5
1.0
.5
0.0
30.0
29.5
29.0
28.5
28.0
27.5
27.0
26.5
0.0
.5
1.0
1.5
2.0
2.5
3.0

(7) Summary

- Our work shows a comparison between a CP-PLL using a **Ring VCO** & another using an **LC VCO**:
  - The Ring VCO gives a higher KVCO, which affects the PLL's stability & gives a higher jitter than that in the LC VCO.
  - Using the LC VCO, we were able to achieve a low RMS jitter with a reasonable power dissipation, achieving the required FOM.

- In our corners' analysis:
  - The range of the output frequency after the PLL locks is between **1.916 GHz & 1.946 GHz**.
  - The range of the feedback frequency after the PLL locks is between **30.015 MHz & 30.077 MHz**.