EE230 Homework #3 (10 points) Oct. 30, 2018

Due: Nov. 20, 2018 4:00PM
Late homework policy. 1-point deduction for each day you miss the due date.
Extra 1-point credit for the student who submitted homework first.

For this homework, you will be modeling the Type-II Charge Pump PLL in a behavioral language. Take the PLL spec of the final project and implement the PLL behavior in Verilog-A or Verilog-AMS.

The behavioral simulation results should show the correct operation of the PLL having the following specification.

- VDD = 1V
- Reference clock 30MHz
- VCO frequency 1.9 GHz

Additionally, you are required to implement a MATLAB code to check the stability of the PLL based on the 2nd order loop filter (R-C1 // C2).

For full score, please submit the followings:

1. Schematic of the PLL you used to verify the Verilog codes
2. Verilog code for each block of the PLL and the simulation results
3. MATLAB code to check the stability of the PLL and the simulation result

File name should be EE230HW#3_Lastname_Firstname.pdf.

Also, the first page of the pdf file should include your name. Otherwise, 1-point deduction.

Please submit just one pdf file to sang-soo.lee@sjsu.edu. No Zip file or image files please!