ECEN620: Network Theory Broadband Circuit Design Fall 2018

Lecture 6: Loop Filter Circuits

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Announcements

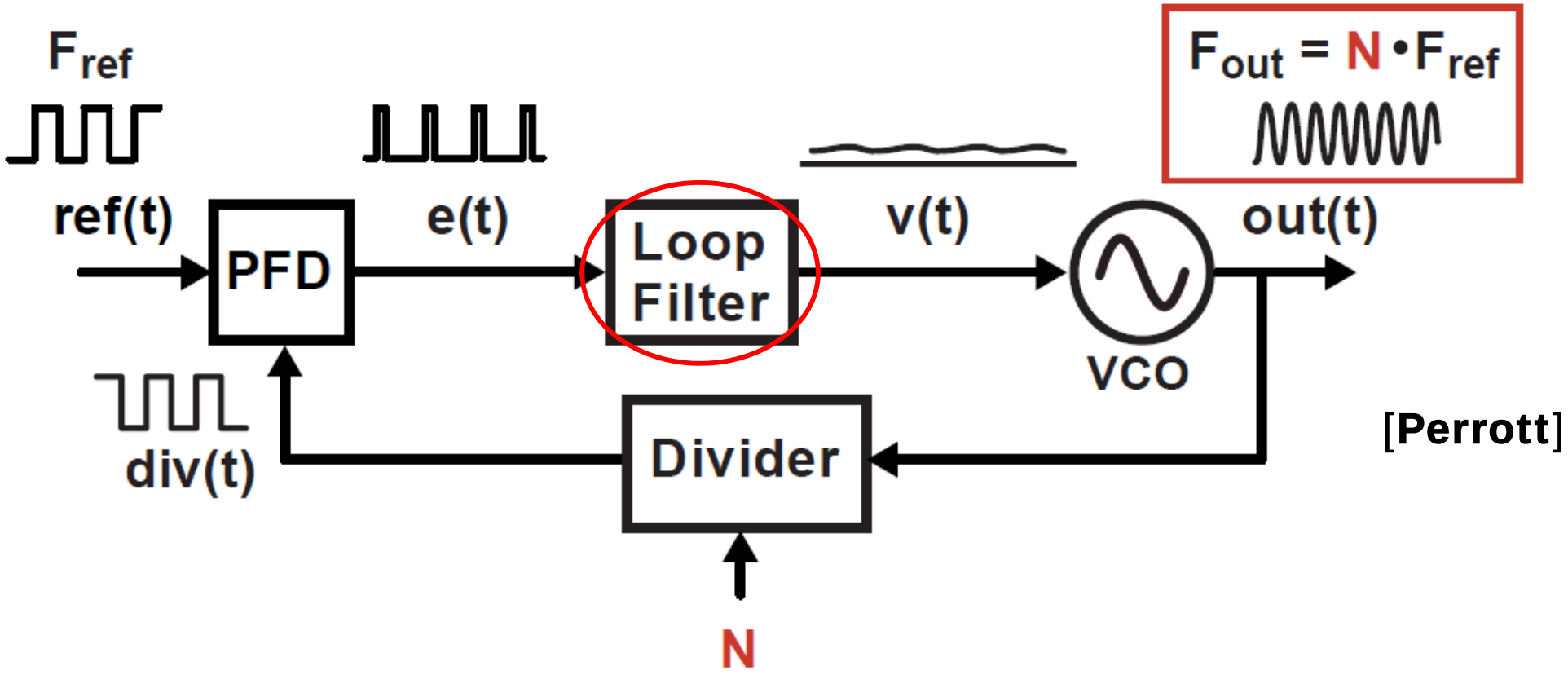
- HW2 is due Oct 11
  - Requires transistor-level design
  - For 90nm CMOS device models, see http://www.ece.tamu.edu/~spalermo/ecen689/cadence_90nm.pdf
  - Can use other technology models if they are a 130nm or more advanced CMOS node

Agenda

- Loop filter circuits
  - Voltage-mode filters
  - Charge-Pump PLL PI filter
  - Filter with capacitive multiplier
  - Split Proportional & Integral Path Filters
  - Pattern Jitter
  - Sample-Reset Loop Filter

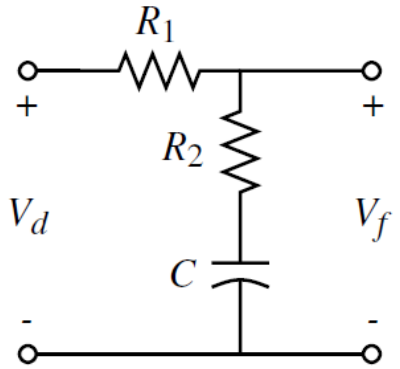
- Some loop filter papers are posted on the website

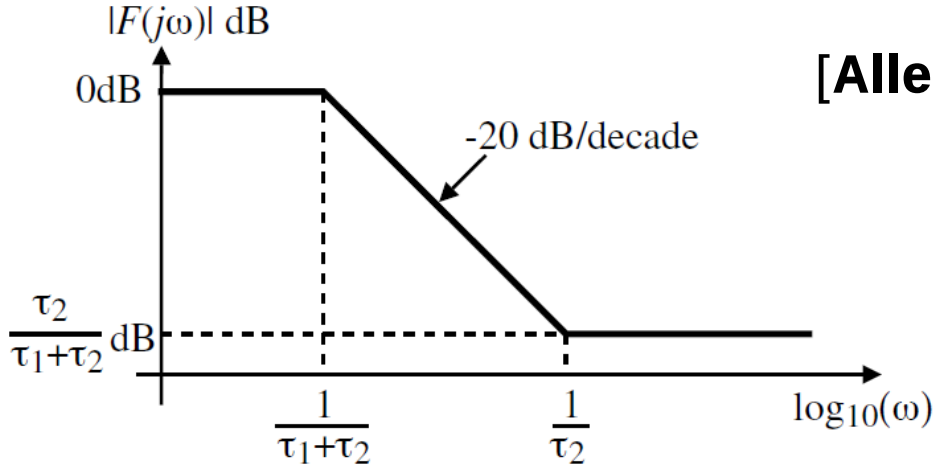
PLL Block Diagram



- The lowpass loop filter extracts the average of the phase detector error pulses in order to produce the VCO control voltage

Passive Lag-Lead Filter





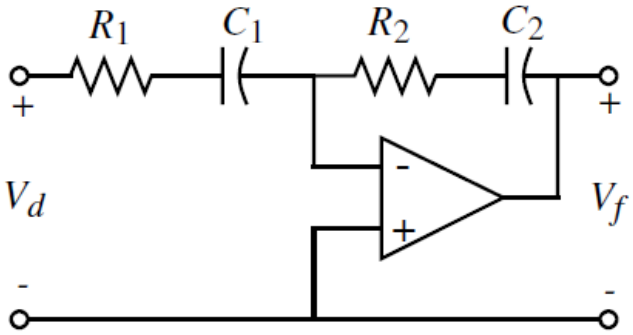
[Allen]

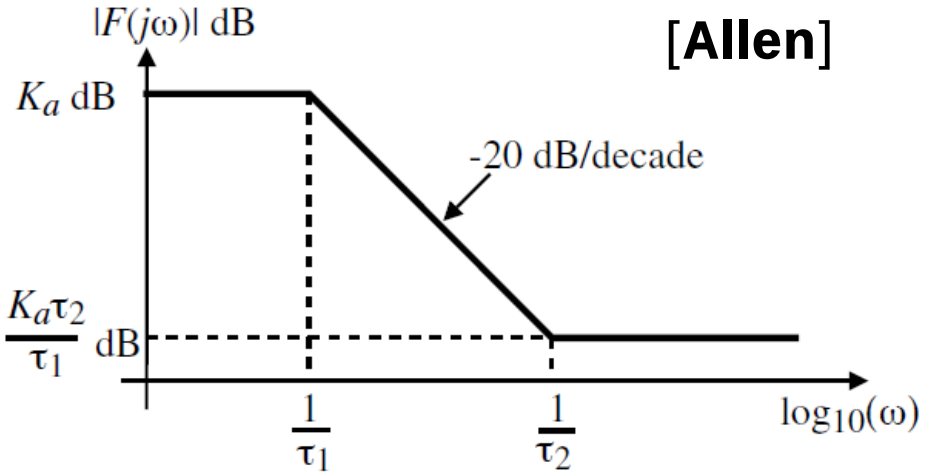
$$F(s)=\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}$$

$$\tau_1 = R_1C \qquad \tau_2 = R_2C$$

- Dimensionless voltage-mode filter used in Type-1 PLLs
- Called lag-lead because the pole is at a lower frequency than the zero
- Ideally, the passive filter displays no nonlinearity

Active Lag-Lead Filter





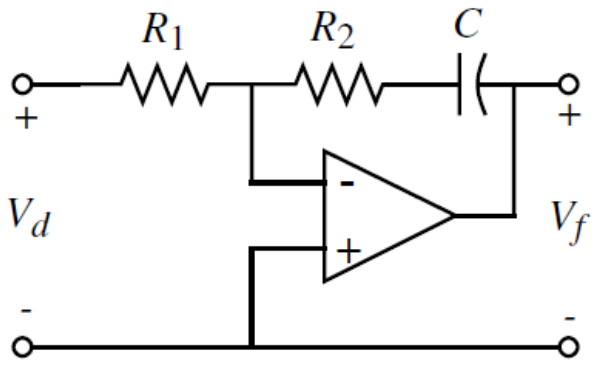
[Allen]

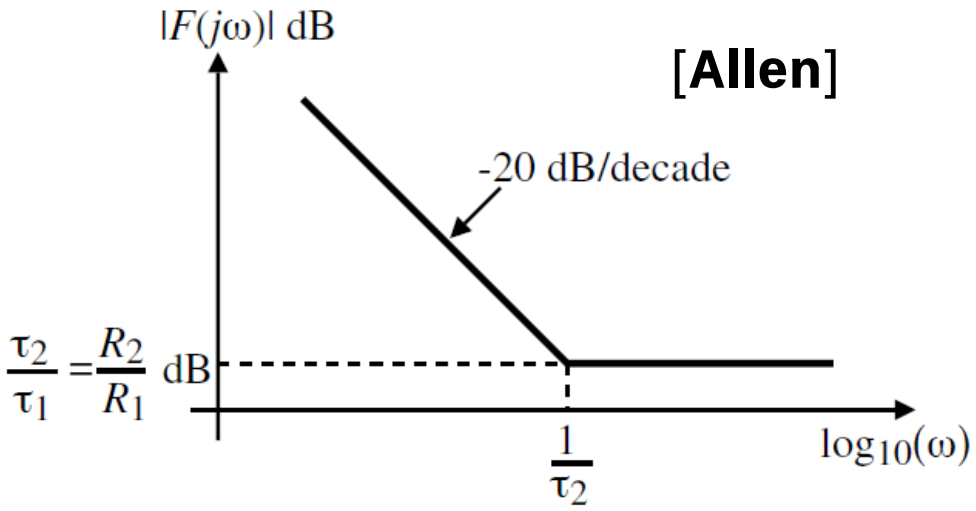
$$F(s) = K_a \frac{1+s\tau_2}{1+s\tau_1}$$

$$\tau_1 = R_1 C \qquad \tau_2 = R_2 C \qquad K_a = -\frac{C_1}{C_2}$$

- Dimensionless voltage-mode filter used in Type-1 PLLs
- Active filter allows for potential gain in the loop filter
- Opamp noise and linearity can impact PLL performance

Active Proportional-Integral (PI) Filter





$$F(s) = -\frac{1 + s\tau_2}{s\tau_1}$$

$$\tau_1 = R_1 C \qquad \tau_2 = R_2 C$$

- Dimensionless voltage-mode filter used in Type-2 PLLs
- Opamp noise and linearity can impact PLL performance
- Opamp open loop gain limits the low-frequency gain and ideal transfer function

Closed-Loop Transfer Functions

Passive Lag - Lead Filter

$$F(s)=\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)} \rightarrow H(s)=\frac{\frac{K_{PD}K_{VCO}\tau_2}{\tau_1+\tau_2}\left(s+\frac{1}{\tau_2}\right)}{s^2+\left(\frac{1+K_{PD}K_{VCO}\tau_2/N}{\tau_1+\tau_2}\right)s+\frac{K_{PD}K_{VCO}}{N(\tau_1+\tau_2)}}$$

$$\omega_n=\sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1+\tau_2)}} \quad \zeta=\frac{\omega_n}{2}\left(\tau_2+\frac{N}{K_{PD}K_{VCO}}\right)$$

Active Lag - Lead Filter (Assuming Overall Negative Feedback)

$$F(s)=K_a\frac{1+s\tau_2}{1+s\tau_1} \rightarrow H(s)=\frac{\frac{K_{PD}K_aK_{VCO}\tau_2}{\tau_1}\left(s+\frac{1}{\tau_2}\right)}{s^2+\left(\frac{1+K_{PD}K_aK_{VCO}\tau_2/N}{\tau_1}\right)s+\frac{K_{PD}K_aK_{VCO}}{N\tau_1}}$$

$$\omega_n=\sqrt{\frac{K_{PD}K_aK_{VCO}}{N\tau_1}} \quad \zeta=\frac{\omega_n}{2}\left(\tau_2+\frac{N}{K_{PD}K_aK_{VCO}}\right)$$

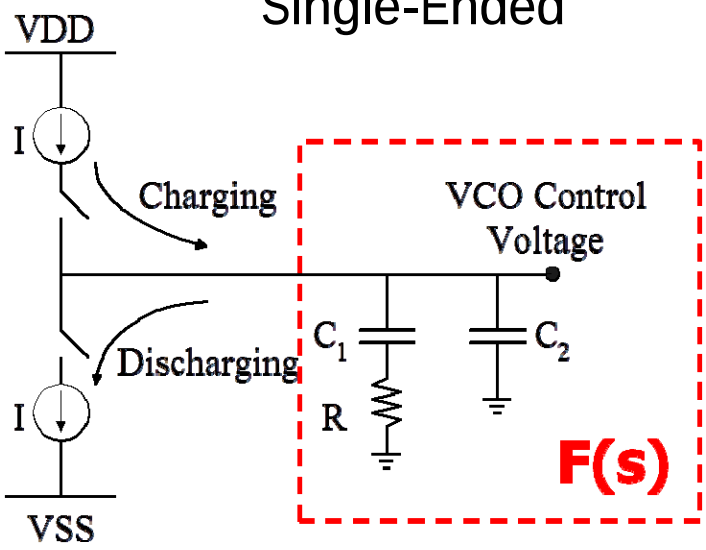
Active PI Filter (Assuming Overall Negative Feedback)

$$F(s)=-\frac{1+s\tau_2}{s\tau_1} \rightarrow H(s)=\frac{\frac{K_{PD}K_{VCO}\tau_2}{\tau_1}\left(s+\frac{1}{\tau_2}\right)}{s^2+\left(\frac{K_{PD}K_{VCO}\tau_2}{N\tau_1}\right)s+\frac{K_{PD}K_{VCO}}{N\tau_1}}$$

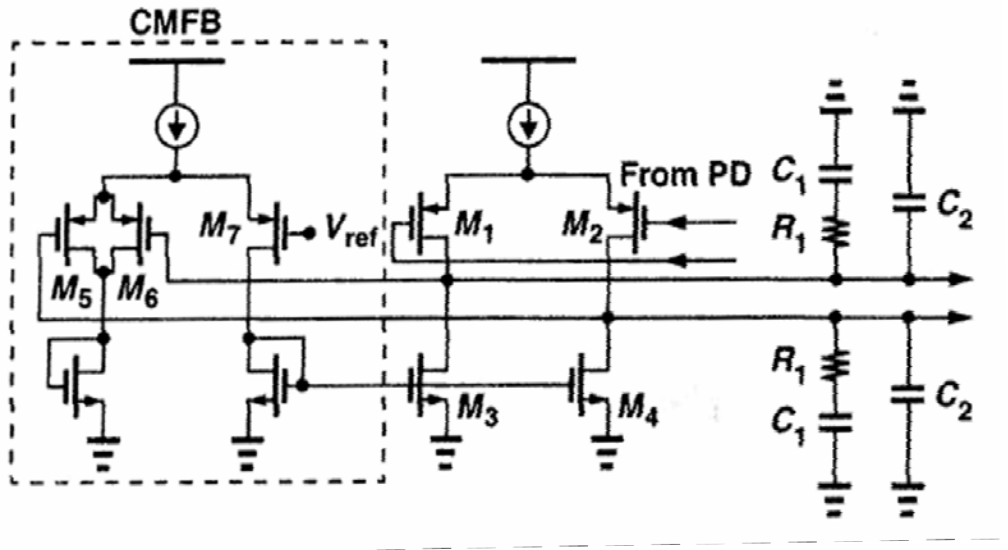
$$\omega_n=\sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}} \quad \zeta=\frac{\omega_n}{2}\tau_2$$

Charge Pump PLL Passive PI Loop Filter

Single-Ended



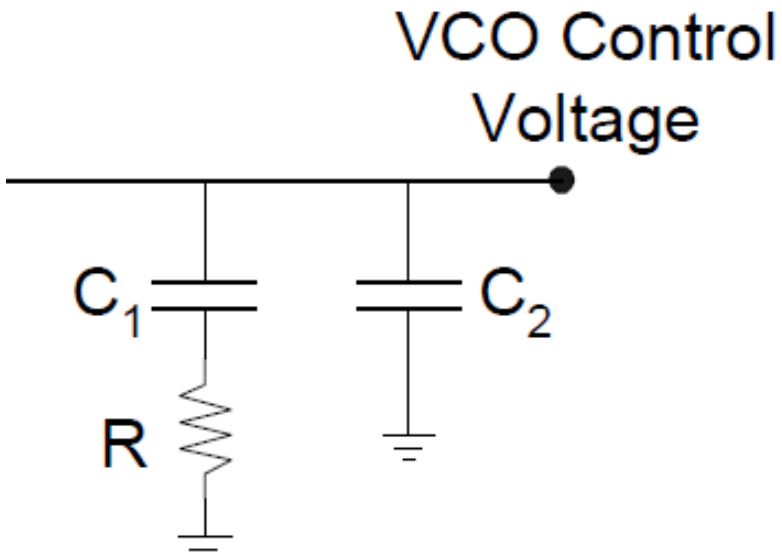
Fully Differential



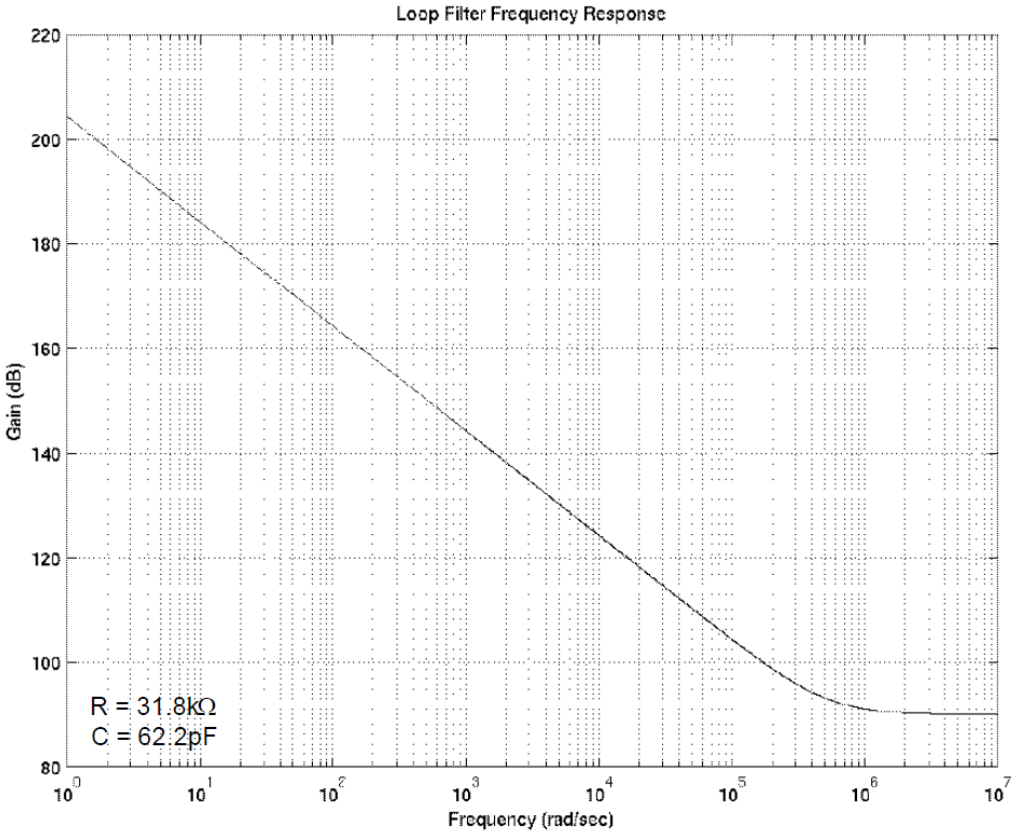
- Simple passive filter is most commonly used
- Integrates low-frequency phase errors onto C1 to set average frequency
- Resistor (proportional gain) isolates phase correction from frequency correction
- Primary capacitor C1 affects PLL bandwidth
- Zero frequency affects PLL stability
- Resistor adds thermal noise which is band-pass filtered by PLL

Loop Filter Transfer Function

- Neglecting secondary capacitor, C_2

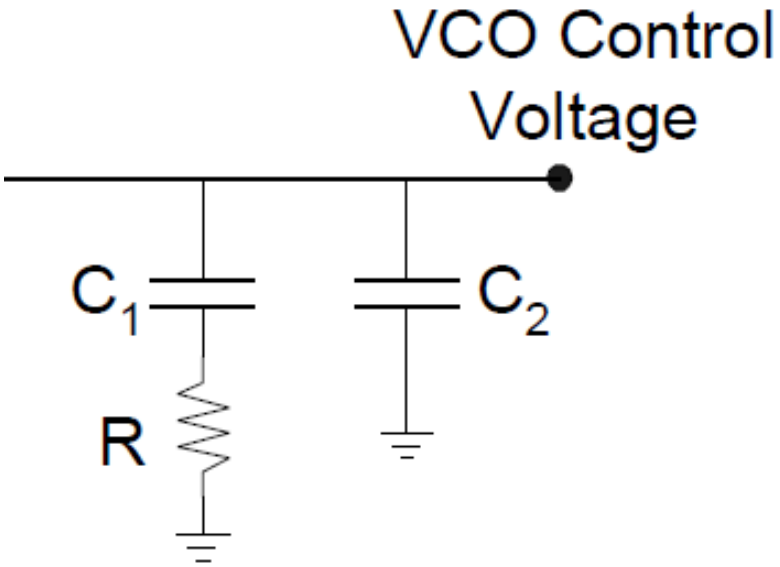


$$F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R\left(s + \frac{1}{RC_1}\right)}{s}$$

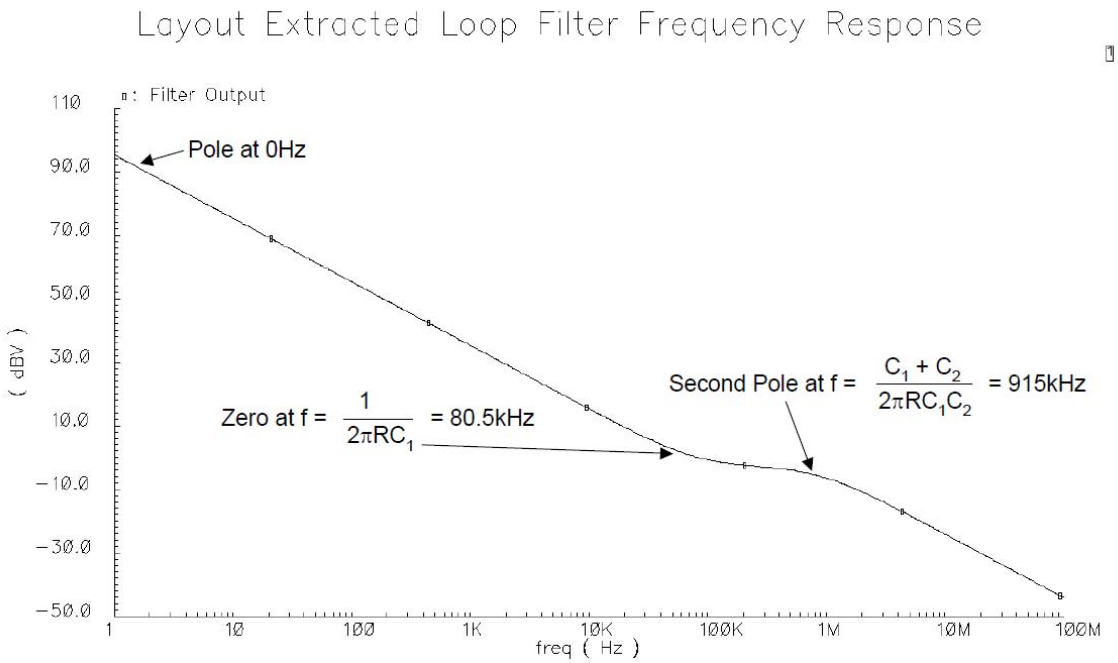


Loop Filter Transfer Function

- With secondary capacitor, C_2

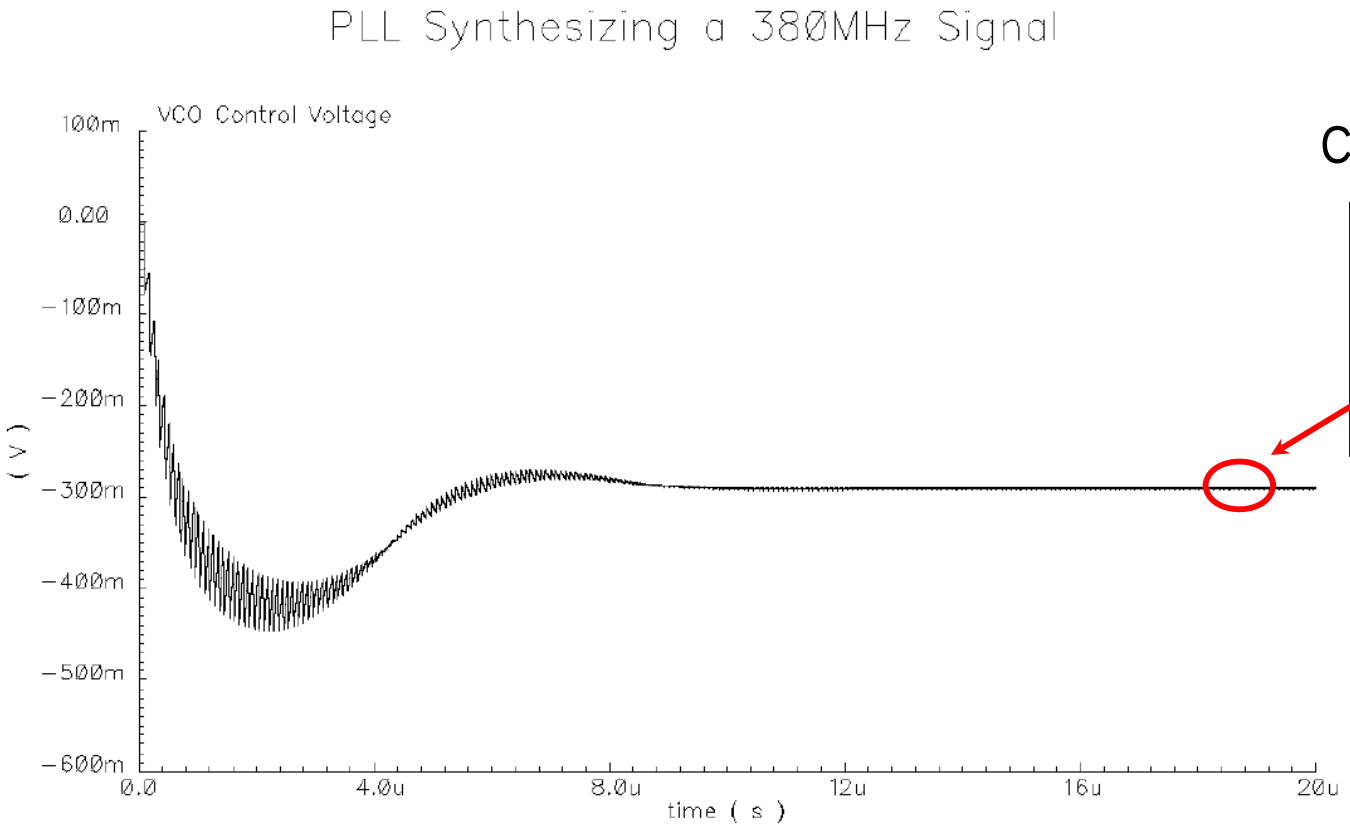


$$Z(s) = \frac{\frac{1}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^2 + \frac{s(C_1 + C_2)}{RC_1C_2}}$$

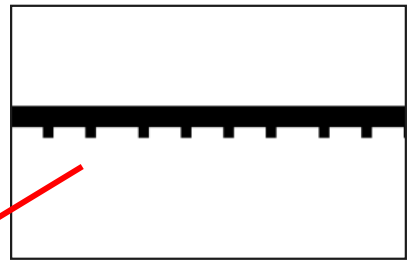


Why have C_2?

- Secondary capacitor smoothes control voltage ripple
- Can't make too big or loop will go unstable
  - $C_2 < C_1/10$ for stability
  - $C_2 > C_1/50$ for low jitter

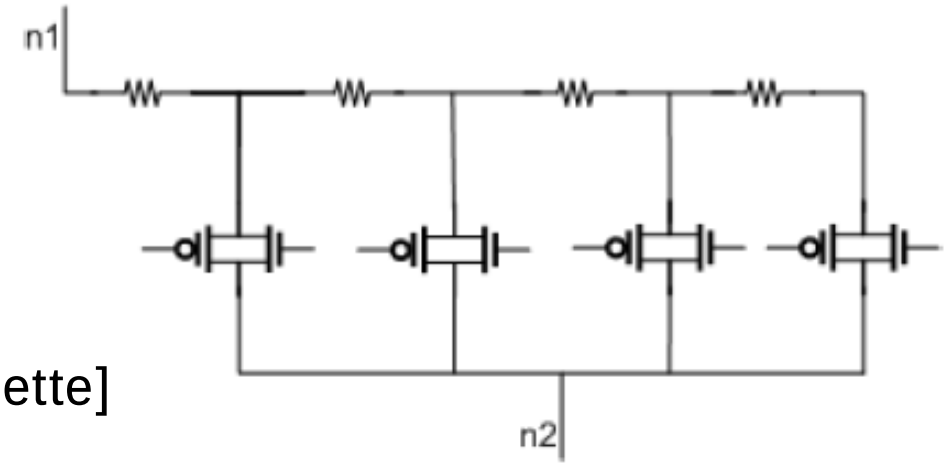


Control Voltage Ripple



Loop Filter Resistors

- Poly, diffusion, and N-well resistors are commonly used
- MOSFET resistors can be used if the resistor is placed "below" the C1 cap
  - This ensures a constant V_{GS} voltage on the transistor
- Programmable R value possible with switches
  - Switches should be CMOS transmission gates to minimize parasitic switch resistance variation with control voltage level
  - Good practice is to make Rswitch <10% of the main filter R to minimize the impact of switch resistatnce variations

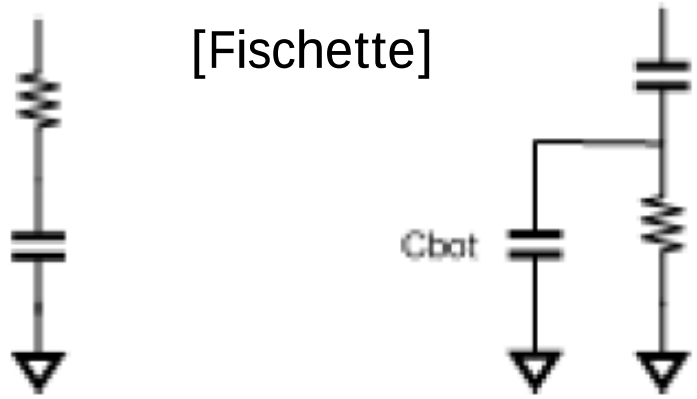


[Fischette]

R or C on Top?

- Ideally, the loop filter has the same transfer function and transient response independent of the RC order
- In reality, the bottom-plate capacitance and switch resistance variation will impact this ideal transfer function
- If the cap is on top, the bottom-plate capacitance will introduce another high frequency pole
- If the resistor is on top, any switch resistance will have increased variation with the control voltage level

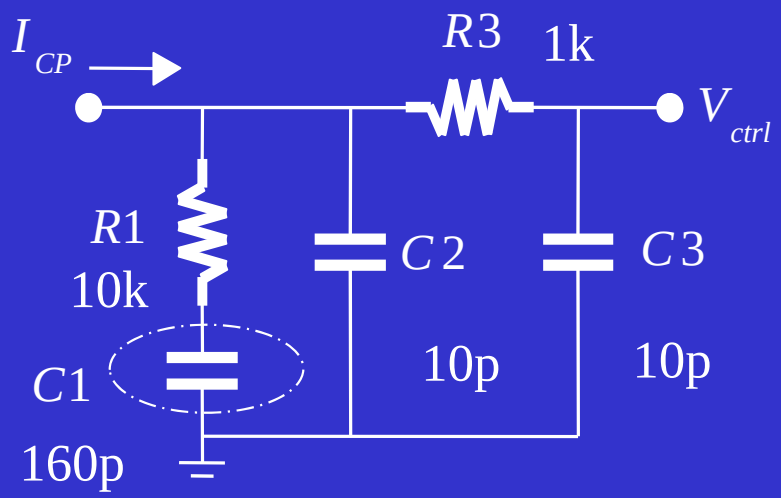
[Fischette]



Loop Filter Capacitors

- To minimize area, we would like to use highest density caps
- Thin oxide MOS cap gate leakage can be an issue
  - Similar to adding a non-linear parallel resistor to the capacitor
  - Leakage is voltage and temperature dependent
  - Will result in excess phase noise and spurs
- Metal caps or thick oxide caps are a better choice
  - Trade-off is area
- Metal cap density can be <1/10 thin oxide caps
- Filter cap frequency response can be relatively low, as PLL loop bandwidths are typically 1-50MHz

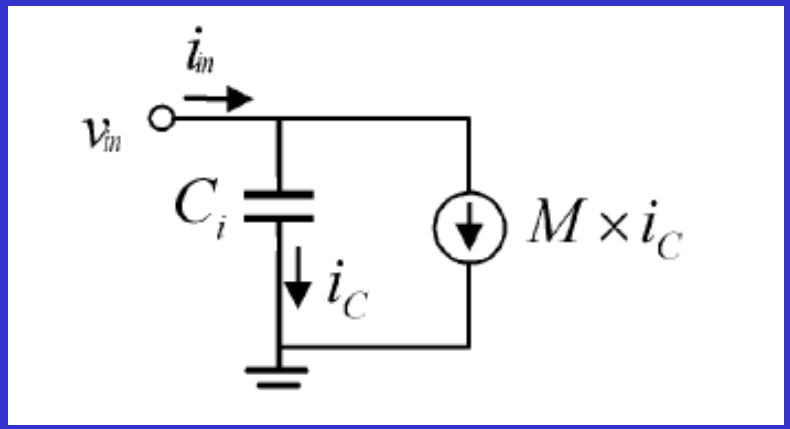
Third-Order Loop Filter

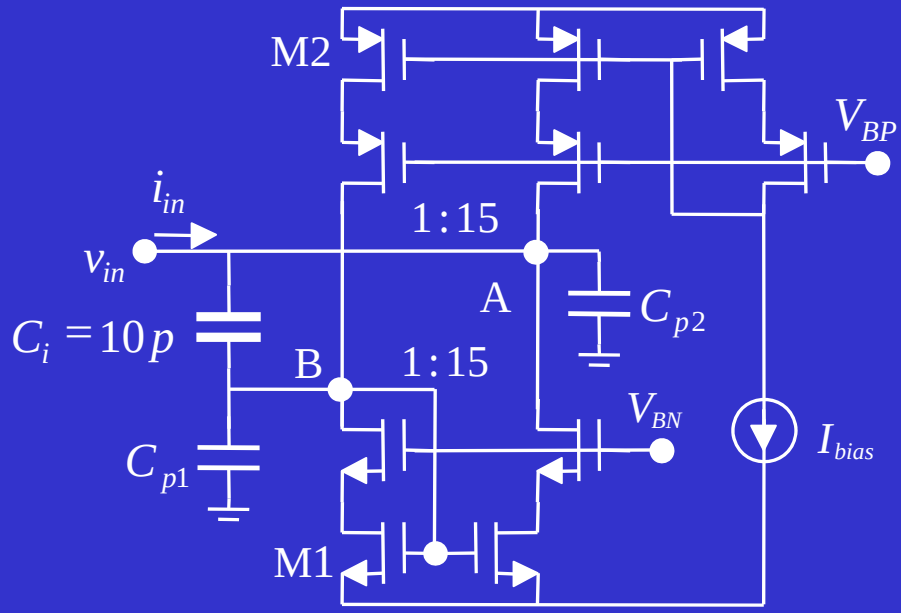


[Shu JSSC 2003]

The 160pF capacitance in TSMC 0.35um CMOS takes about 0.2mm^2. To reduce its area, it is implemented via a 10pF capacitor scaled up by a factor of 16.

Capacitor Multiplier



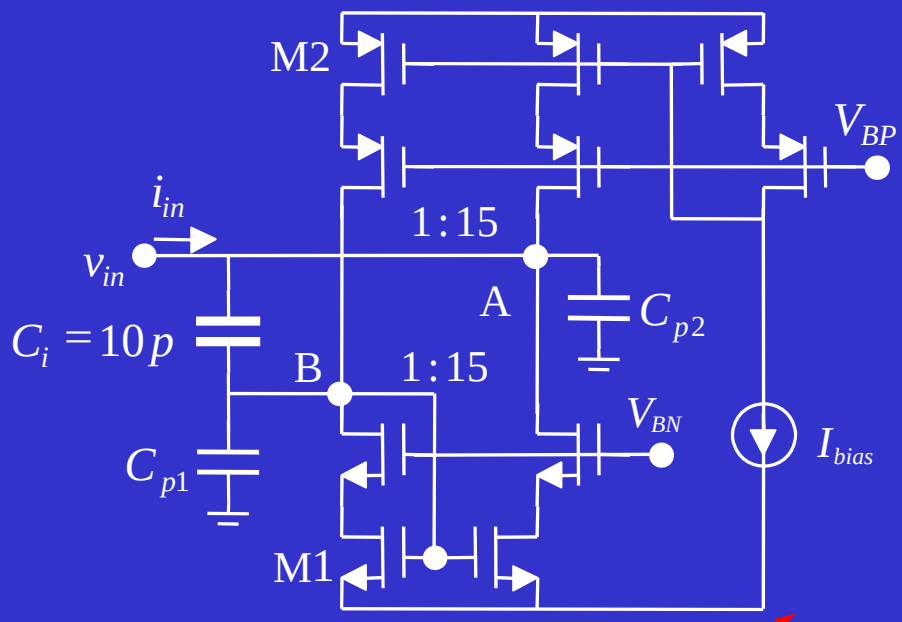


Current ratio M=15

Capacitance ×16

Capacitor Multiplier Transfer Function

$$y_{\text{in}} = \frac{i_{\text{in}}}{v_{\text{in}}} = g_{oA} + s\left[C_{p2} + (M+1)C_i \frac{1 + s\frac{C_{p1}}{(M+1)g_{m1}}}{1 + s\frac{C_i + C_{p1}}{g_{m1}}}\right]. \quad (7)$$



Looking at the impedance, we get 2 poles and a zero

ω_{c1} and ω_{c3} are poles, ω_{c2} is a zero

Low freq. pole (ideally at 0)

$$\omega_{c1} = \frac{g_{oA}}{C_{p2} + (M+1)C_i} \approx \frac{g_{oA}}{C_1}$$

High freq. zero (ideally at ∞)

$$\omega_{c2} = \frac{g_{m1}}{(C_i + C_{p1})} \approx \frac{(M+1)g_{m1}}{C_1}$$

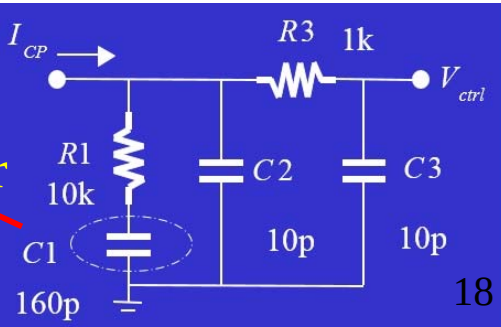
High freq. pole (ideally at ∞)

$$\omega_{c3} = \frac{(M+1)g_{m1}}{C_{p1}}.$$

Current ratio M=15

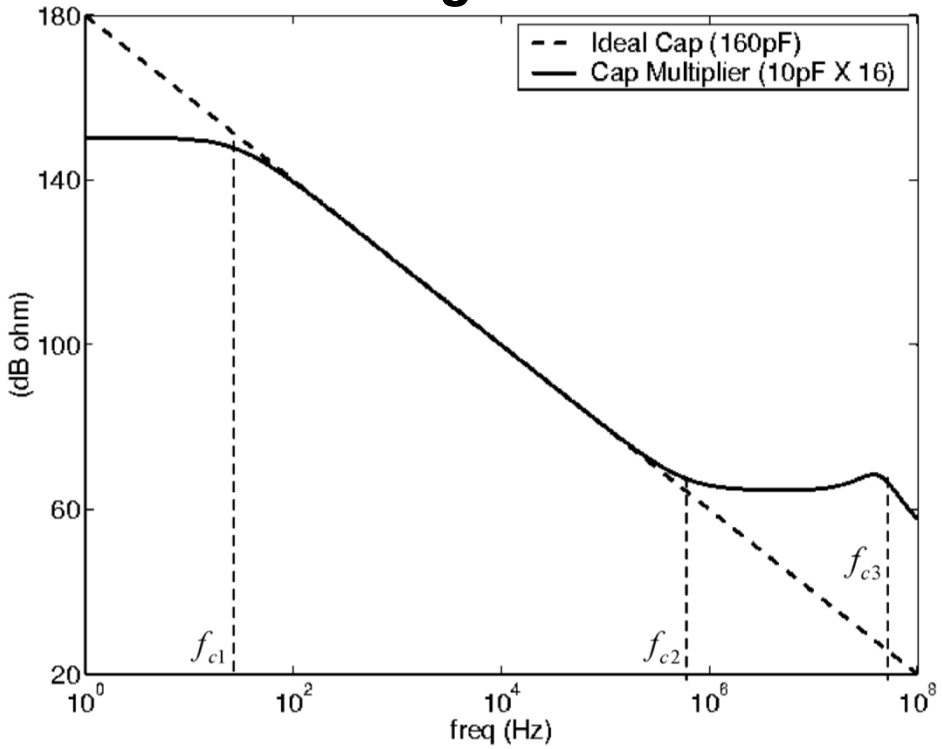
Capacitance ×16

Original Filter



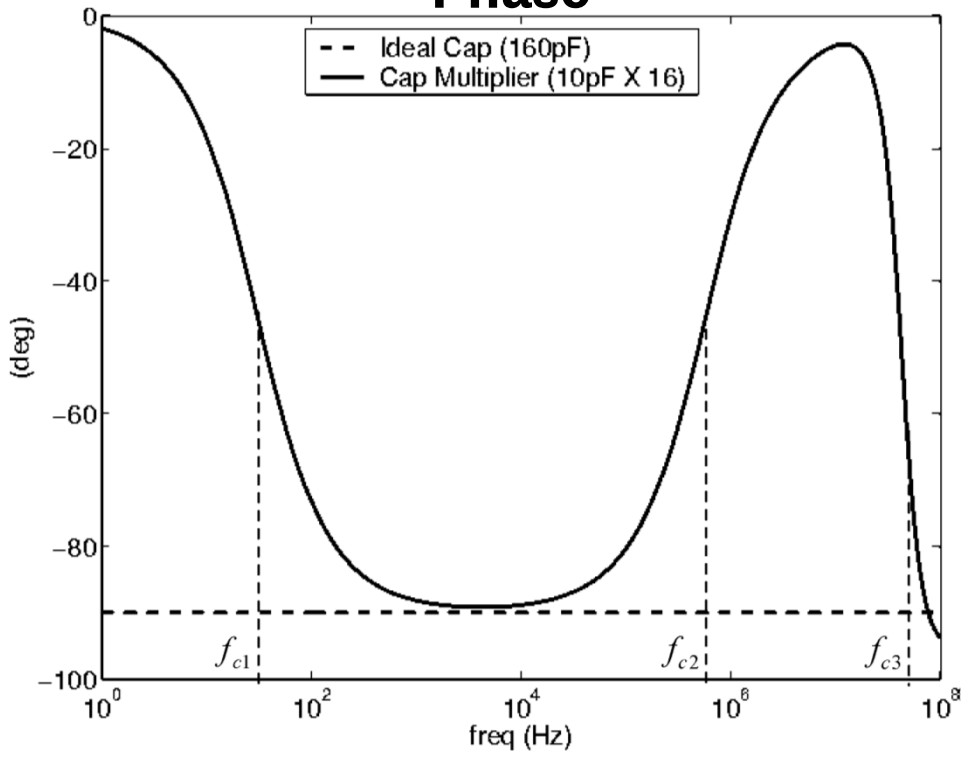
Capacitance Multiplier Impedance

Magnitude



(a)

Phase



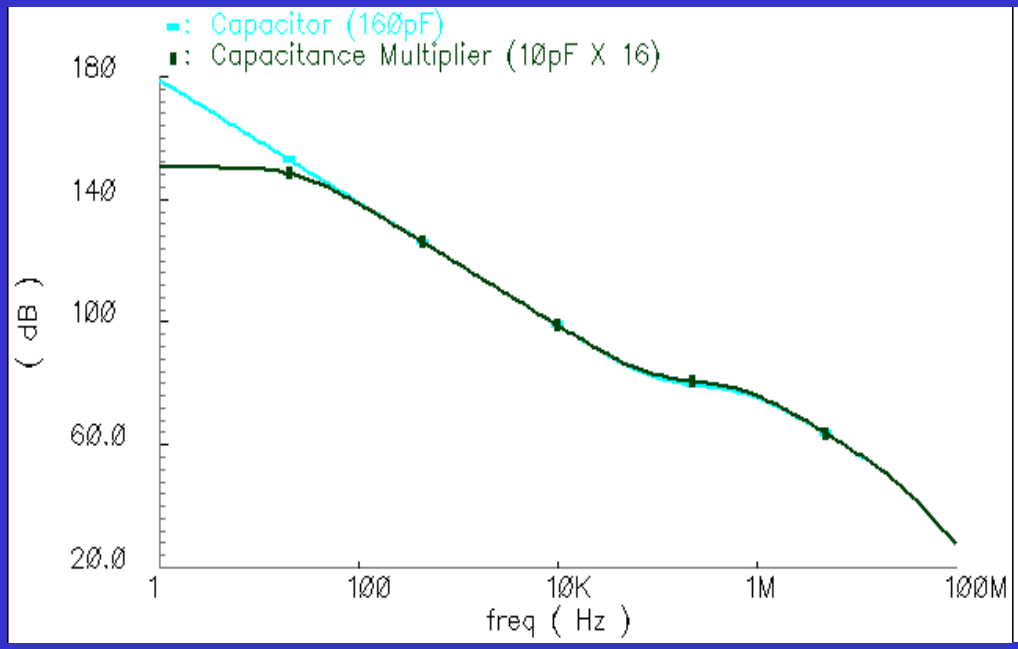
(b)

$$\omega_{c1} = \frac{g_{oA}}{C_{p2} + (M+1)C_i} \approx \frac{g_{oA}}{C_1}$$ (dominant pole)

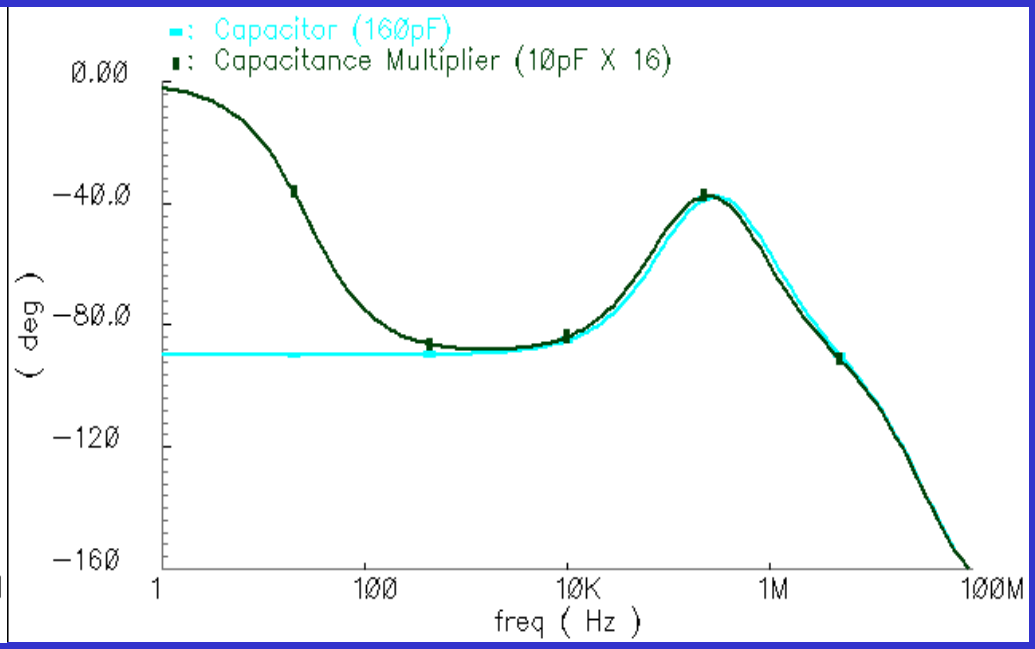
$$\omega_{c2} = \frac{g_{m1}}{(C_i + C_{p1})} \approx \frac{(M+1)g_{m1}}{C_1}$$ (high frequency zero)

$$\omega_{c3} = \frac{(M+1)g_{m1}}{C_{p1}}.$$ (high frequency pole)

Loop Filter Sim. w/ Capacitance Multiplier



(a) magnitude

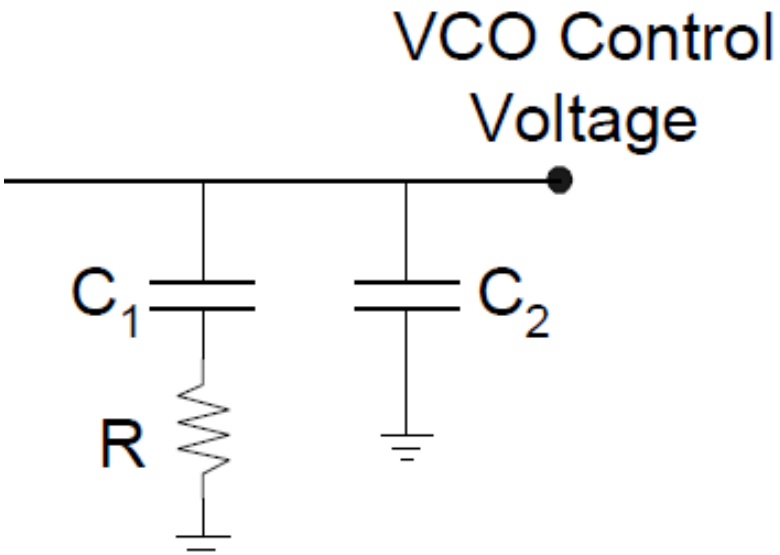


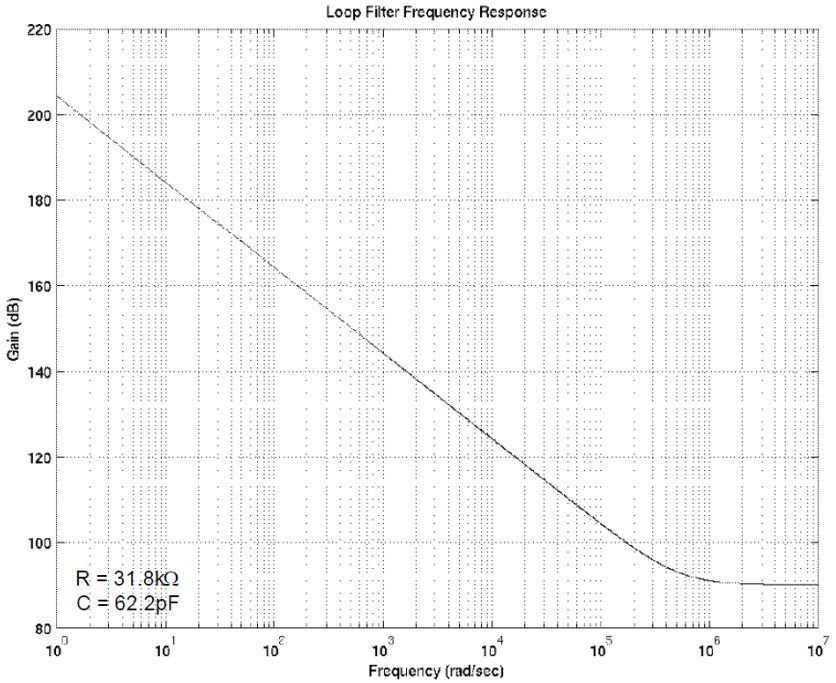
(b) phase

- It shows that with capacitance scaling the large capacitor in the loop filter can be easily integrated on chip within small area
- This approach is simple and the leakage is very small

Loop Filter Transfer Function

- Neglecting secondary capacitor, C_2





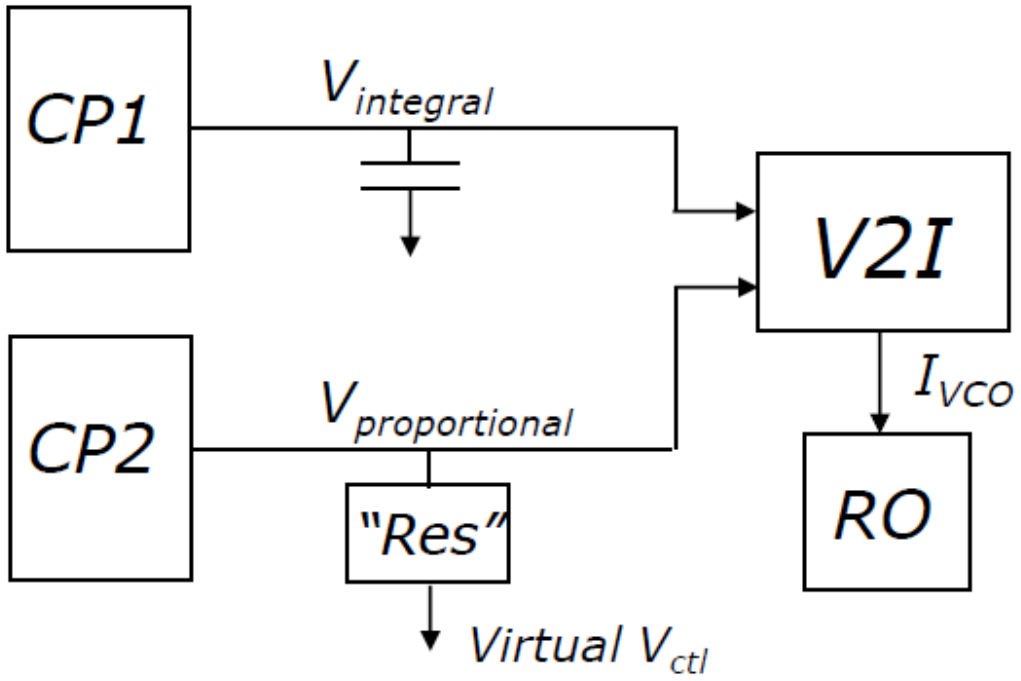
$$F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R\left(s + \frac{1}{RC_1}\right)}{s} = R + \frac{1}{sC_1}$$

Proportional term

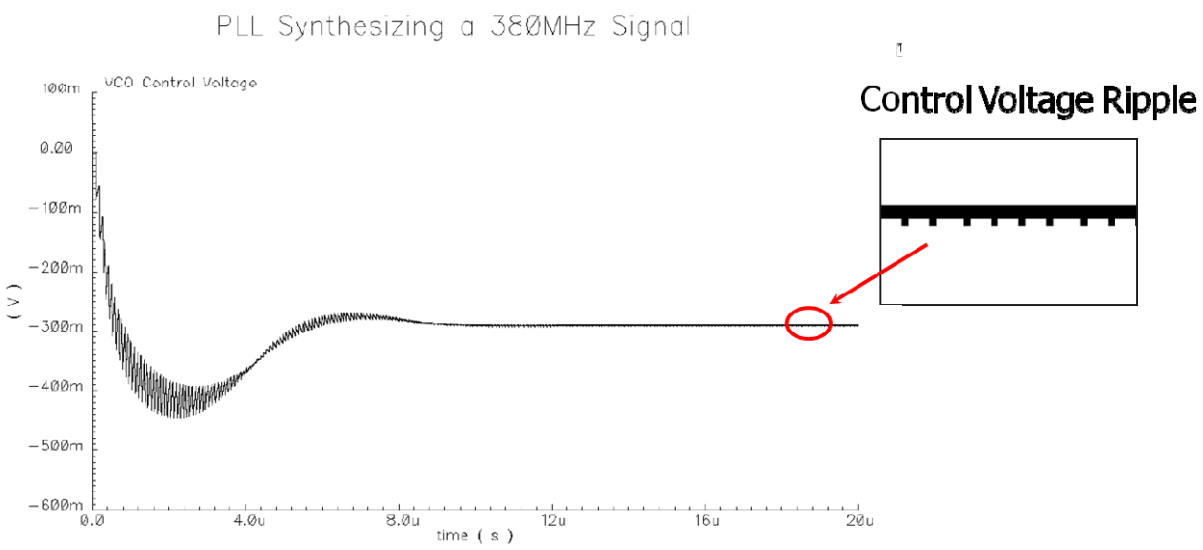
Integral term

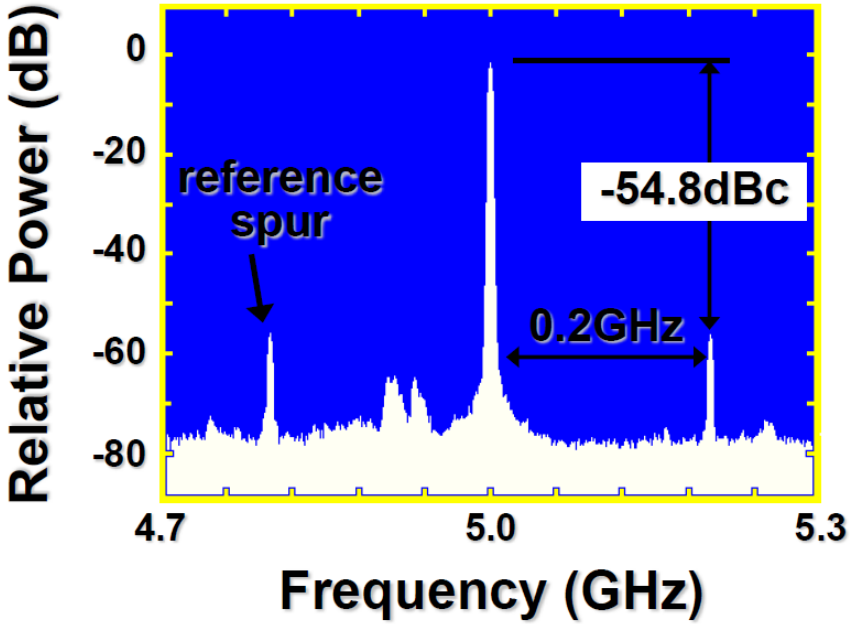
Split Proportional & Integral Gain Path

- Proportional and integral gain paths can be split by utilizing 2 independent charge pumps driving the integral capacitor and the proportional effective resistor
- Often, the proportional and integral voltages are summed with a voltage-to-current converter to control a current-controlled oscillator (ICO)
  - Allows for self-biased PLL architectures whose normalized loop bandwidth and damping factor remains constant over different output frequencies
  - We will look at these PLL architectures in more detail later



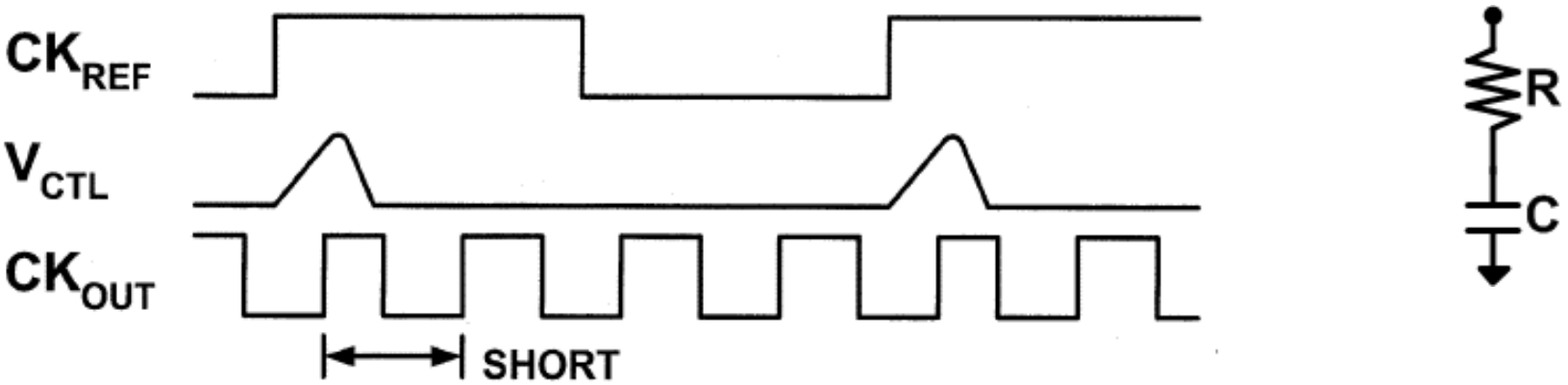
Control Voltage Ripple





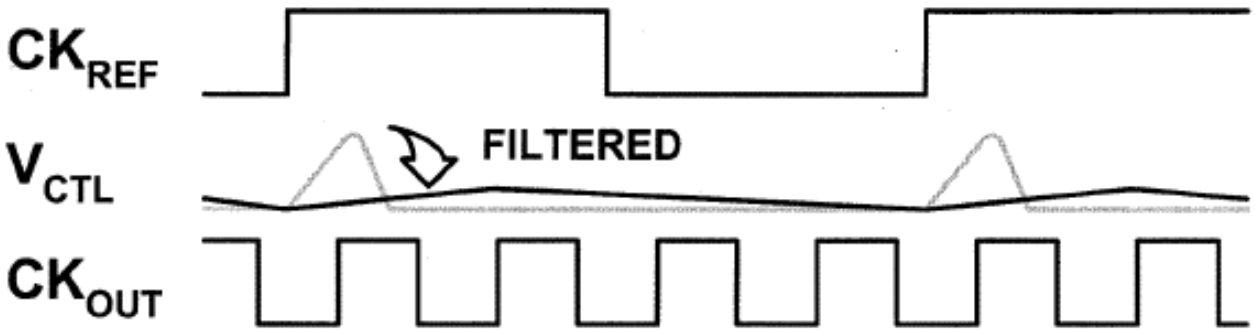
- After phase locking, disturbances at a time interval equal to the reference clock period cause time-domain period jitter and frequency-domain reference clock spurs
- Caused by charge pump current imbalance, loop filter leakage, and reference clock jitter

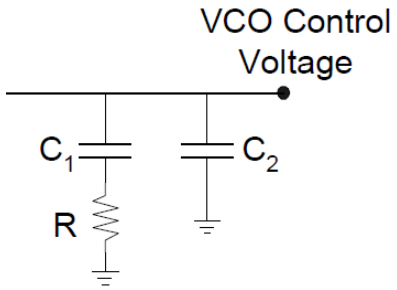
Pattern Jitter



- A dominant form of pattern jitter is due to the proportional gain term, I_{CP}*R
- Every time the reference clock goes high, charge pump mismatch current dropped on the filter resistor causes control voltage ripple
- This results in shorter (or longer) output cycles that occur at a time interval equal to the reference clock period

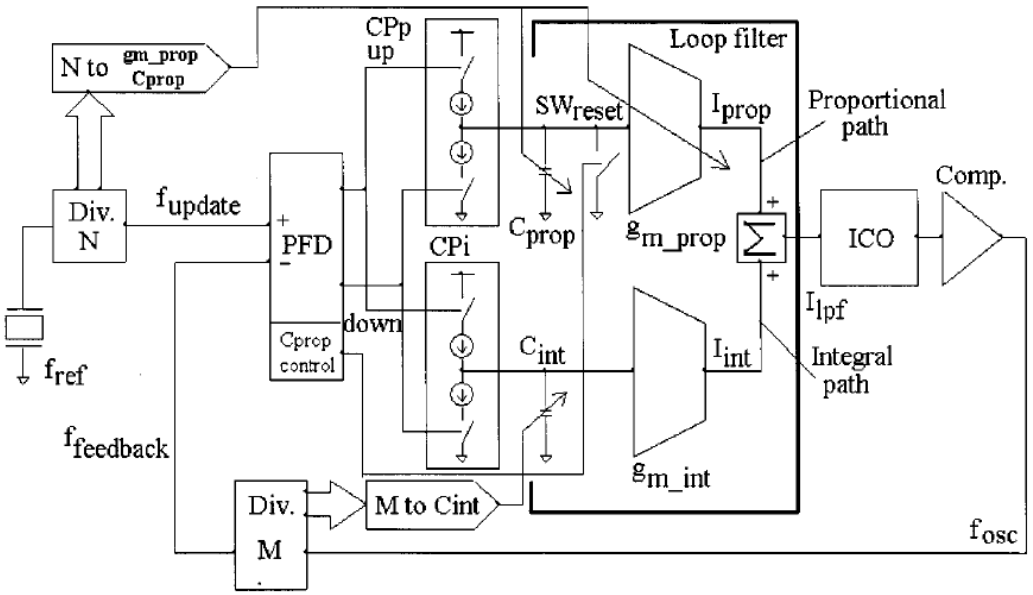
Pattern Jitter w/ Secondary Capacitor



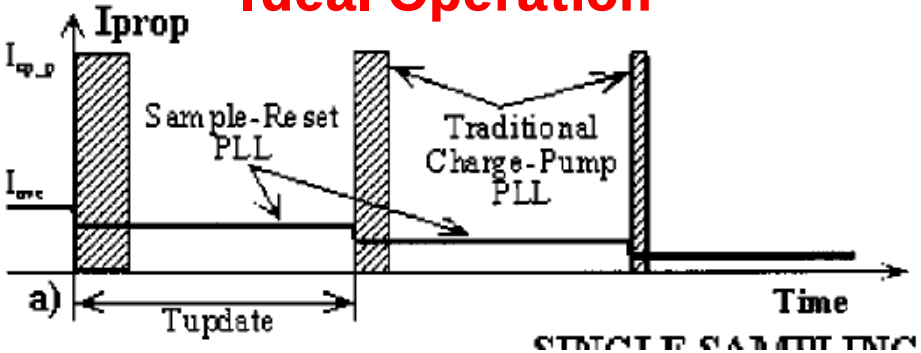


- Adding a secondary loop filter capacitor introduces extra filtering, which reduces the control voltage disturbance amplitude, but extends it over many cycles
- Makes an ideal second-order PLL into a third-order system
- Stability limits the size of C_2
- Can we get this same effect without compromising stability?

PLL w/ Sample-Reset Loop Filter

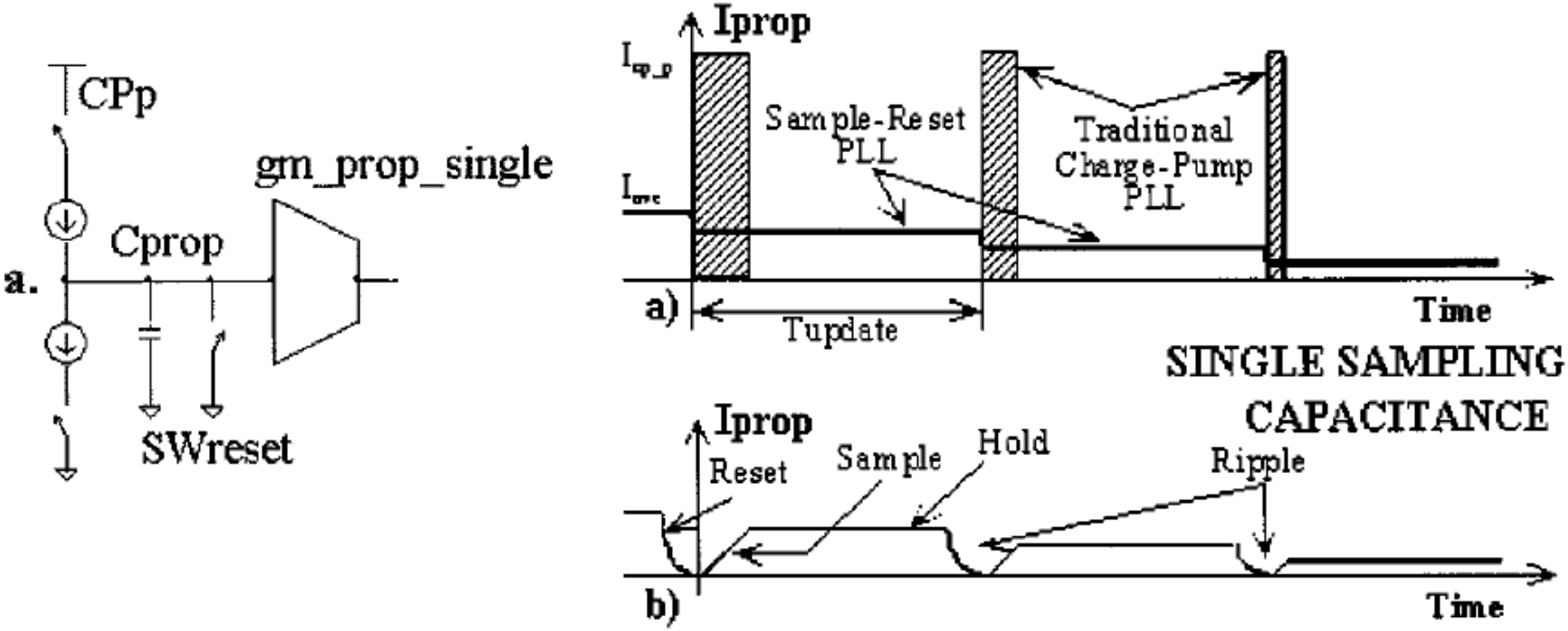


Ideal Operation



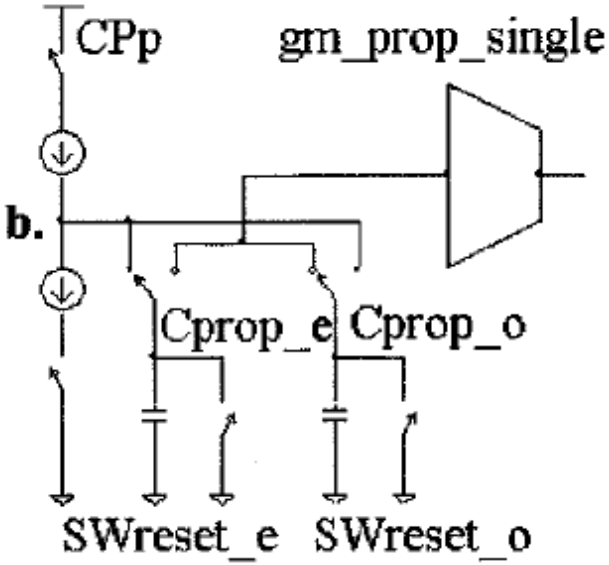
- A PLL with a standard RC filter produces a voltage spike equal to I_{CP}*R for a duration equal to the phase error
- A sample-reset loop filter replaces the resistor with a capacitor that is charged during the phase error and reset every reference cycle
- This spreads the correction voltage nearly uniformly over the entire reference period and reduces the correction voltage peak value
- This eliminates the need for additional filtering with a secondary capacitor, providing the opportunity for near 90° phase margin

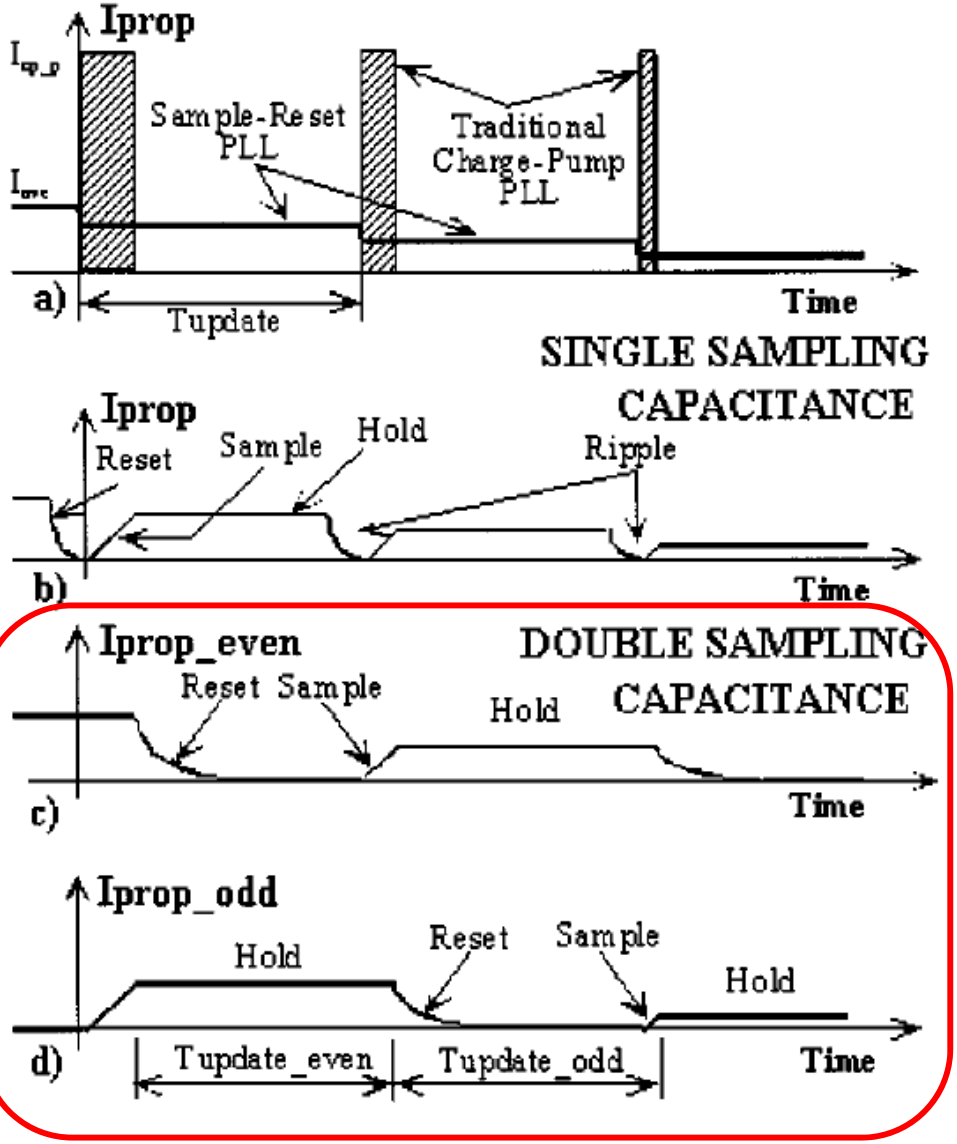
Sample-Reset Loop Filter w/ Single Capacitor



- A single-capacitor implementation still has a (reduced) ripple component due to the sample, hold, and reset operation
- Also, a very short reset pulse needs to be generated, which may be difficult to realize with the control logic

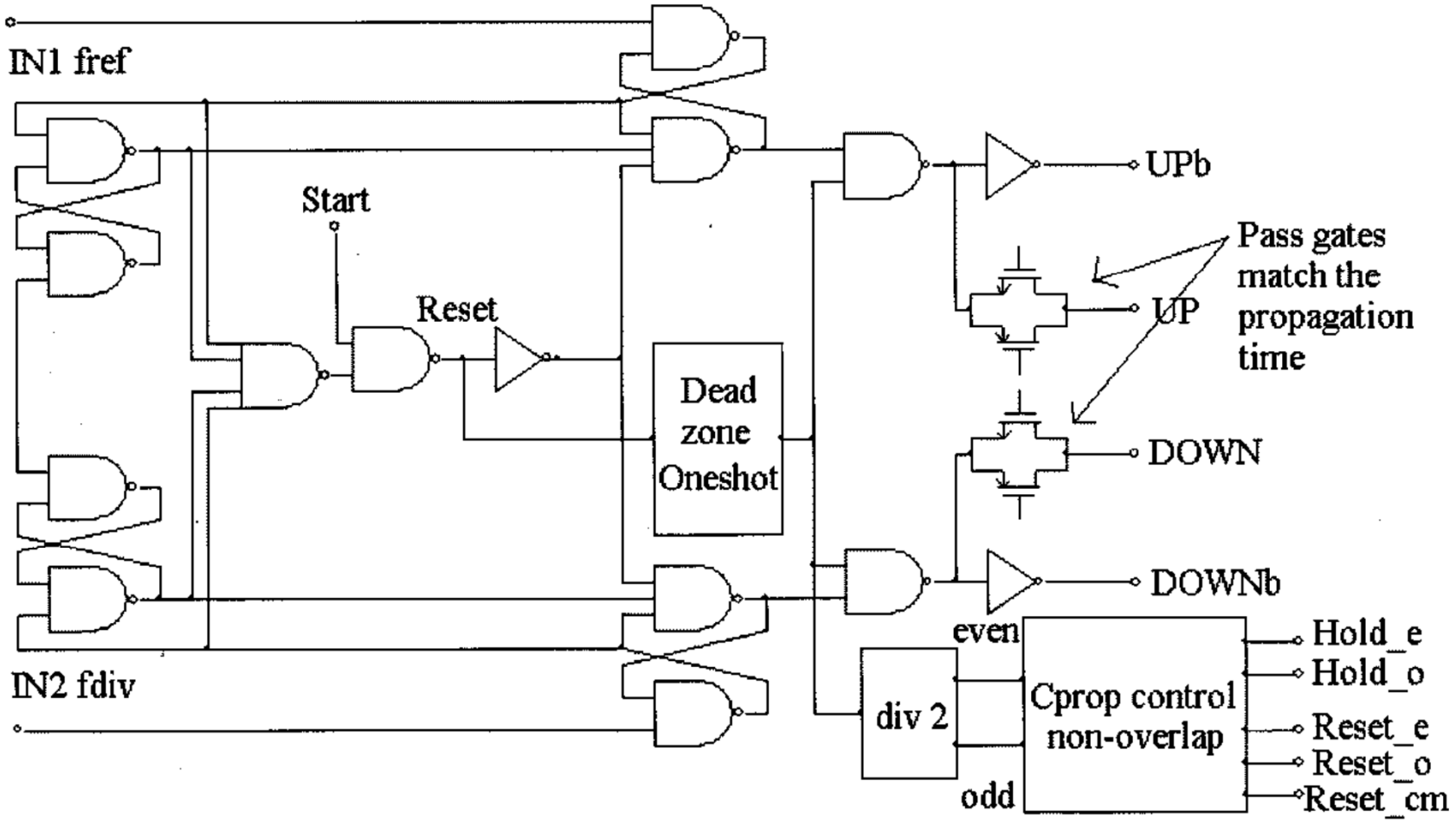
Sample-Reset Loop Filter w/ Double Capacitors





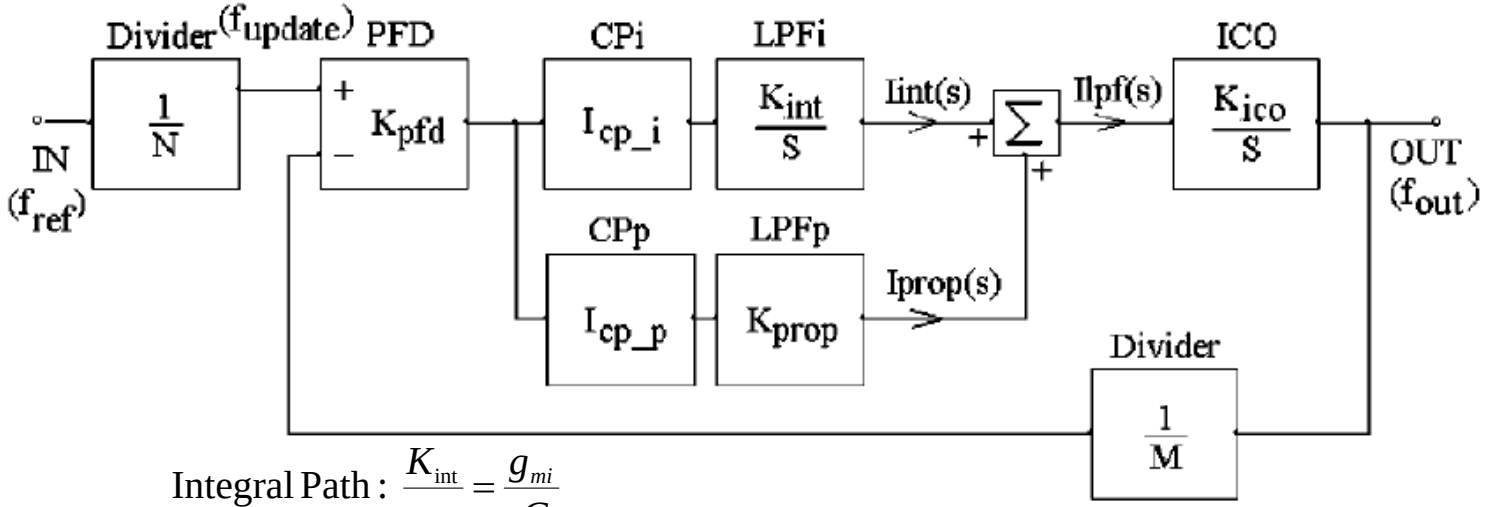
- With a double-capacitor implementation, the remaining ripple is dramatically reduced
- While one capacitor is being reset and then having the phase error sampled, the other capacitor which holds the previous sampled proportional voltage is attached to the gm output stage

Sample-Reset PLL PFD & Filter Switch Signal Generation



- The PFD reset signal is divided by 2 to produce the even and odd switch control signals
- During reset, the charge pump shouldn't be conducting and the filter capacitor can be applied to the main loop

Sample-Reset PLL Small-Signal Model



$$\text{Integral Path}: \frac{K_{\text{int}}}{s} = \frac{g_{mi}}{sC_i}$$

$$\text{Proportional Path}: K_{prop} = \frac{T_{update} g_{mp}}{C_p}$$

$$\text{Total ICO Current}: I_{lpf}(s) = I_{\text{int}}(s) + I_{prop}(s) = \left(\frac{I_{cp\_i}}{2\pi}\right)\left(\frac{g_{mi}}{sC_i}\right) + \left(\frac{I_{cp\_p}}{2\pi}\right)\left(\frac{T_{update} g_{mp}}{C_p}\right)$$

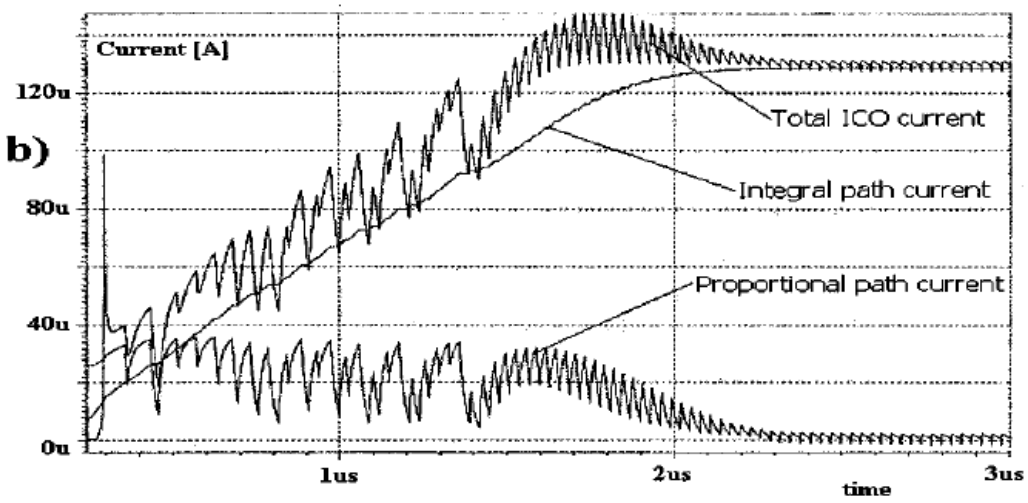
$$H(s) = \frac{\left(\frac{I_{cp\_i}}{2\pi}\right)\left(\frac{g_{mi}}{C_i}\right)K_{ico}\left(1 + s\left(\frac{I_{cp\_p}}{I_{cp\_i}}\right)\left(\frac{C_i}{C_p}\right)\left(\frac{T_{update} g_{mp}}{g_{mi}}\right)\right)}{s^2 + \left(\frac{I_{cp\_p}}{2\pi}\right)K_{ico} T_{update} g_{mp} s + \frac{I_{cp\_i} g_{mi} K_{ico}}{2\pi M C_i}}$$

$$\omega_n = \sqrt{\frac{I_{cp\_i} g_{mi} K_{ico}}{2\pi M C_i}} \qquad \omega_z = \left(\frac{I_{cp\_i}}{I_{cp\_p}}\right)\left(\frac{C_p}{C_i}\right)\left(\frac{g_{mi}}{T_{update} g_{mp}}\right)$$

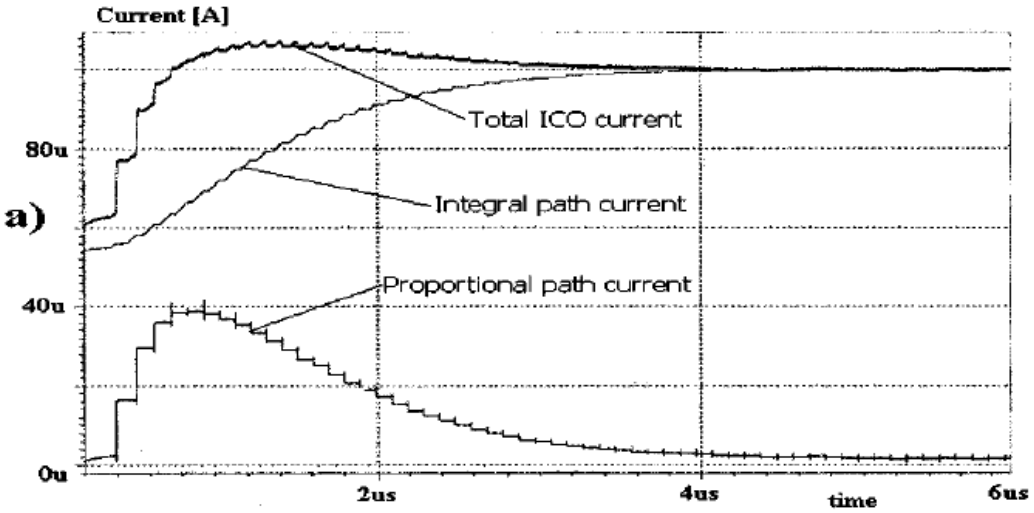
$$\zeta = \frac{1}{2}\left(\frac{\omega_n}{\omega_z}\right) = \frac{1}{2}\sqrt{\frac{K_{ico} C_i}{2\pi M I_{cp\_i} g_{mi}}}\left(\frac{I_{cp\_p} T_{update} g_{mp}}{C_p}\right)$$

ICO Control Waveforms

Standard Charge Pump PLL



PLL w/ Sample-Reset Filter



- PLL w/ sample-reset filter has dramatically reduced ripple voltage on oscillator control signal
- The control signal displays an almost ideal stair-step response

Next Time

- VCOs