# Capacitive DAC for Asynchronous SAR ADC

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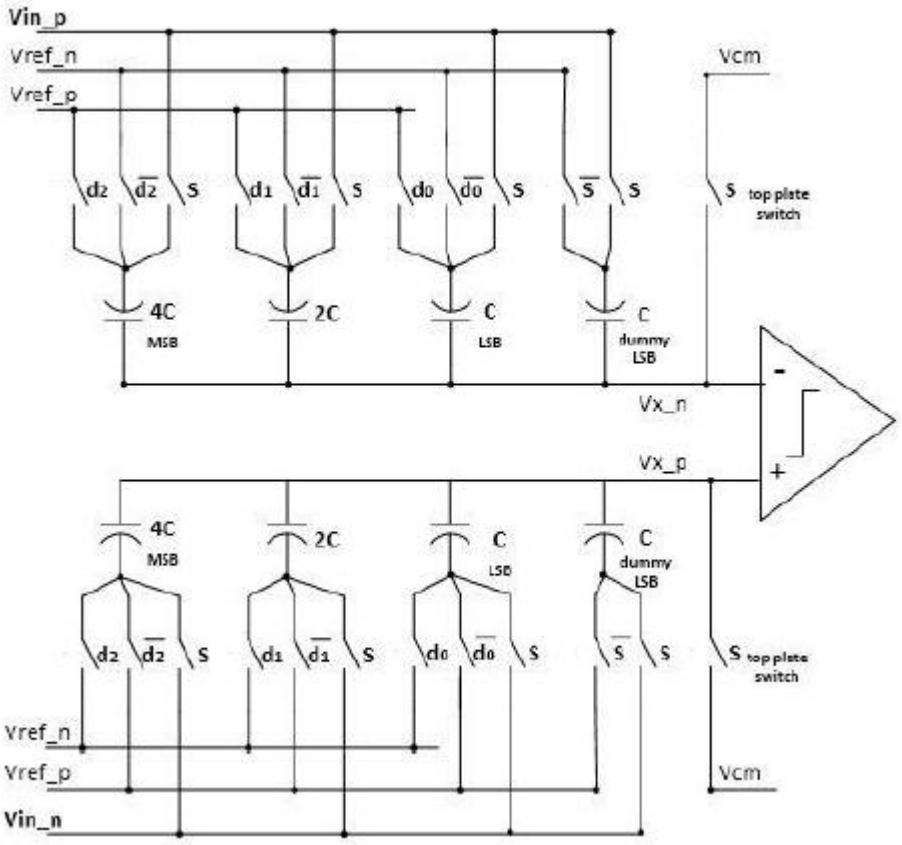
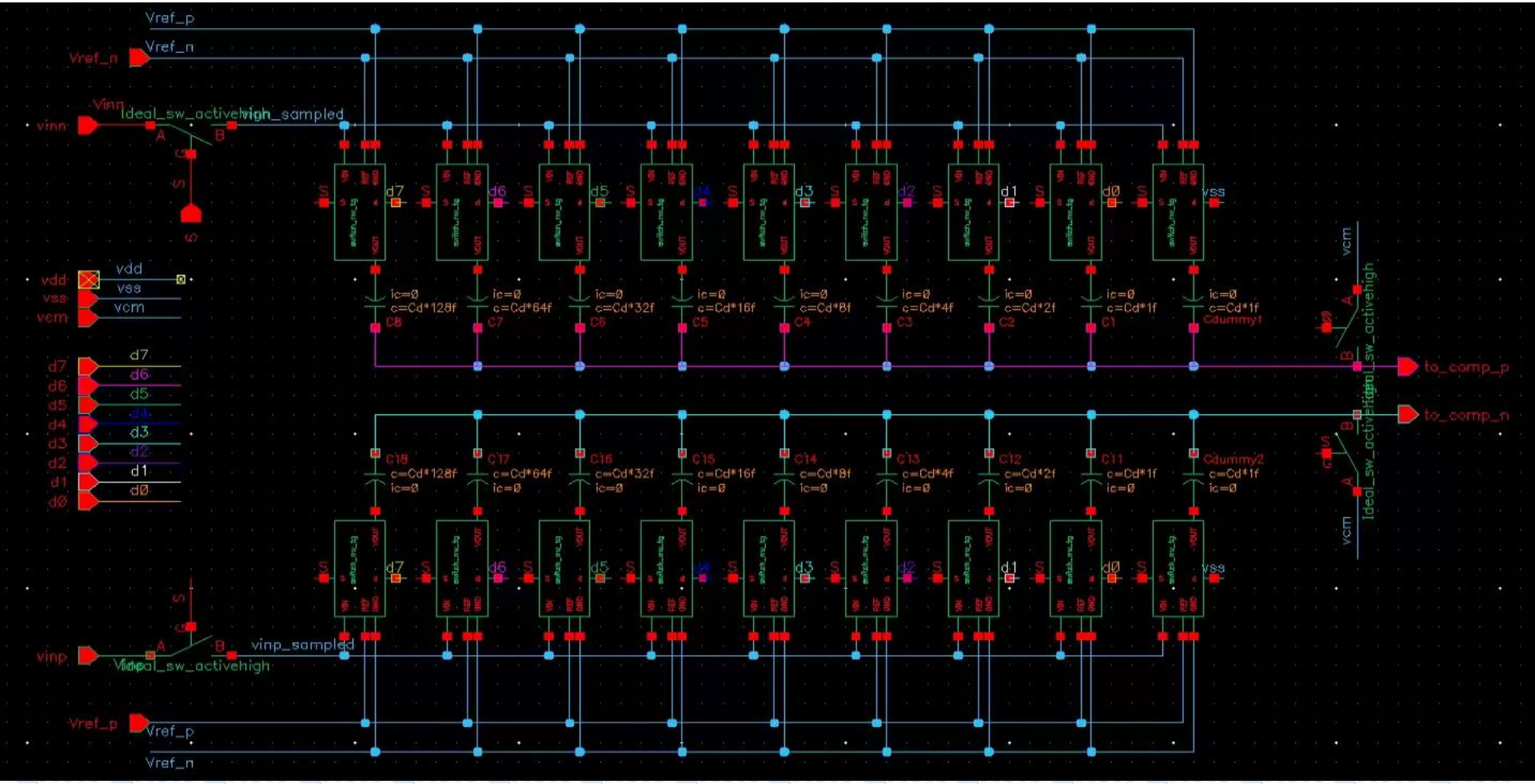
# Reference

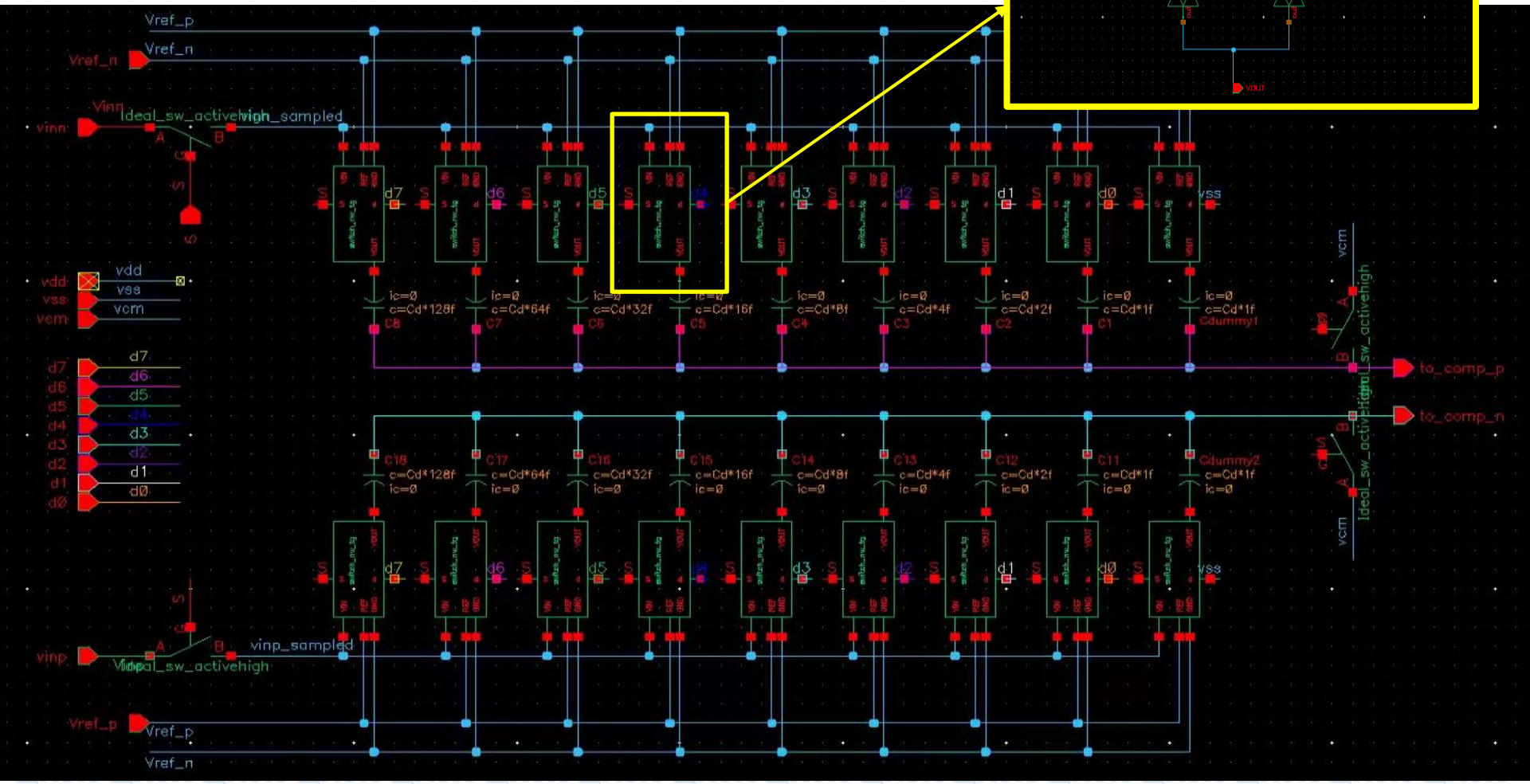



Reference:
O. Kardonik, " A study of SAR ADC and implementation of 10-bit asynchronous design," M.S. Thesis, Department of Electrical and Computer Engineering, University of Texas at Austin, 2013.

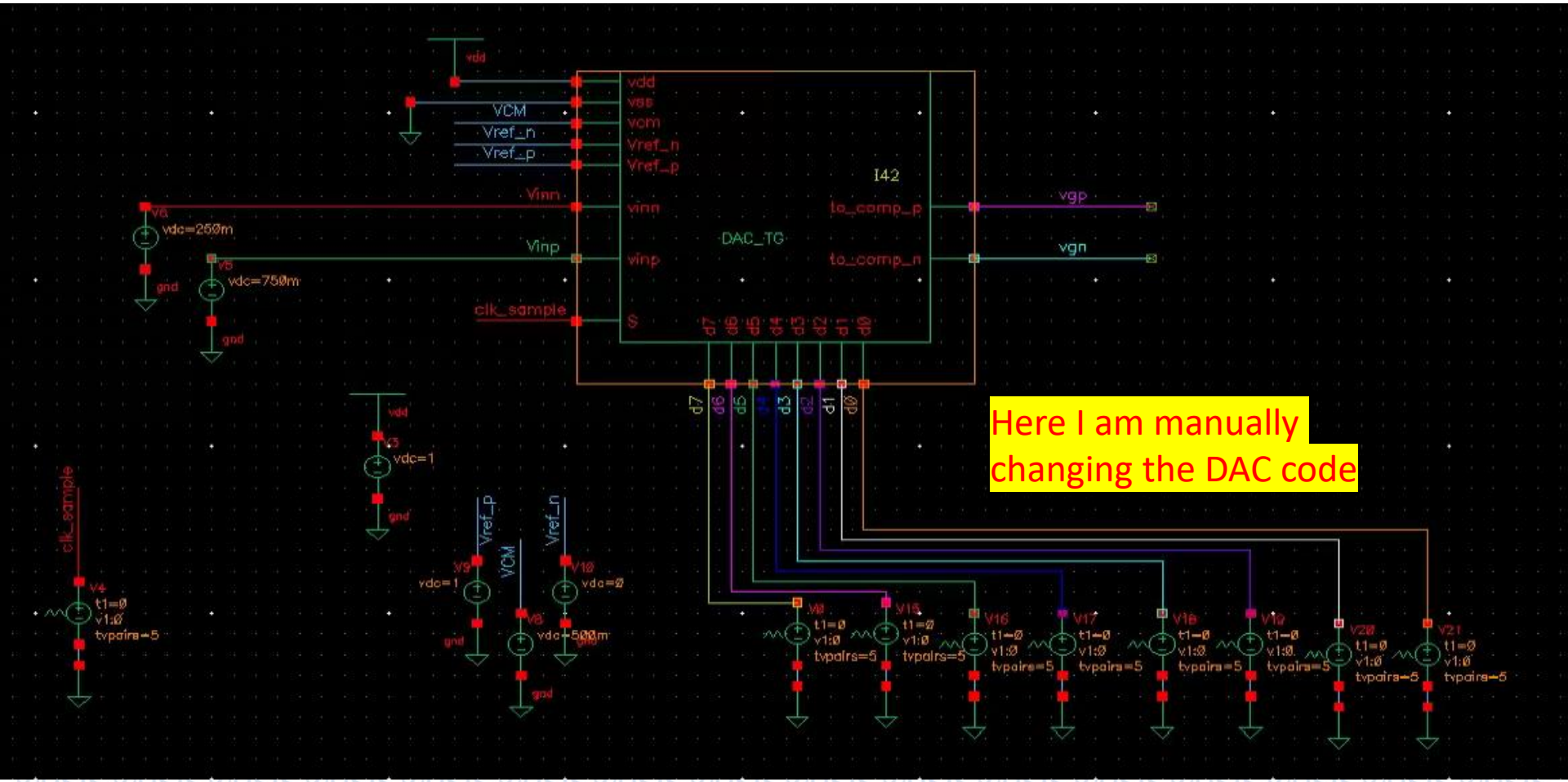
# Schematics


Vref_p
Vref_n
Vinn
ideal_sw_activehigh
vinn
vdd
vss
vcm
d7
d6
d5
d4
d3
d2
d1
d0
ic=0
c=Cd*128f
c=Cd*64f
c=Cd*32f
c=Cd*16f
c=Cd*8f
c=Cd*4f
c=Cd*2f
c=Cd*1f
Cdummy1
Cdummy2
to_comp_p
to_comp_n
vinp
vinp_sampled

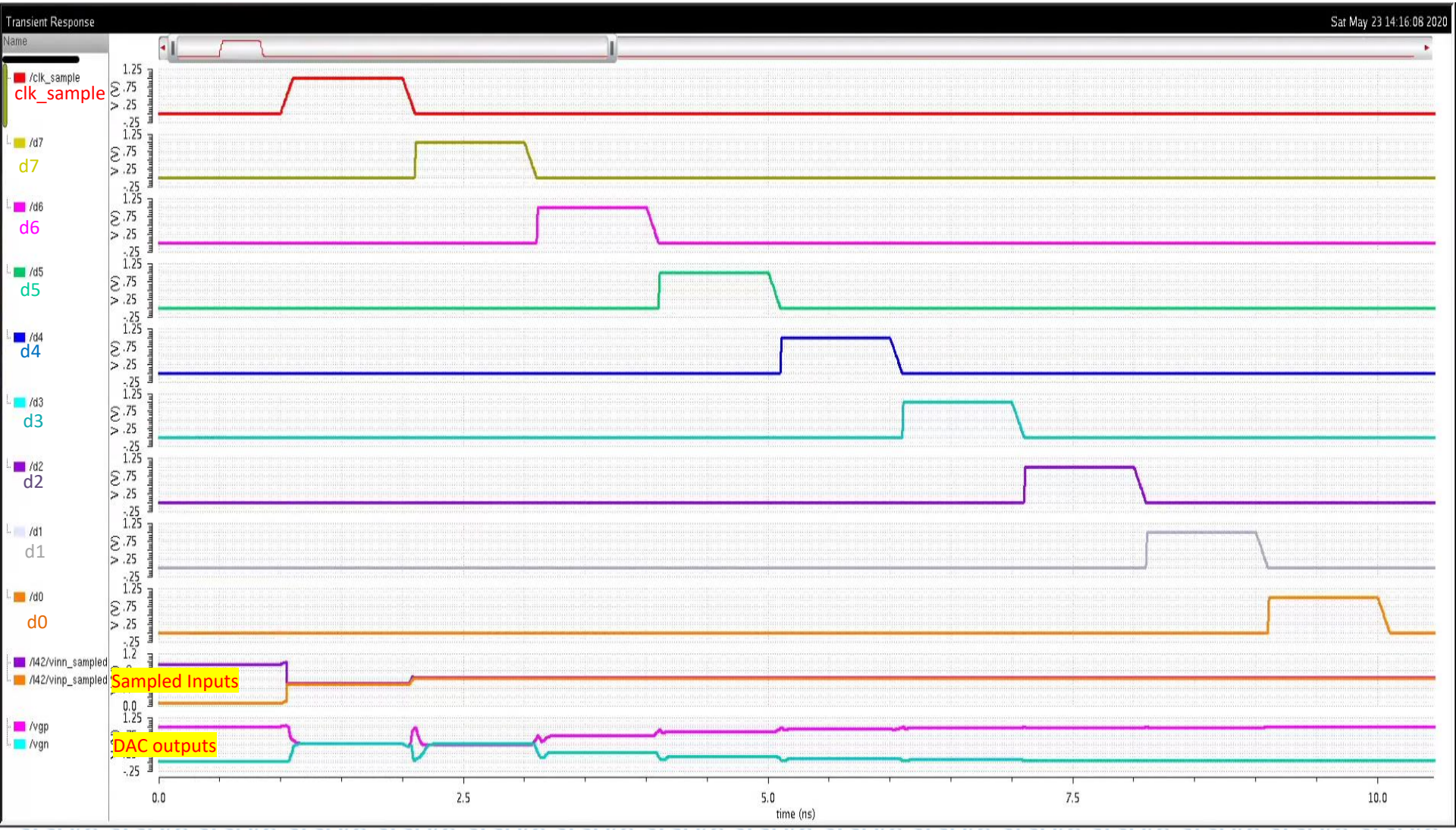
# Schematics


Vref_p
Vref_n
Vinn
ideal_sw_activehigh_sampled
vinn
vdd
vss
vcm
d7
d6
d5
d4
d3
d2
d1
d0
ic=0
c=Cd*128f
c=Cd*64f
c=Cd*32f
c=Cd*16f
c=Cd*8f
c=Cd*4f
c=Cd*2f
c=Cd*1f
Cdummy1
Cdummy2
to_comp_p
to_comp_n
vinp
vinp_sampled
ideal_sw_activehigh

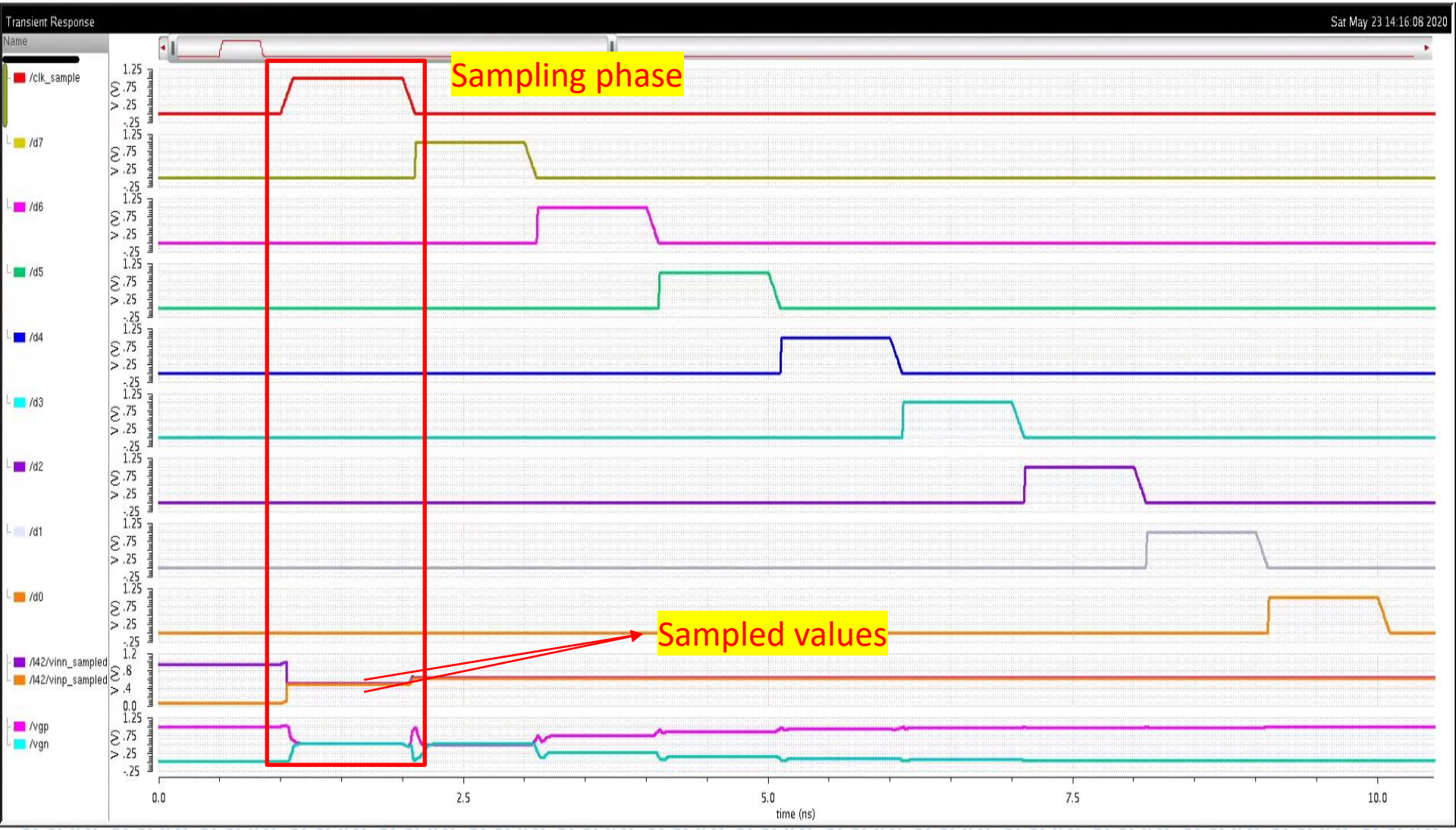
# Testbench


vdd
VCM
Vref_n
Vref_p
Vinn
Vinp
clk_sample
vdc=250m
vdc=750m
gnd
I42
DAC_TG
vinn
vinp
vcm
vss
S
to_comp_p
to_comp_n
vgp
vgn
d7
d6
d5
d4
d3
d2
d1
d0
vdc=1
vdc=500m
tvpairs=5
Here I am manually changing the DAC code

# Waveforms


Transient Response
Sat May 23 14:16:08 2020
Name
/clk_sample
clk_sample
/d7
d7
/d6
d6
/d5
d5
/d4
d4
/d3
d3
/d2
d2
/d1
d1
/d0
d0
/I42/vinn_sampled
/I42/vinp_sampled
Sampled Inputs
/vgp
/vgn
DAC outputs
1.25
.75
.25
-.25
1.2
0.0
0.0
2.5
5.0
7.5
10.0
time (ns)

# Waveforms

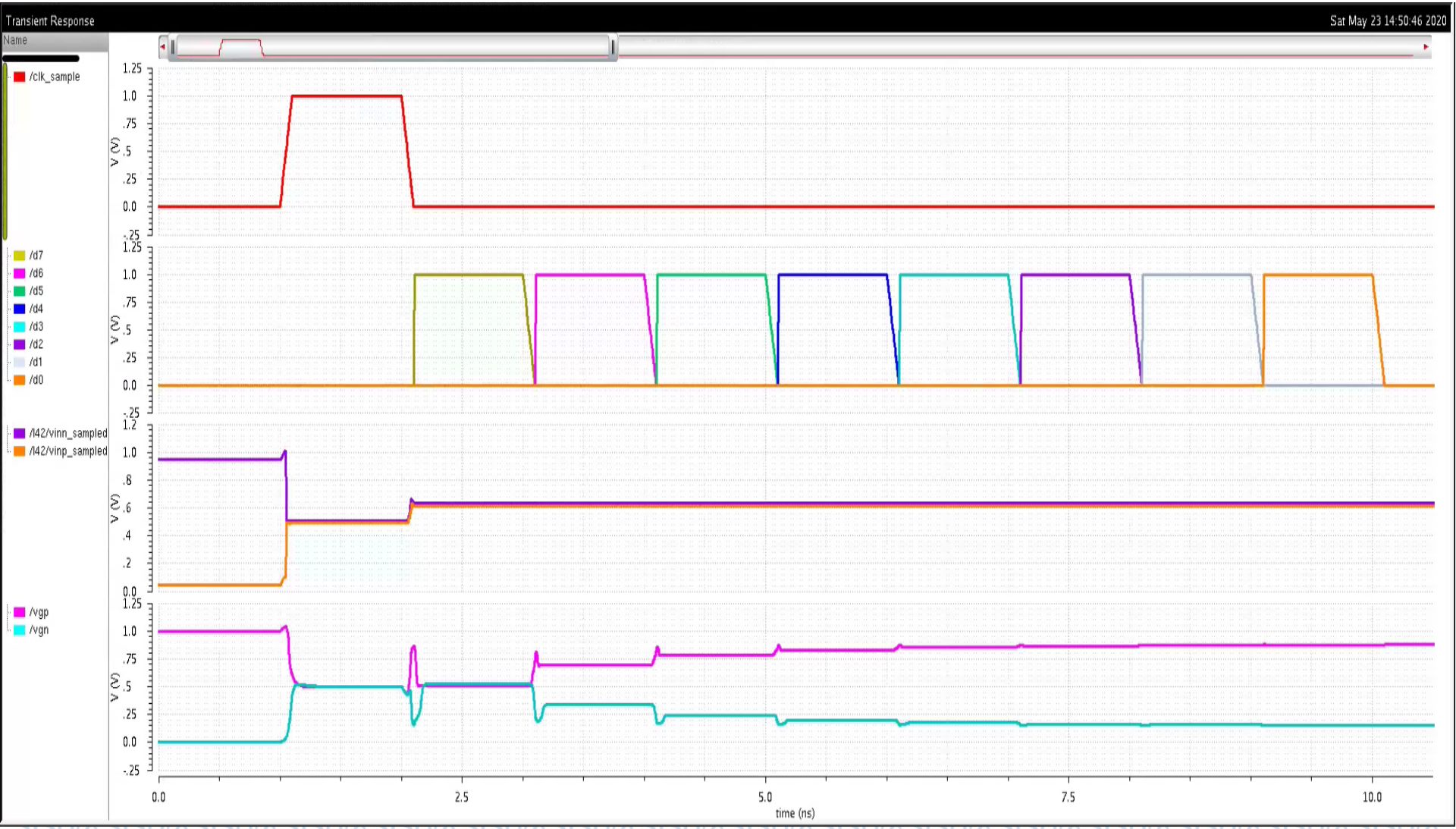

Transient Response
Sat May 23 14:16:08 2020
Name
/clk_sample
/d7
/d6
/d5
/d4
/d3
/d2
/d1
/d0
/I42/vinn_sampled
/I42/vinp_sampled
/vgp
/vgn
Sampling phase
Sampled values
V (V)
time (ns)
0.0
2.5
5.0
7.5
10.0

# Waveforms


Transient Response
Sat May 23 14:16:08 2020
Name
/clk_sample
/d7
/d6
/d5
/d4
/d3
/d2
/d1
/d0
/I42/vinn_sampled
/I42/vinp_sampled
/vgp
/vgn
Sampling phase
Outputs of the DAC =
Inputs to the Comparator
0.0
2.5
5.0
7.5
10.0
time (ns)

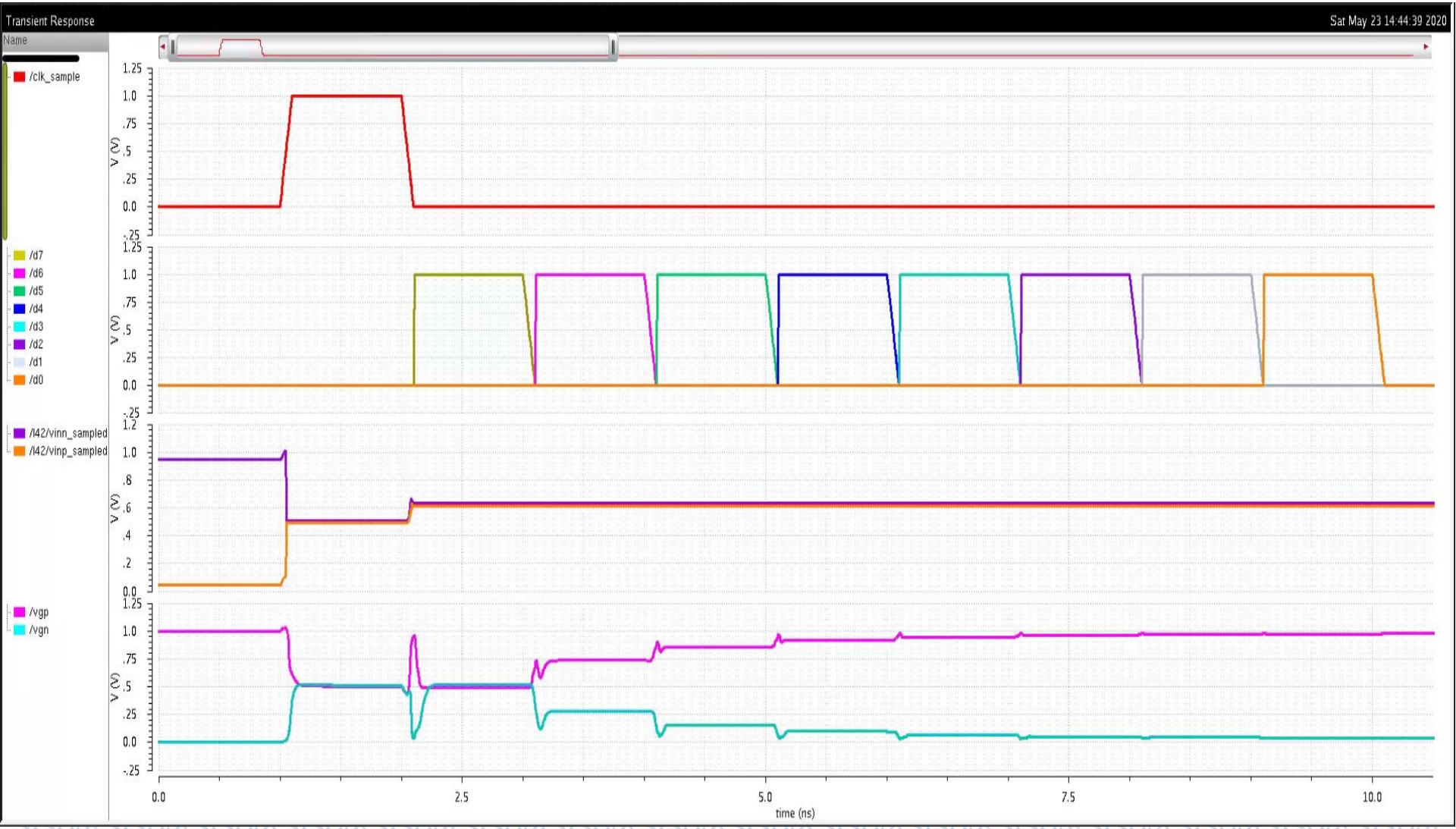
**Unit Cap:**
**Cd = 1fF**

# Waveforms



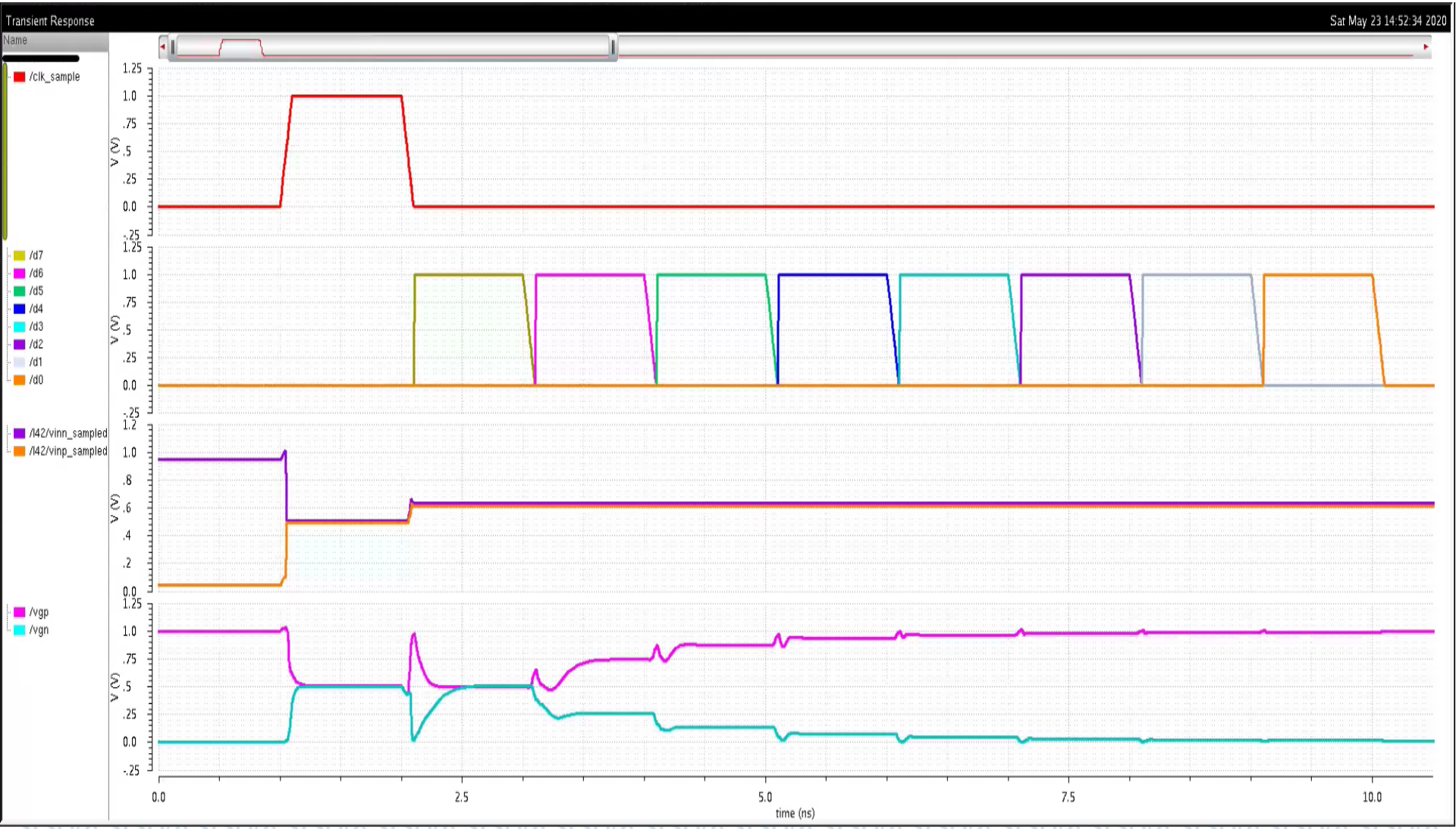
**Unit Cap:**
**Cd = 10fF**

# Waveforms



**Unit Cap:**
**Cd = 50fF**

# Waveforms



# Note

- The settling time decreases by:
  1. Decreasing the unit Cap value.
  2. Decreasing the resistance of the transmission gate switches. (By increasing W of the PMOS & NMOS of the TG switches)