A High Speed Dynamic StrongARM Latch Comparator

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***Abstract*—In this paper, a new design has been proposed for a high speed, low power StrongARM latch in 65nm CMOS technology. Latching speed improvements of 18% and 16% have been achieved in comparison to the conventional [4] and improved StrongARM [5], respectively, while the energy consumption has also been reduced.**

Keywords—StrongARM latch, low power circuit design; comparator; high speed

I. INTRODUCTION

As decision speed is the major figure of merit for latches, much focus has been placed to improve the performance of latch circuits. Attempts for enhancement of the performance have often resulted in high energy consumption and/or increased area. A successful scheme to achieve high speeds has been using the Current-Mode-Logic to steer current at different rates based on the input signals. Transforming the continuous CML to charge steering has shown significant advantages in improving the figure of merit [1]. This technique reduces power dissipation and maintains rail-to-rail output, without degrading the speed [2]. Owing to its first use in Digital Equipment Corporation's StrongARM microprocessor [3], the latch has coined the name of "StrongARM" latch and has been improved multiple times since then [4-5].

The conventional [4] and improved [5] StrongARM latch circuits are shown in Fig. 1a and 1b, respectively. The whole cycle of operation for these two topologies can be described in three stages: reset, amplification, and regeneration. In the reset mode, CLK signal is set to low, allowing nodes (A and A') to pre-charge to V_{dd} via Charging Transistors (CT_1 and CT_2). These StrongARM topologies comprise of two cross-coupled pairs ($T_{1,2}$ and $T_{3,4}$) with input differential transistors in between (T_5 and T_6). Given that the differential input transistors are ON by the common mode bias voltage, unlike the designs in [2] and [4], there is no need for extra transistors (CT_3 and CT_4 as shown in Fig. 1a) to charge up the nodes A_x and A_x'. The amplification mode starts by setting CLK to high, thus deactivating the CT_1-CT_2 pair and activating the tail current transistor T_7. This creates a discharging path for (A - A') and (A_x -A_x') nodes to ground. A small voltage variance across the input transistors will cause the nodes in the two branches to discharge with different rates. Once the voltages across the (A – A') nodes reach (V_{dd}-V_{th}), the regeneration phase starts in which the PMOS cross-coupled pair (T_1-T_2) start conducting to rebuild a high potential in one of the nodes based on the polarity of the differential input.

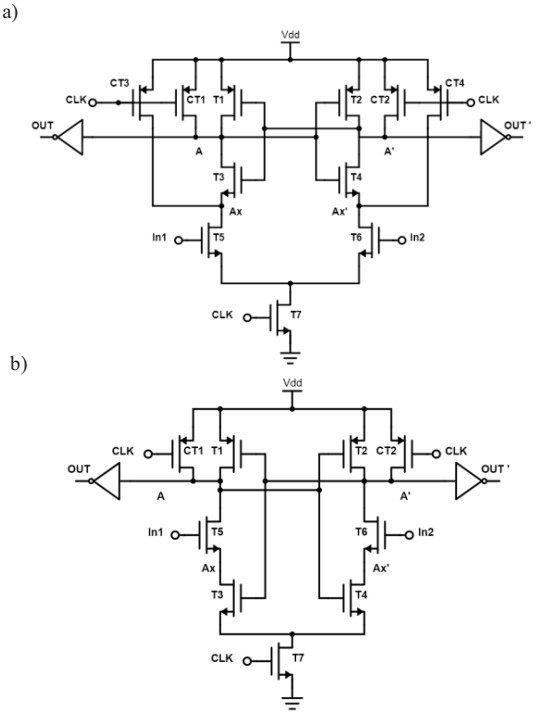

Fig. 1. a) Conventional StrongARM Latch Topology[4], b)Improved StrongARM Latch Topology [5]

II. PROPOSED DESIGN

The improved StrongARM latch topology shown in Fig. 1b benefits from using input common mode voltage in the reset phase to charge up the A_x-A_x' nodes. Fig. 2 shows the proposed StrongARM topology. The main idea here is to turn off the input differential pair transistors, thus improving both of the speed and energy. As shown in Fig. 2, CLK' is used as a select signal to provide the differential transistors with either input signals or ground. During the reset phase, both A and A' nodes are charged up to V_{DD} through $CT_{1,2}$. This will turn on the lower cross coupled NMOS transistors T_3 and T_4, which will connect the nodes A_x and A_x' to ground. Unlike the previous StrongARM topologies that use a clocked tail current transistor (T_7) to avoid creating a path from V_{DD} to ground, the proposed topology turns off $T_{5,6}$ to disconnect the upper and lower halves

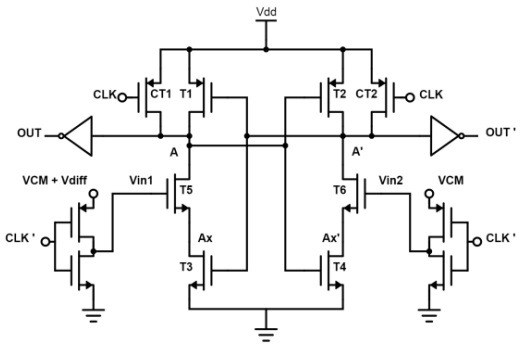

Fig. 3. Proposed StrongARM Latch Topology

of the StrongARM. That way, nodes (A and A') and (A_x and A_x') will be set to strong V_{dd} and ground signals respectively. Therefore, once the evaluation stage starts, higher current passes from drain to source of the differential transistors. In addition, V_{GS} is higher in the proposed latch because of the low potential at the source terminals. As the transconductance of the input differential transistors is a function of both I_{DS} and V_{GS}, the amplification gain is higher and the divergence of A and A' signals occurs earlier as a consequence.

III. Simulation Results

Fig. 3 shows the simulation results for the conventional, improved and proposed StrongARM latch comparators using TSMC 65nm Process Design Kit [6]. For a fair comparison, all designs are simulated under the same conditions. A 10 mV differential input voltage and a fan-out of 4 (FO4) load test have been used. It can be easily observed in the grayed region that the rate of discharge of A and A' nodes in the proposed latch is steeper than that of the improved StrongARM. The proposed design exhibited improvements of about 16% in speed in comparison to [5]. Table I compares the delay and energy obtained by this work among the advanced StrongARM comparators in the literatures using 65nm CMOS technology.

Fig. 3 also shows that the proposed design has a slight increase in the clock feedthrough due to the instantaneous off-state of the input differential transistors. This is caused because "Vin_1" and "Vin_2" nodes experience negative clock feedthrough effect that causes the input transistors (T_5 and T_6)

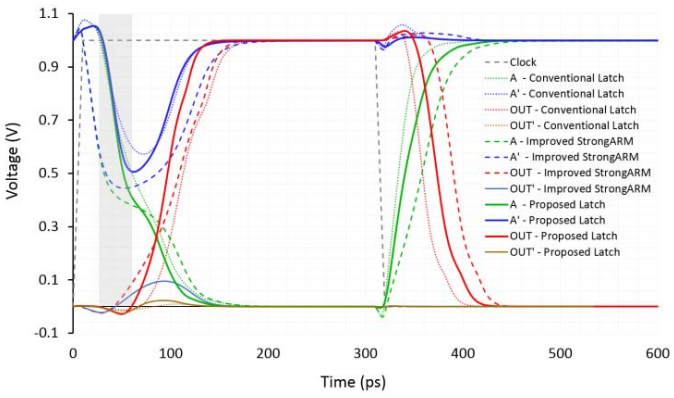

Fig. 3. The response of the Conventional [4], Improved [5] and Proposed StrongARM Latch Topologies

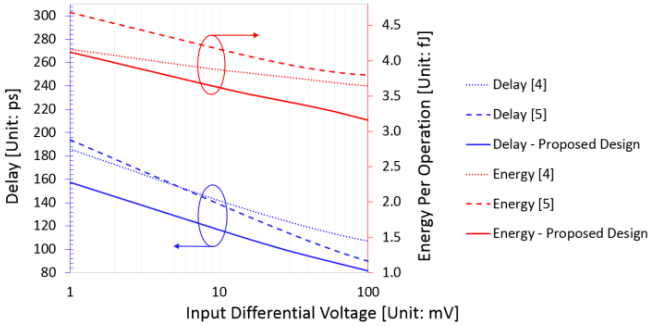

Fig. 4. Delay and E/Op vs. Differential Input for [4],[5] and this work

TABLE I. Delay-Energy Comparison for Vdiff=10milliVolts

	Delay (ps)	*Energy (fJ)*
Conventional StrongARM[4]	141.9	3.875
Improved StrongARM[5]	138.6	4.165
Proposed StrongARM	116.4	3.62

to remain shut for a short interval of time, while nodes (A and A') get charged further. Nevertheless, once the differential transistors are turned on by the common mode voltage, they amplify the differential voltage in a swift manner. One way to address this issue is by introducing CLK' slightly before CLK, so $Vin_{1,2}$ nodes have enough time to reach voltages above the threshold voltage of the input differential pair.

Fig. 4 and Table I show the comparison of performance and energy per operation for the existing comparators [4-5] and the proposed topology in 65nm CMOS technology.

Conclusion

In this work, the performance of the StrongARM latch comparator has been improved by using a new scheme that turns the differential transistors "On" in the evaluation phase and "Off" in the reset phase. This way, the amplification gain in the evaluation phase will be enhanced, which results in faster separation of output signals. The proposed topology was simulated and benchmarked in 65nm CMOS technology to show improvement in both performance and energy in comparison to the mainstream topologies in the literature.

References

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