Dynamic Comparator for Asynchronous SAR ADC

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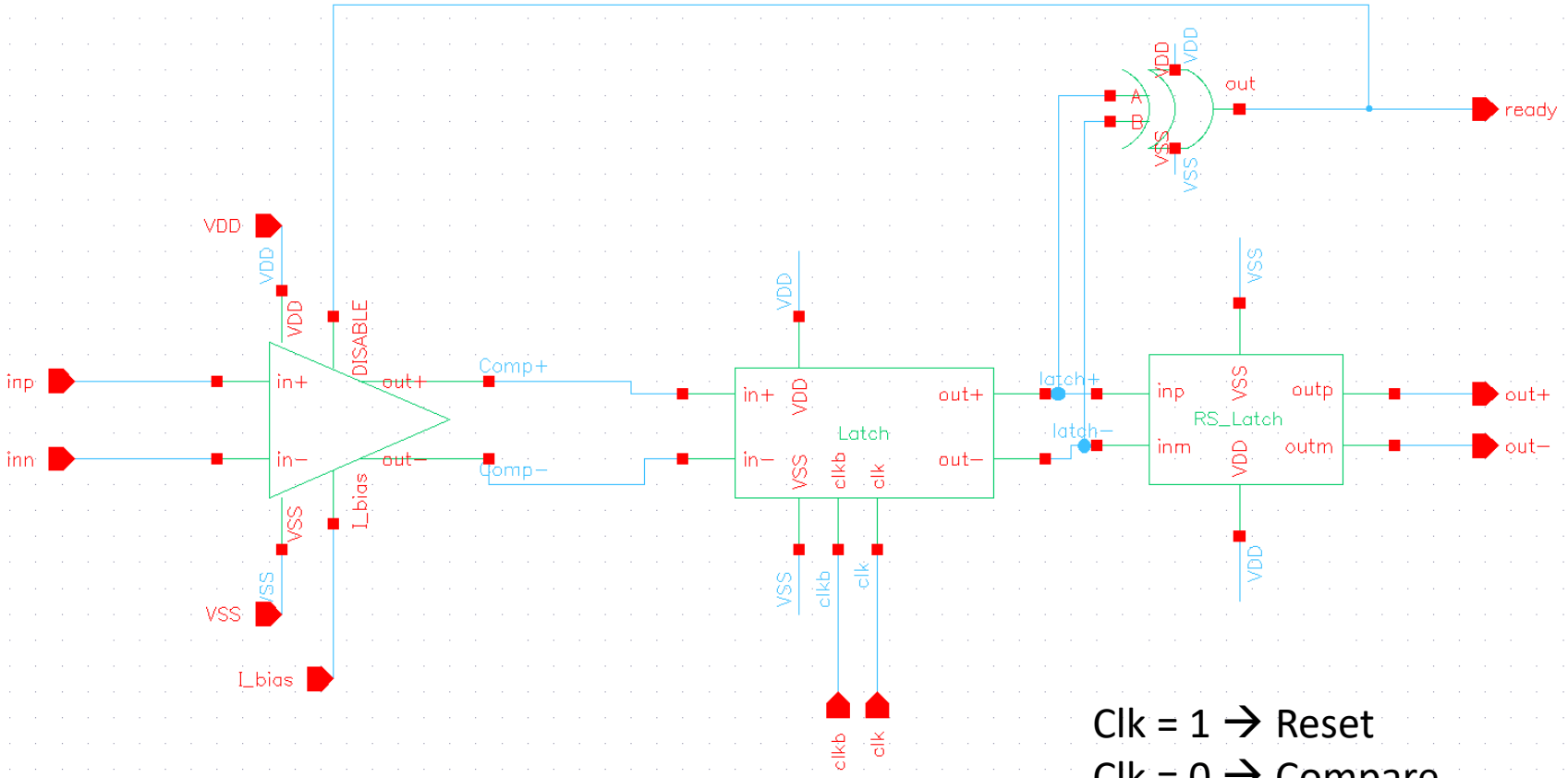
4/16/2020

Block Diagram

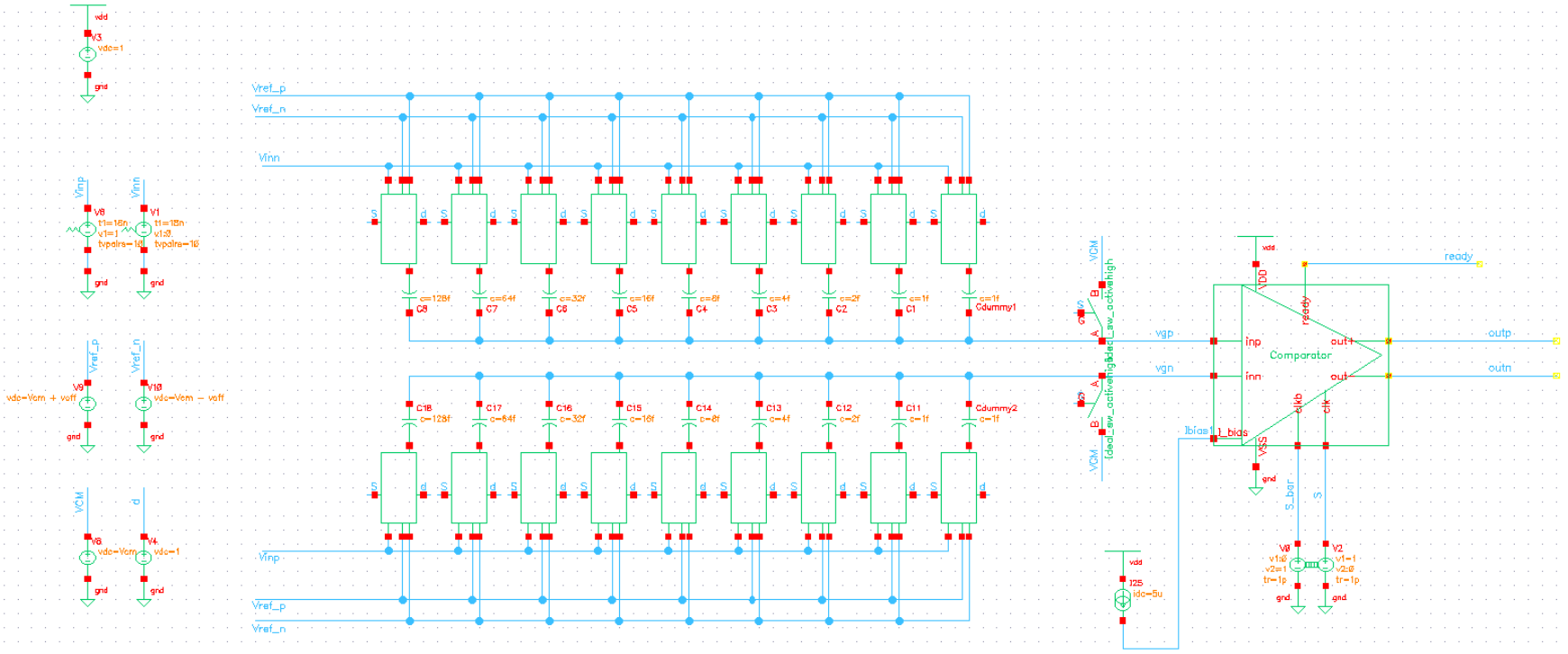


Clk = 1 → Reset

Clk = 0 → Compare

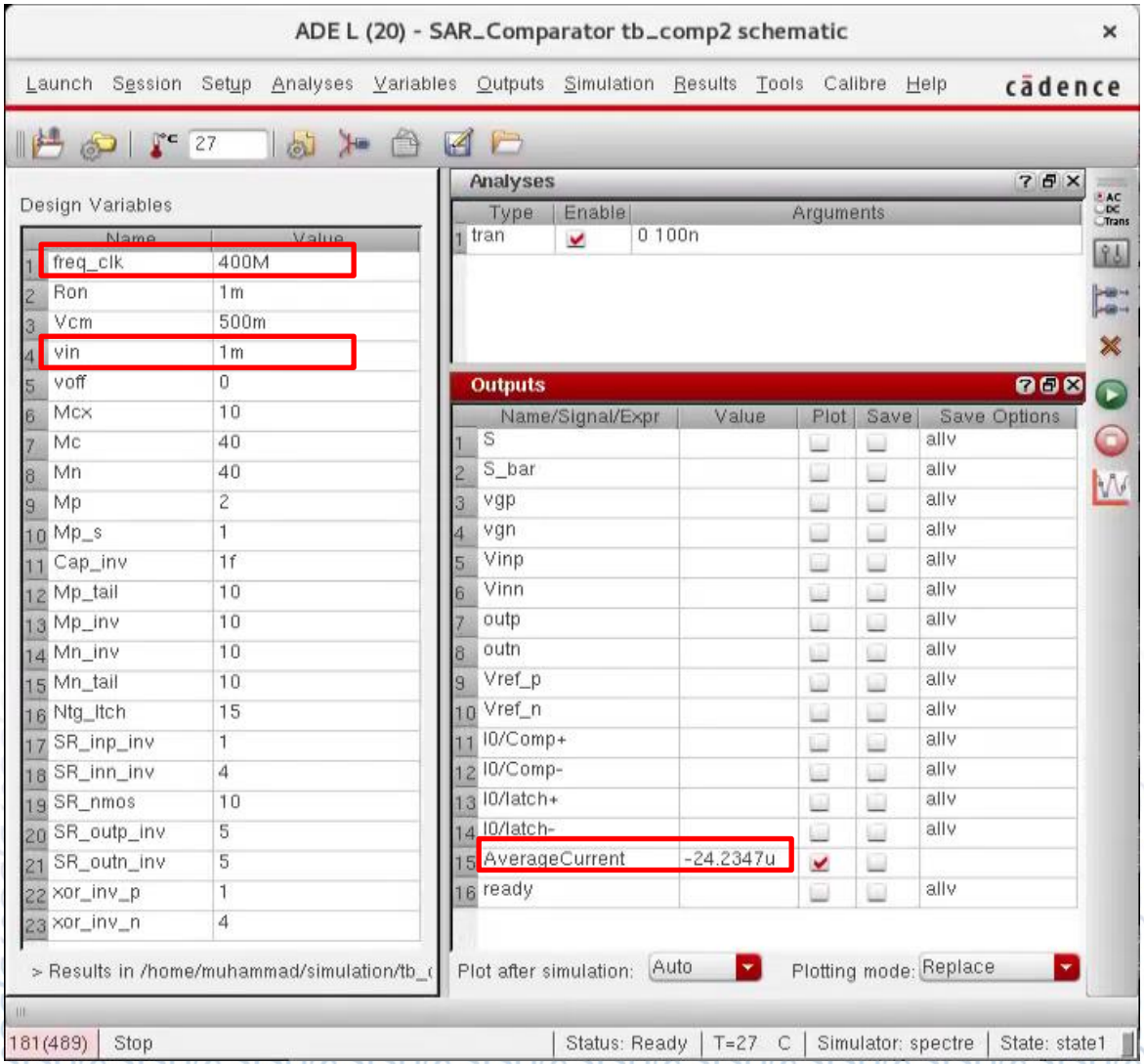
Testbench & Simulations

Testbench



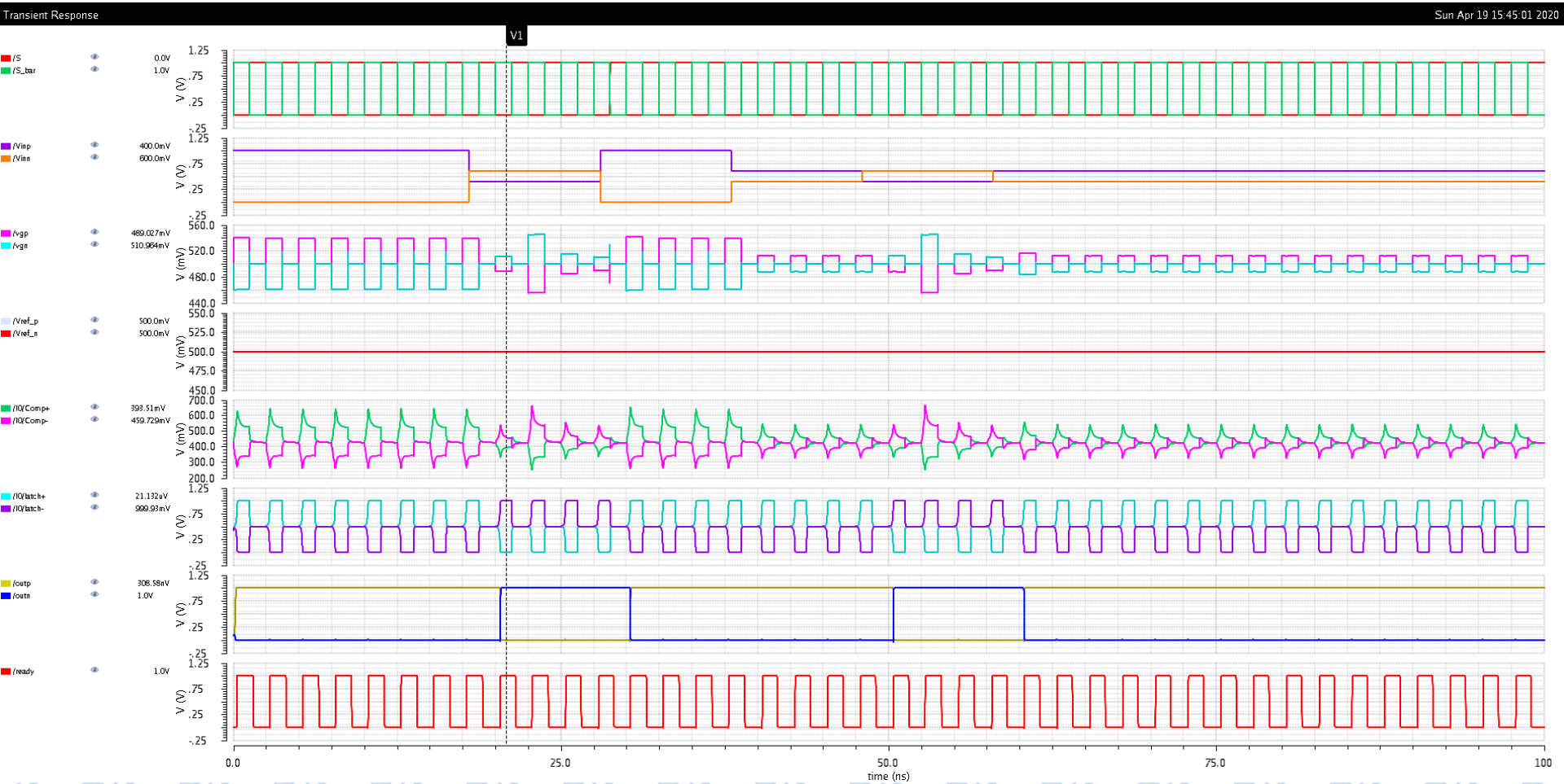
Vref_p
Vref_n
Vinn
Vinp
vdd
gnd
vgp
vgn
outp
outn
ready
Comparator
inp
inn
out1
out
clkb
clk
VDD
VSS
S_bar
S
Ibias1
I_bias
I25
idc=5u
Cdummy1
Cdummy2

Testbench (parameters)



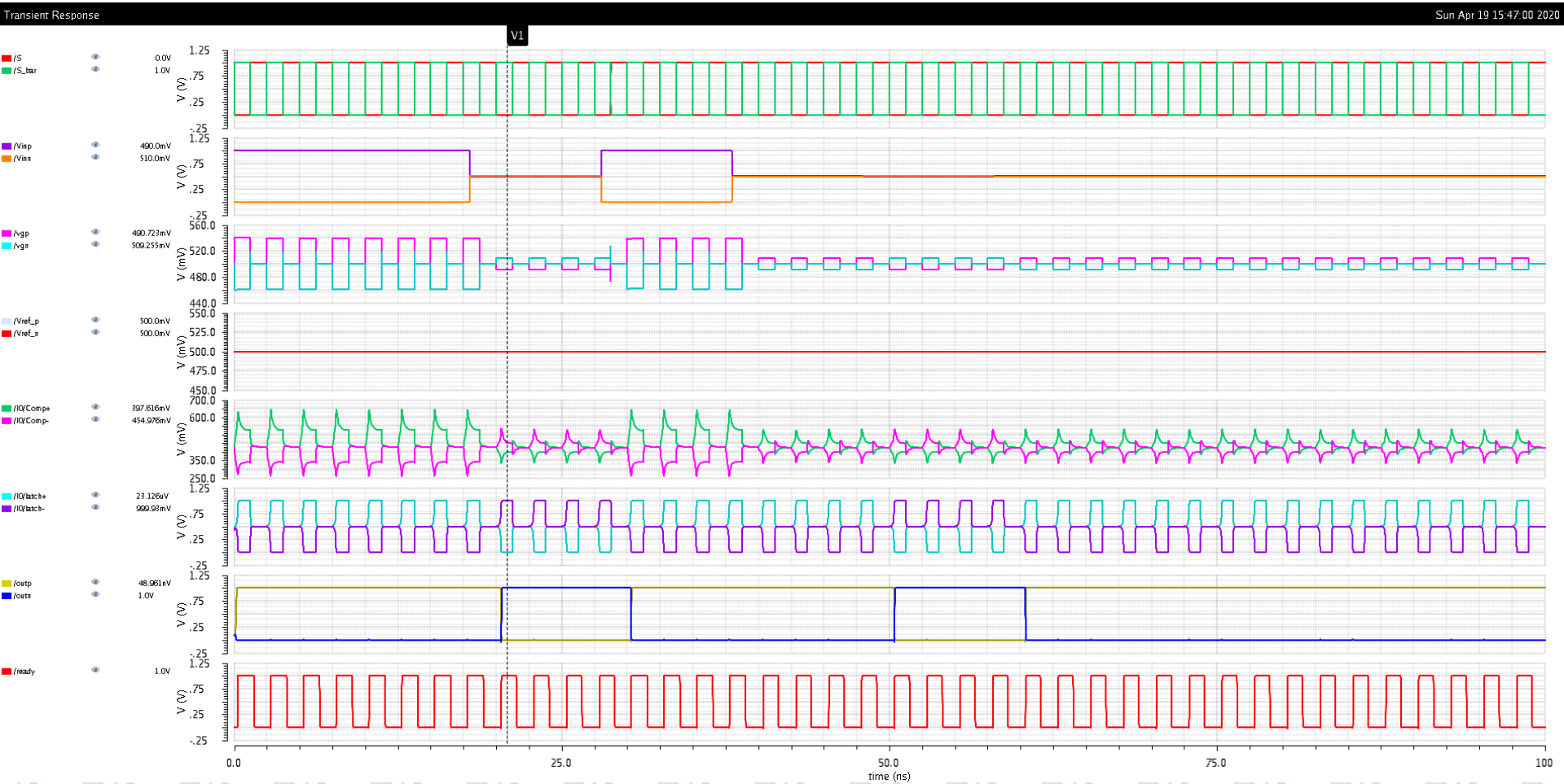
Overdrive test

Diff Vin_min = 2 x 100 mV



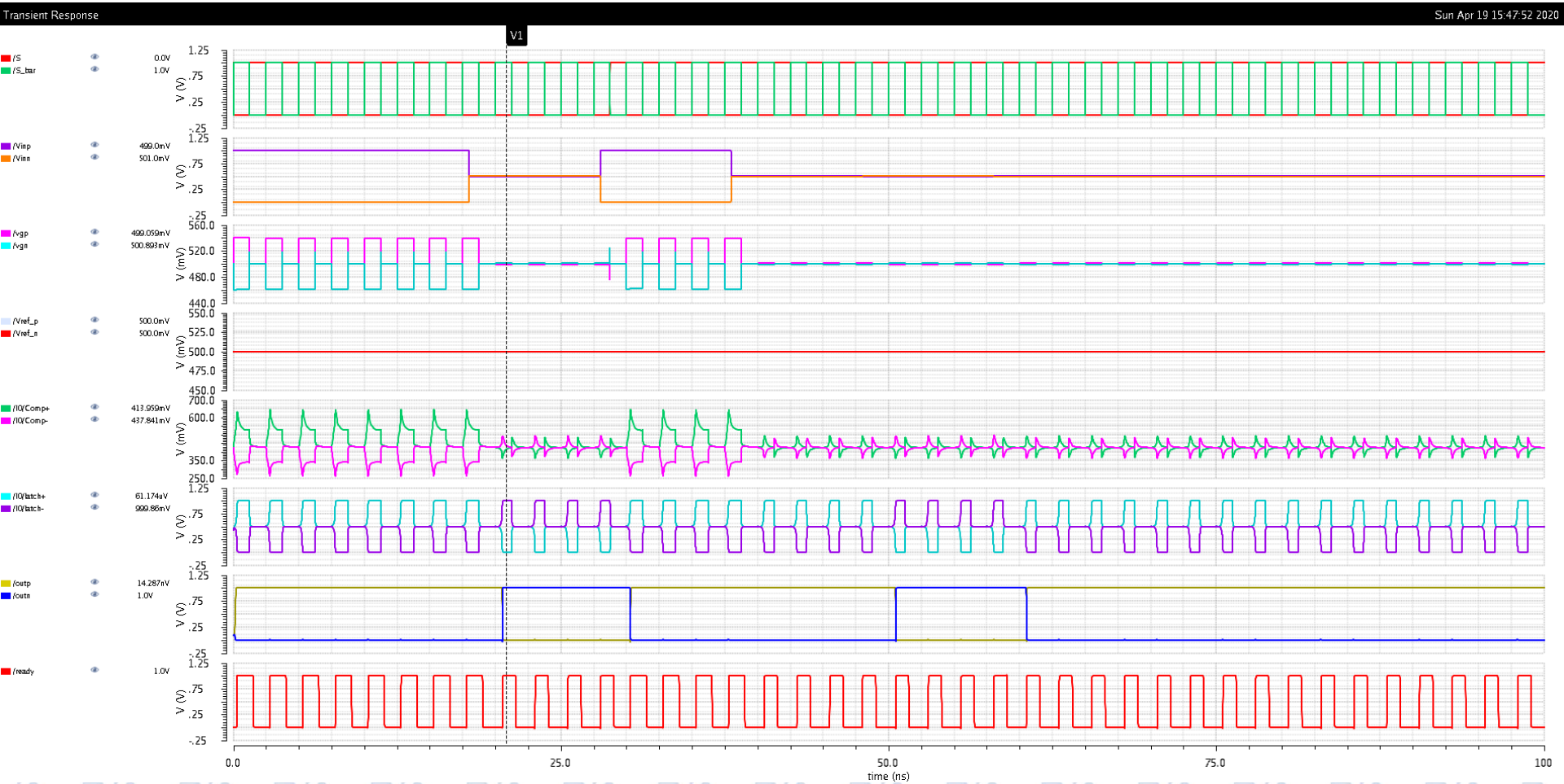
Overdrive test

Diff Vin_min = 2 x 10 mV



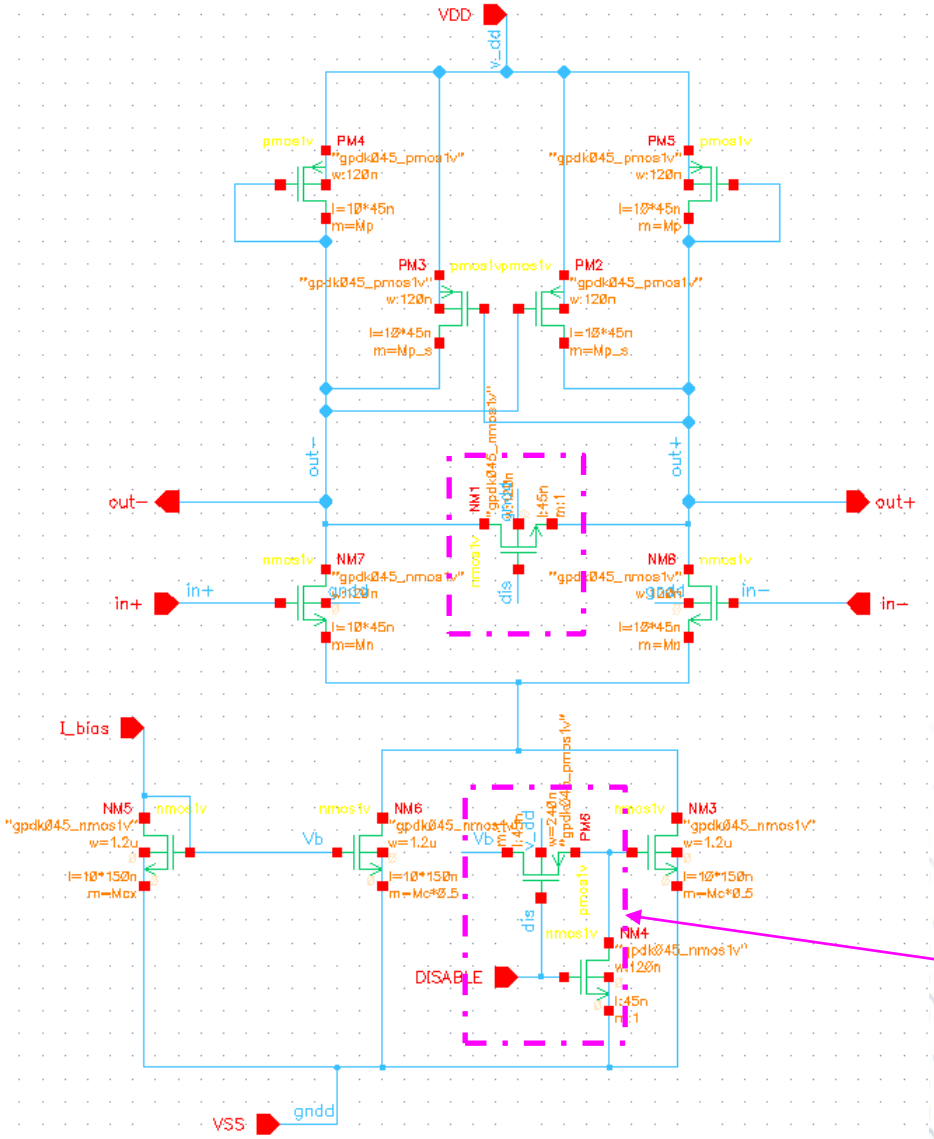
Overdrive test

Diff Vin_min = 2 x 1 mV (Smallest Resolution)

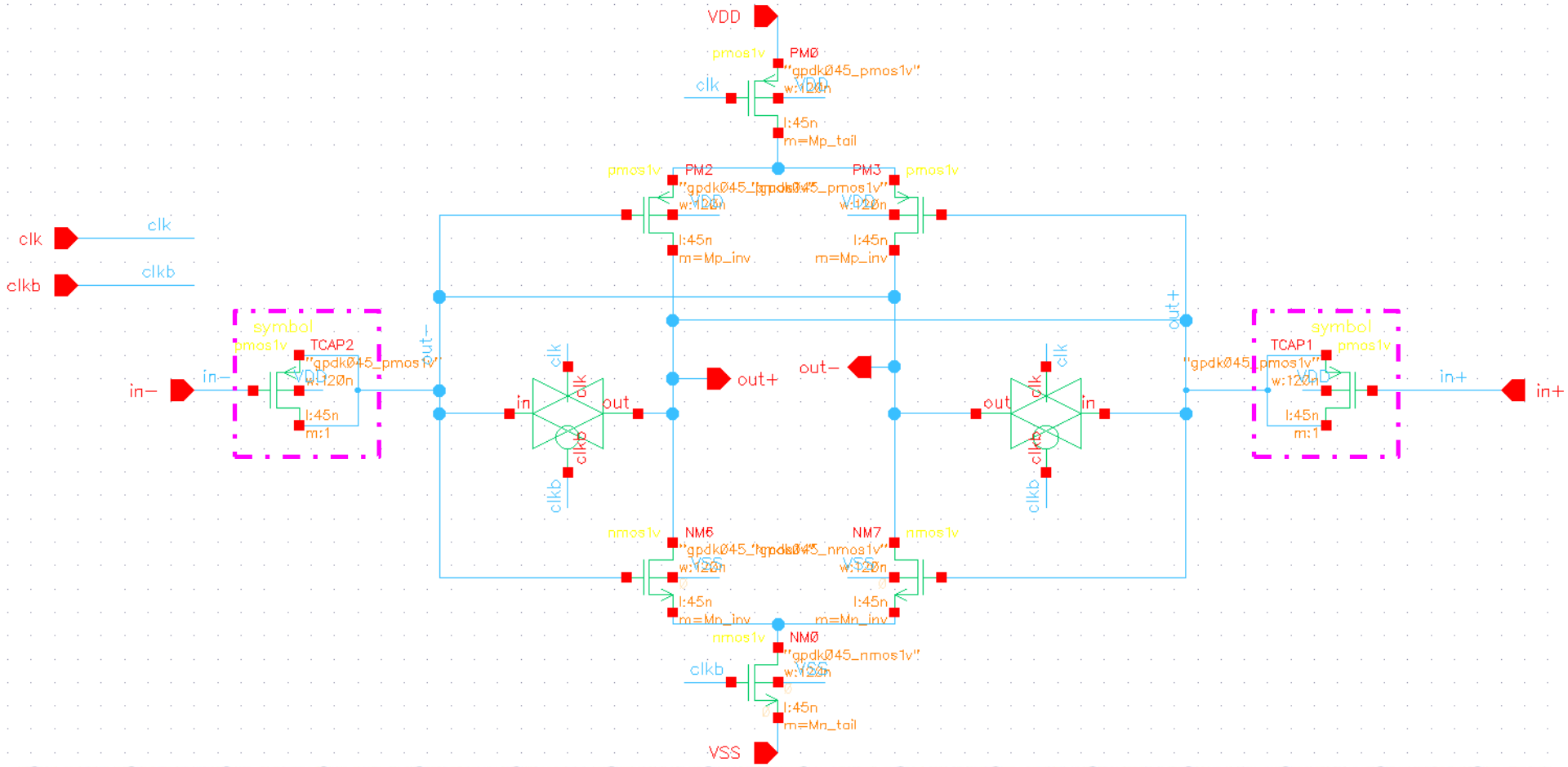


Modifications

1) Preamp:

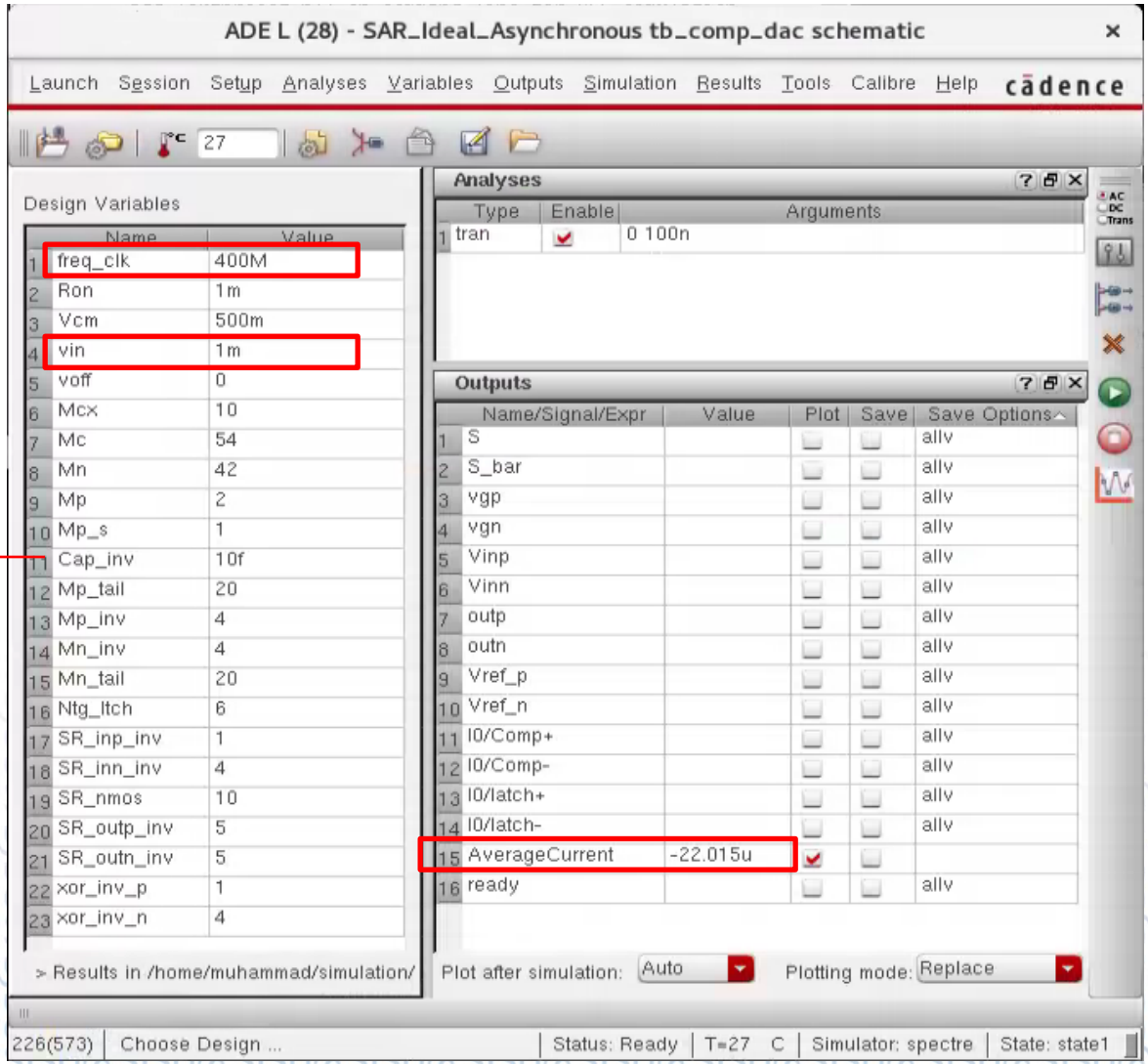

VDD
v_dd
PM4
PM5
PM3
PM2
"gpdk045_pmos1v"
w:120n
l=10*45n
m=Mp
m=Mp_s
out−
out+
in+
in−
NM1
NM7
NM8
"gpdk045_nmos1v"
l=10*45n
m=Mn
dis
I_bias
NM5
NM6
NM3
NM4
PM6
w=2.40n
w=1.2u
l=10*150n
m=Mcx
m=Mc*0.5
Vb
DISABLE
VSS
gndd
*For Partial turn-off

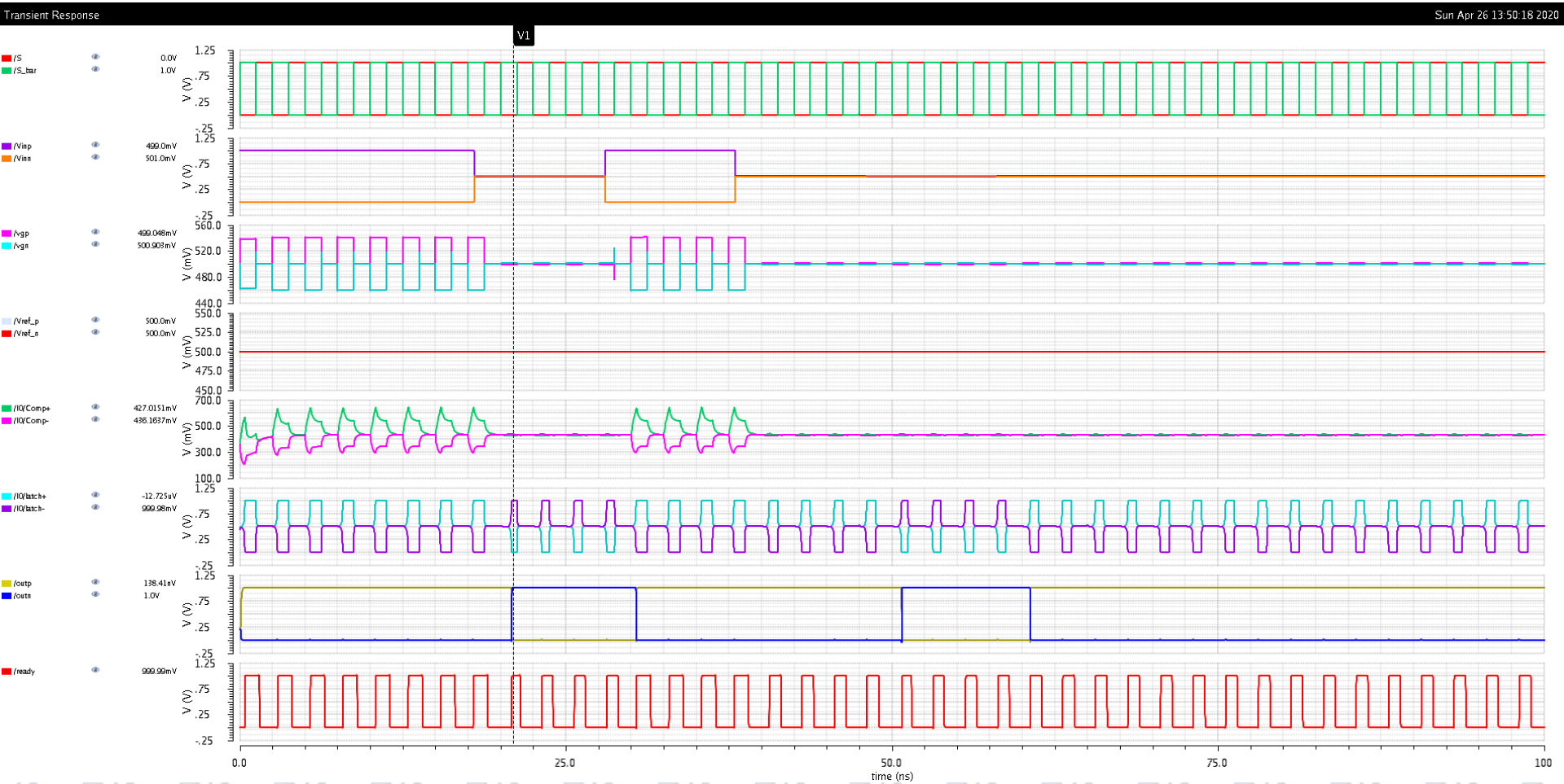
2) Regenerative Latch:



Testbench (parameters)

Removed



Overdrive test

Diff Vin_min = 2 x 1 mV (Smallest Resolution)