Digital Logic for Asynchronous SAR ADC

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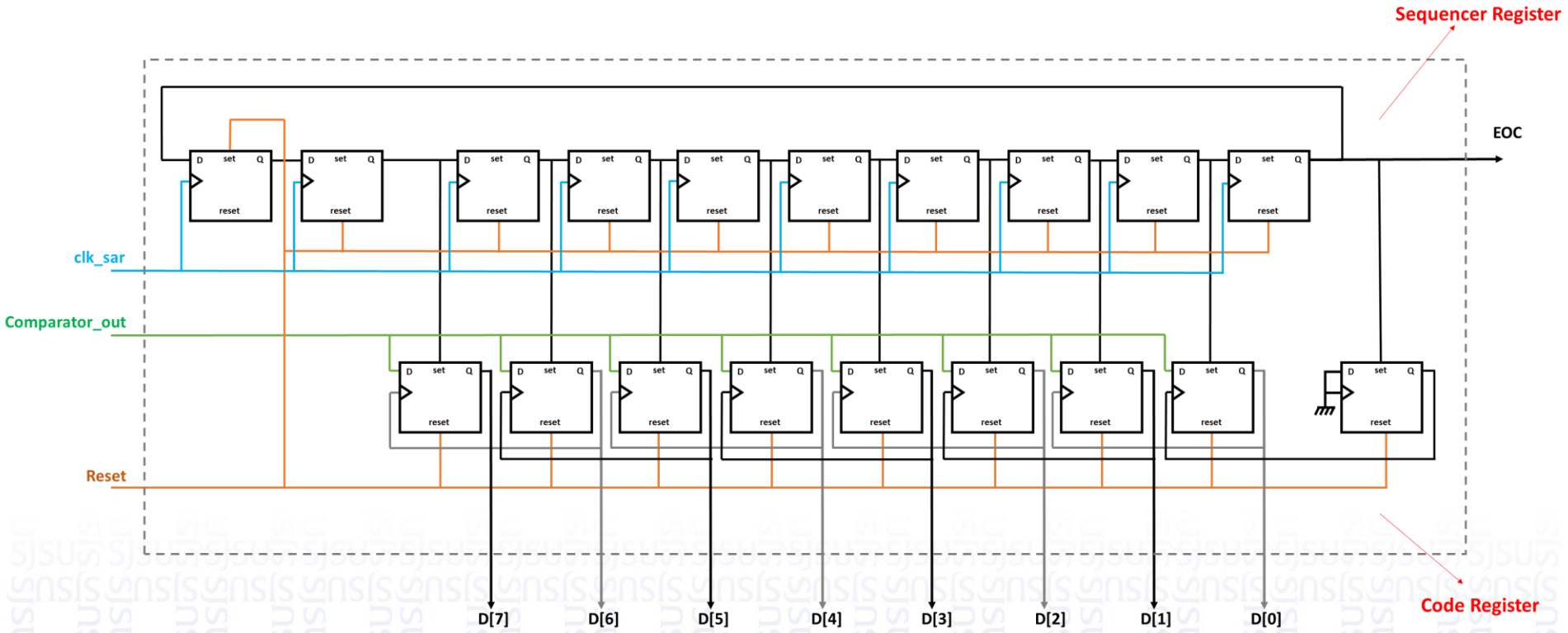
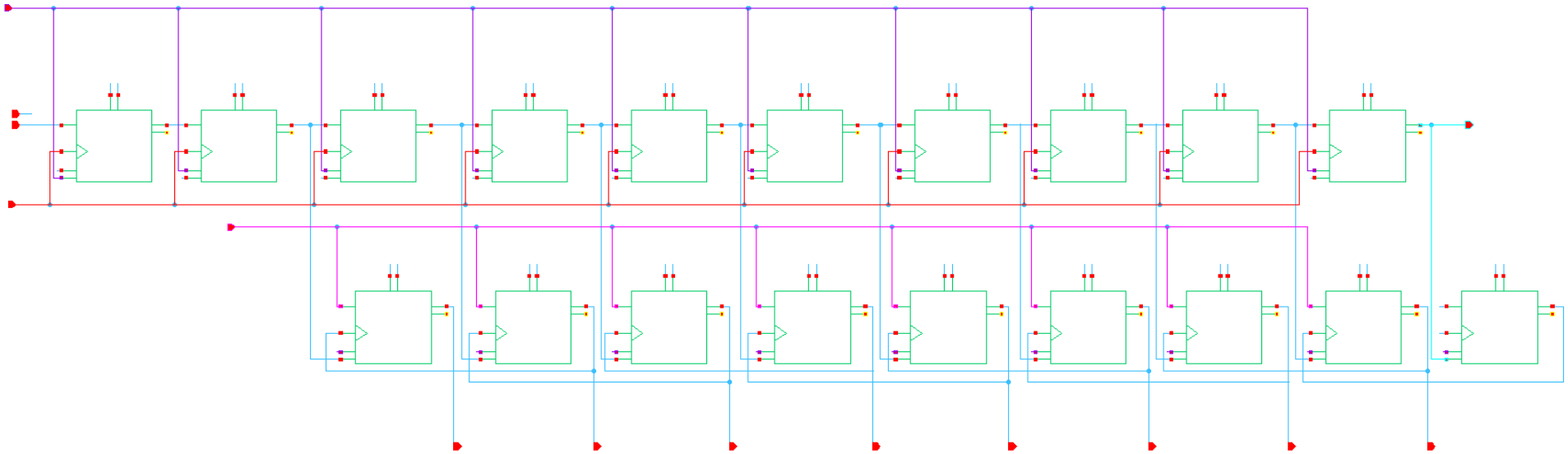
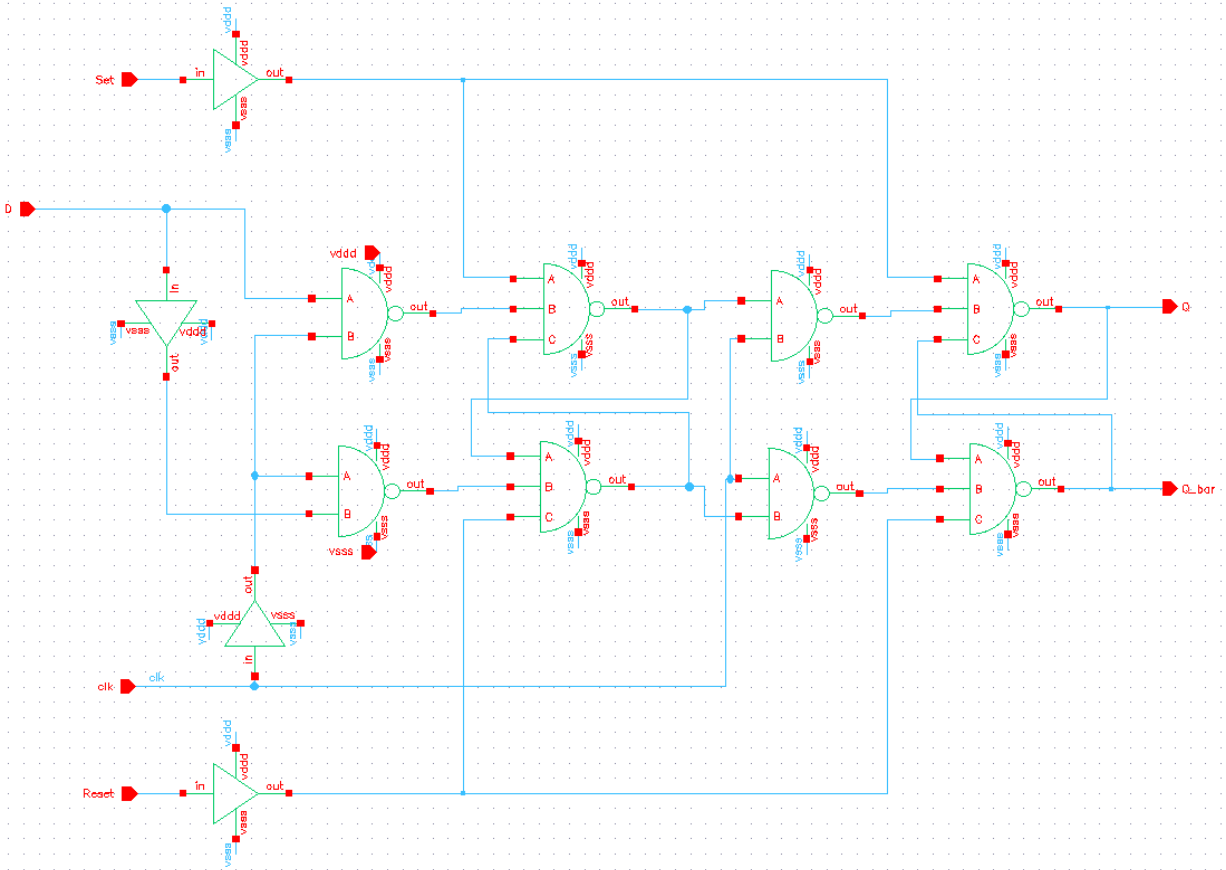
Block Diagram



Schematics

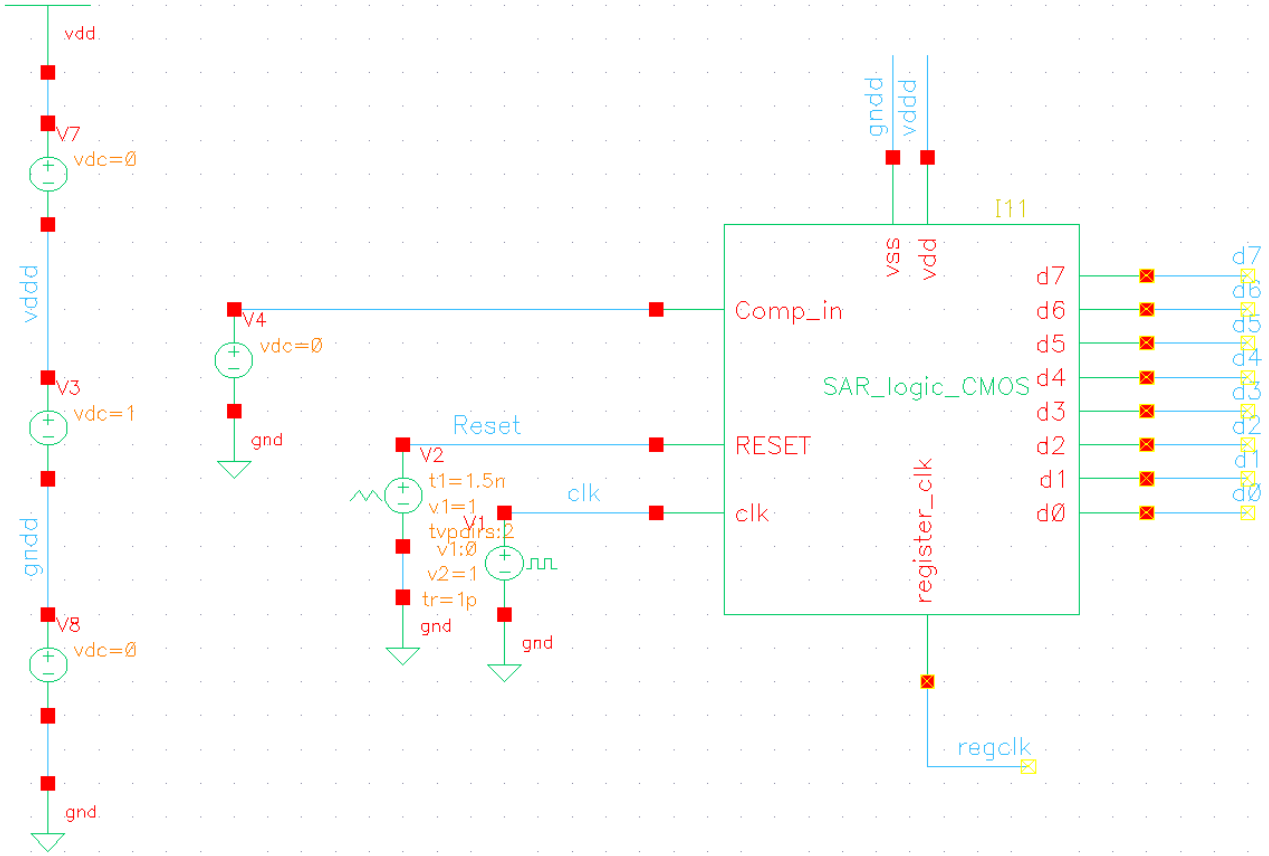


D-flipflop
with asynchronous Set & Reset



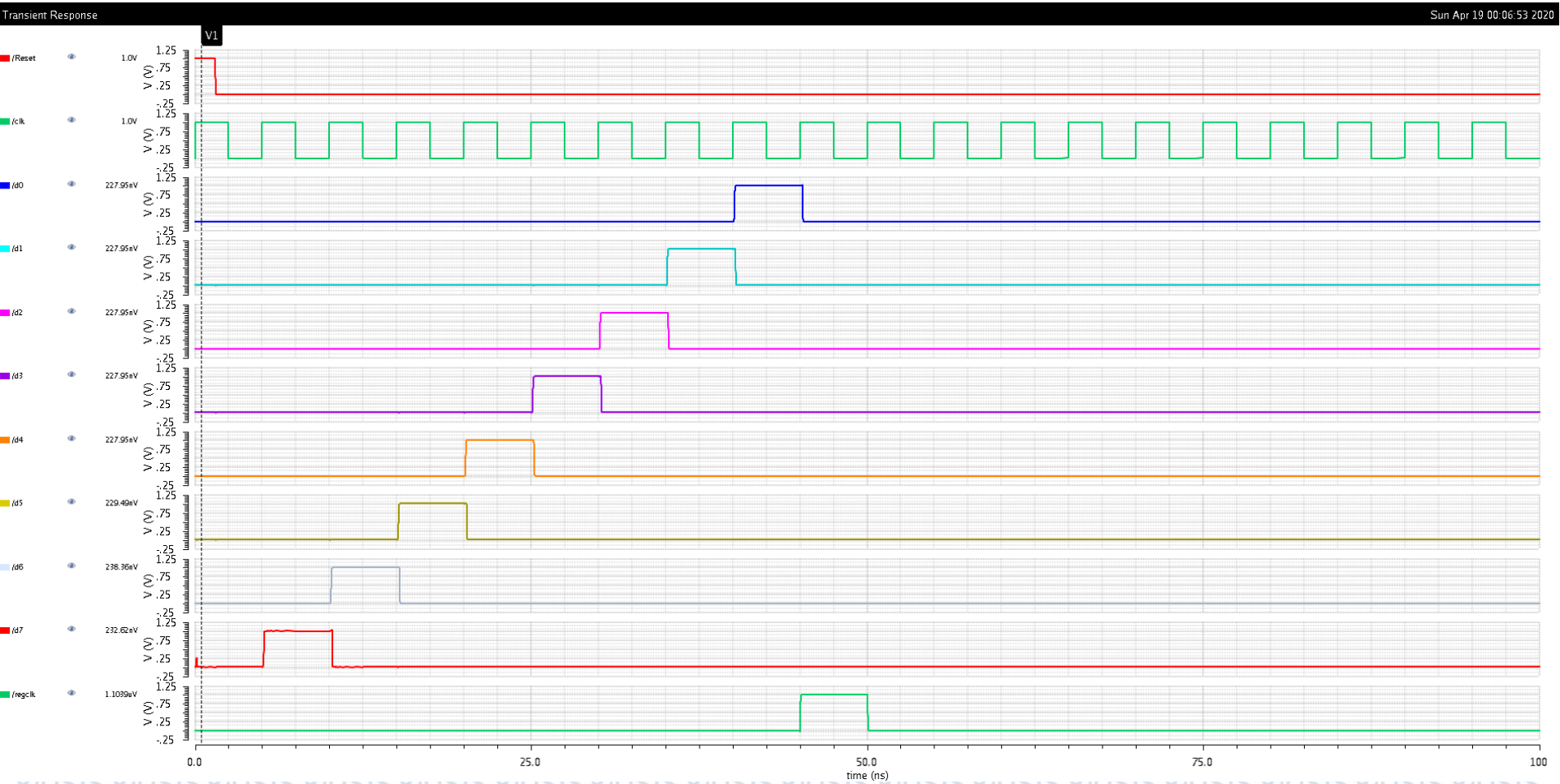
Testbench & Simulations

Testbench


vdd
V7
vdc=0
vddd
V3
vdc=1
gndd
V8
vdc=0
gnd
V4
vdc=0
gnd
Reset
V2
t1=1.5n
v1=1
v1:0
v2=1
tr=1p
gnd
clk
V1
tvpdrs:2
gnd
gndd
vddd
I11
vss
vdd
Comp_in
RESET
clk
SAR_logic_CMOS
register_clk
d7
d6
d5
d4
d3
d2
d1
dØ
regclk

Waveforms

Comp_in = 0



Waveforms

Comp_in = 1