Design of Standing-Wave-based Clock Distribution Network

For 10 GHz Clock

Muhammad Aldacher

Outline

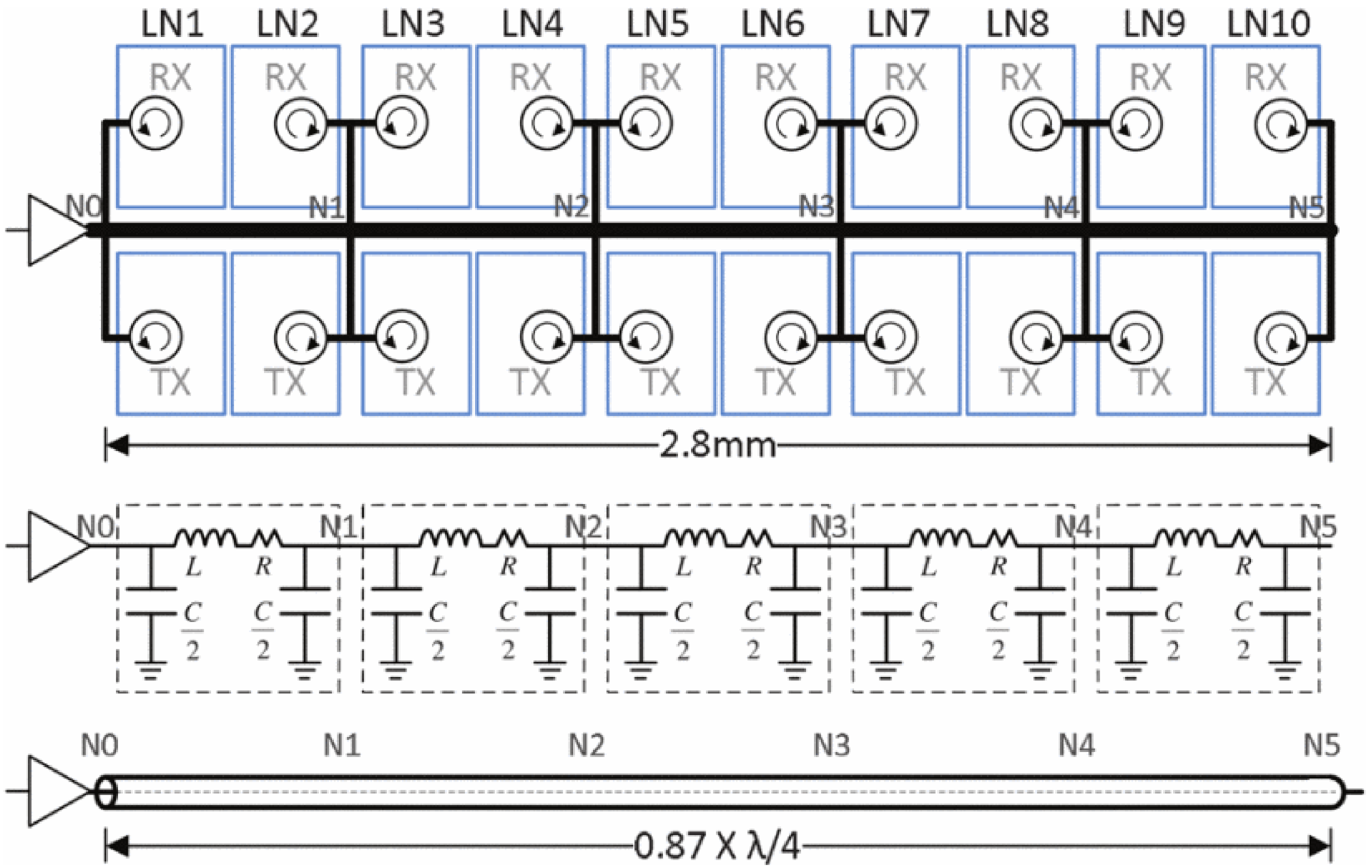
- Description
- Design Implementation
- Testbenches & Simulations
- Conclusion

Description

- This project is about a clock distribution design that distributes a 10 GHz clock to several lanes across a clock channel using a standing wave resonator.

- The main idea of this project is based on the paper: G. Li, W. Lee, D. Cui, B. Zhang, A. Momtaz and J. Cao, "Standing wave based clock distribution technique with application to a 10 × 11 Gbps transceiver in 28 nm CMOS," 2015 IEEE Asian Solid-State Circuits Conference (A-SSCC), Xiamen, China, 2015, pp. 1-4, doi: 10.1109/ASSCC.2015.7387451.

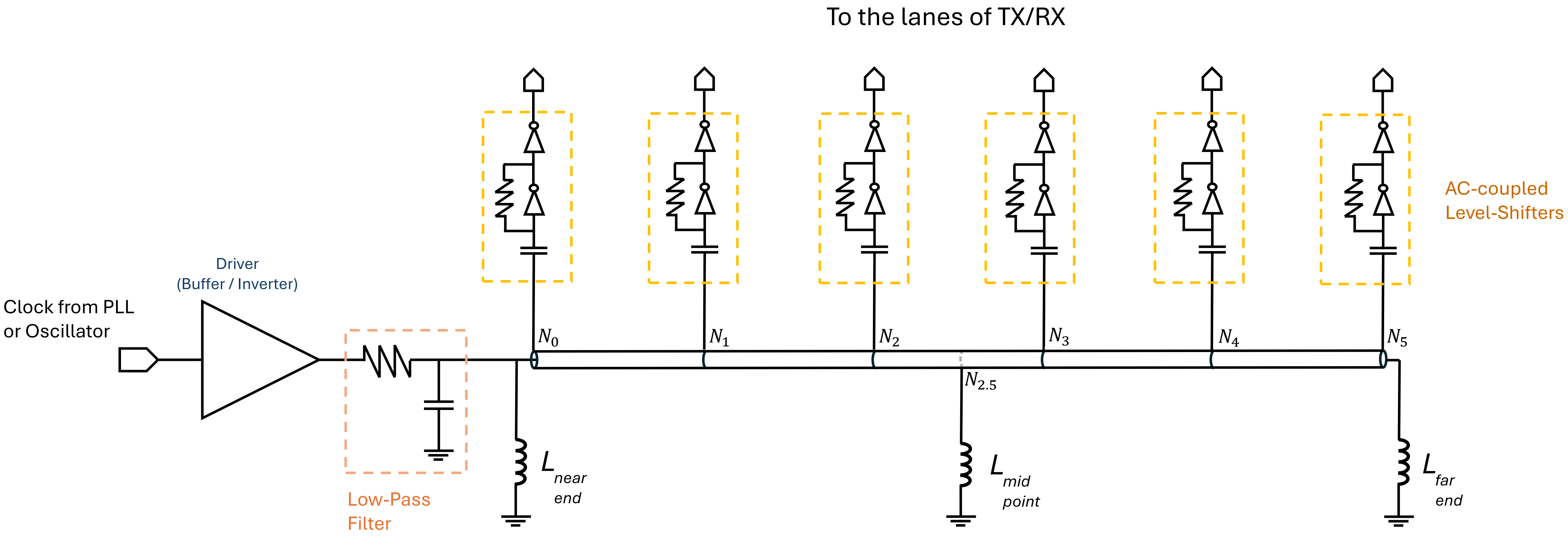
Description



G. Li, W. Lee, D. Cui, B. Zhang, A. Momtaz and J. Cao, "Standing wave based clock distribution technique with application to a 10 × 11 Gbps transceiver in 28 nm CMOS," *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Xiamen, China, 2015, pp. 1-4, doi: 10.1109/ASSCC.2015.7387451.

Design Implementation

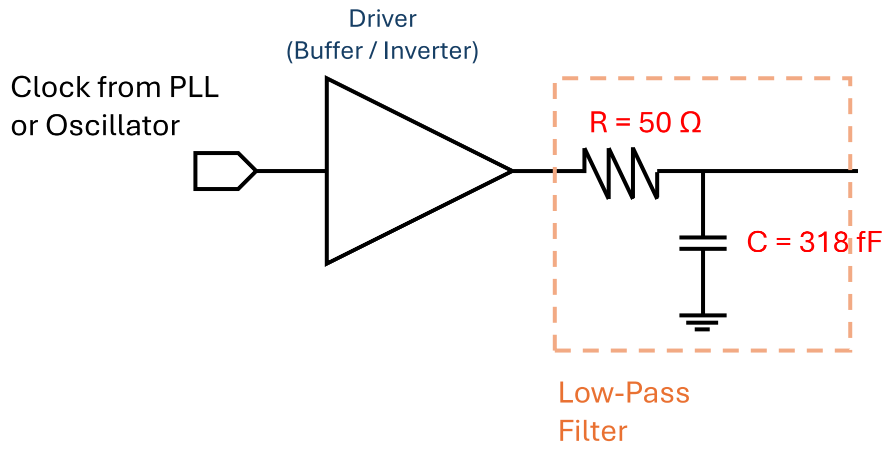
Design Implementation



Design Implementation

1. <u>Input Driver Stage:</u>
   - ➢The Driver is a large inverter to be able to drive a large load.
   - ➢A low-pass filter is used to remove the higher harmonics of the 10 GHz square-wave clock input.

   (A square wave is made up of a fundamental sine wave and odd harmonics of that fundamental. The reflections of the harmonics will cause distortions to the distributed clock signals)

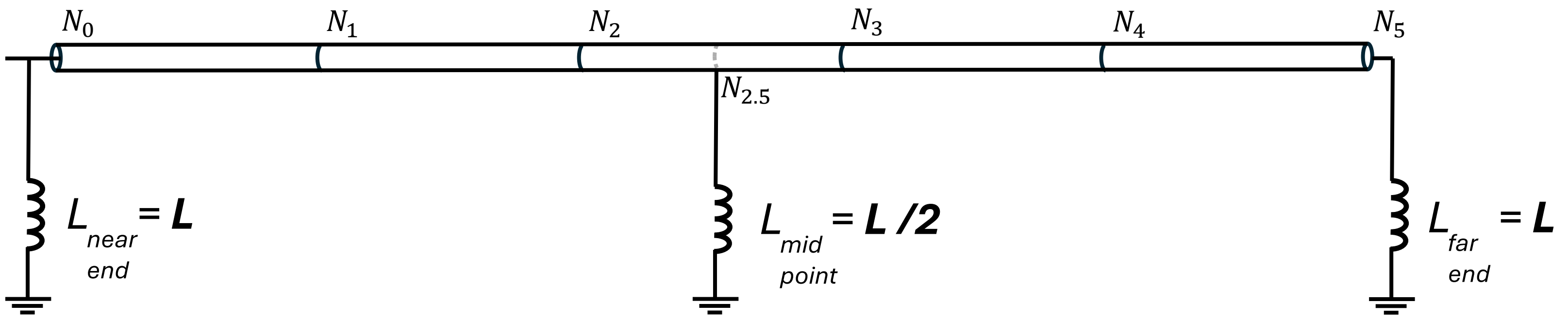


$$f_{LPF} = \frac{1}{2\pi RC} = \frac{1}{2\pi.(50)(318\ x\ 10^{-15})} = 10\ GHz$$

Design Implementation

2. <u>Clock Channel:</u>

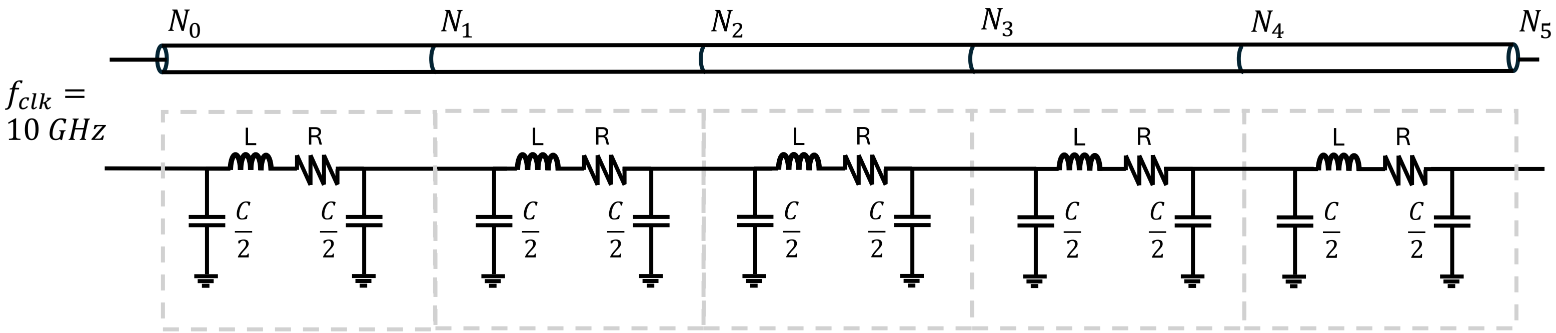
- The clock distribution concept is based on standing waves in a ~ λ/4 transmission line.
- Inductors are used & tuned to ensure reflections form a standing wave & to reduce the voltage-amplitude variation across the transmission line.



Design Implementation

2. <u>Clock Channel:</u>

➢Channel model used:

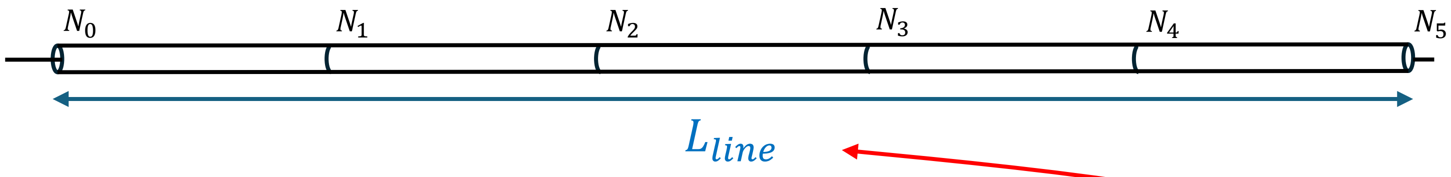


$$L = 100\ {}^{pH}/_{m} \qquad R = 4.5\ {}^{\Omega}/_{m} \qquad C = 190\ {}^{fF}/_{m}$$

Design Implementation

2. <u>Clock Channel:</u>

➢ Calculating the Electrical length of the transmission line (L_{line}):



Phase Velocity:

$$v_p = f_0.\lambda = {}^{1}\!/_{\sqrt{L.C}}$$

Then:

$$\lambda = {}^{1}\!/_{f_0\sqrt{L.C}}$$

$$= {}^{1}\!/_{(10\ GHz)\,.\sqrt{(100\ pH/m)(190\ fF/m)}}$$

$$= \frac{1}{0.0437} = 22.9$$

Phase Shift:

$$\phi = 2\pi.{}^{L_{line}}\!/_{\lambda}$$

Then:

$$\phi_{per\ segment} = 2\pi\left({}^{1}\!/_{22.9}\right) = 0.087\pi$$

$$\phi_{total\ (5\ segments)} = 2\pi\left({}^{5}\!/_{22.9}\right) = 0.87\frac{\pi}{2}$$

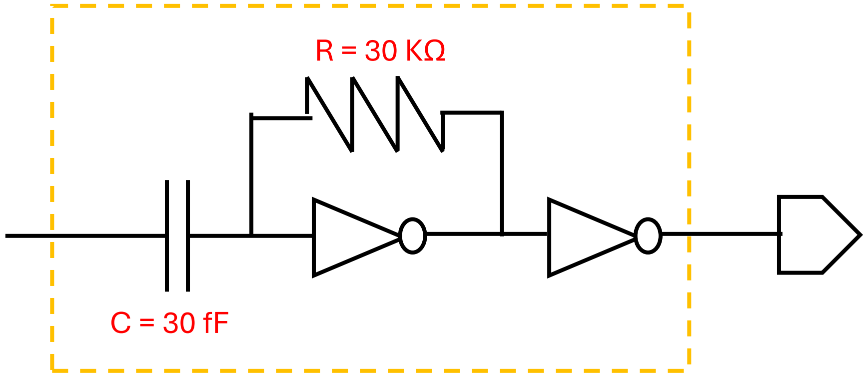
$$L_{line} = \frac{\lambda\ \phi_{total}}{2\pi} = \frac{\lambda}{2\pi}.\left(0.87\frac{\pi}{2}\right) = 0.87\frac{\lambda}{4}$$

Design Implementation

3. <u>Output Level-Shifters:</u>

➢The AC-coupled Level-Shifters blocks the DC-level of the input signal & passes the 10 GHz AC clock signal.

➢The DC-level is set to VDD/2 by the resistor in the loop.



$$f_{HPF} = \frac{1}{2\pi RC} \quad < 10GHz$$

➢R → increased to reduce the leakage & for output to be rail-to-rail.

➢C → should be high enough to pass the 10GHz, but low enough so it won't load the transmission line a lot.

Testbenches & Simulations

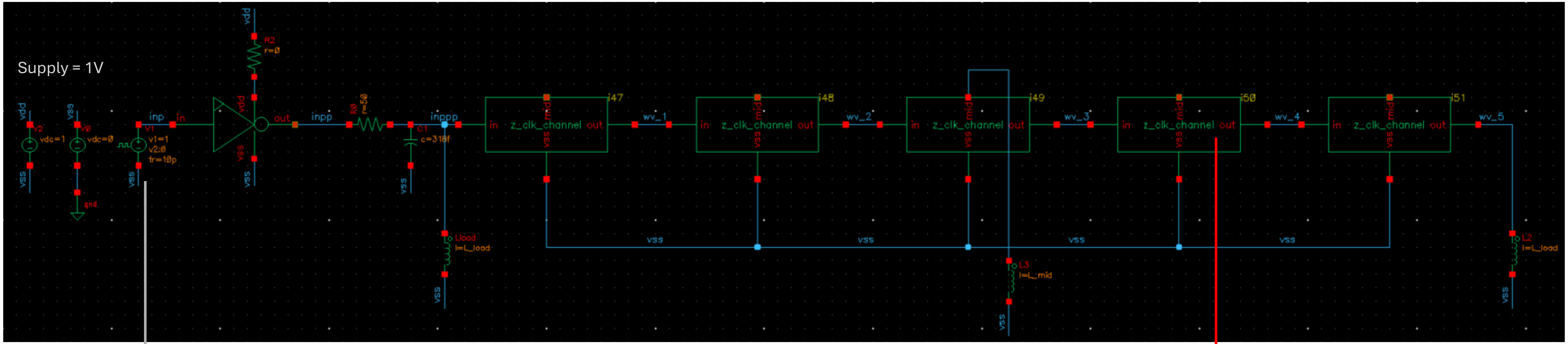
TB1:
Standing Wave Simulations

- Objective:

  - ➢ In TB1, the values of the inductors are swept & chosen:
    - ➢ To ensure the standing wave occurs with minimum distortion
    - ➢ To achieve the highest voltage-amplitudes with minimum variation across the channel.

TB1:
Standing Wave Simulations

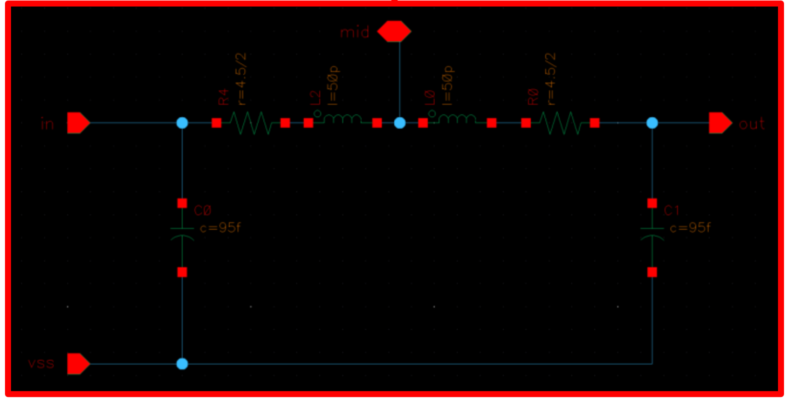
- Schematics



Library Name	analogLib
Cell Name	vpulse
View Name	symbol

Voltage 1	1 V
Voltage 2	0 V
Period	100.0p s
Delay time	1n s
Rise time	10p s
Fall time	10p s
Pulse width	40p s

1-segment:



TB1:

Standing Wave Simulations

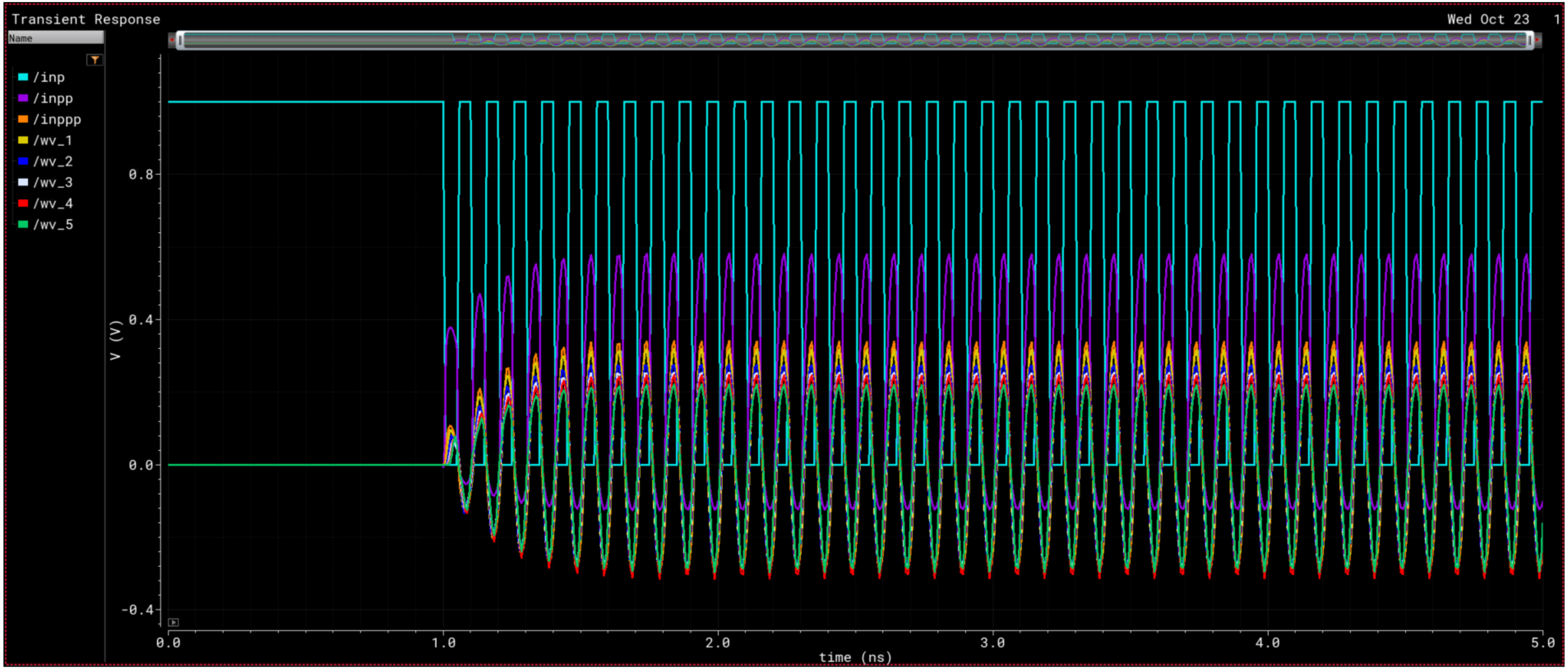
- Setup & Measurements

Name	Value
Filter	Filter
Tests	
Transient	
Simulator	spectre
Analyses	
tran	0 5n
Click to add analysis	
Design Variables	
Click to add test	
Global Variables	
L_load	2*L_mid
L_mid	390p

Name	Type	Details	EvalType	Plot	Save
Filter	Filter	Filter	Filter		
	signal	/inp	point	✓	✓
	signal	/inpp	point	✓	✓
	signal	/inppp	point	✓	✓
	signal	/wv_1	point	✓	✓
	signal	/wv_2	point	✓	✓
	signal	/wv_3	point	✓	✓
	signal	/wv_4	point	✓	✓
	signal	/wv_5	point	✓	✓
p_wv0_max	expr	value(VT("/inppp") xmax(clip(VT("/inppp") 4.5e-09 5e-09) 1))	point	✓	
p_wv1_max	expr	value(VT("/wv_1") xmax(clip(VT("/wv_1") 4.5e-09 5e-09) 1))	point	✓	
p_wv2_max	expr	value(VT("/wv_2") xmax(clip(VT("/wv_2") 4.5e-09 5e-09) 1))	point	✓	
p_wv3_max	expr	value(VT("/wv_3") xmax(clip(VT("/wv_3") 4.5e-09 5e-09) 1))	point	✓	
p_wv4_max	expr	value(VT("/wv_4") xmax(clip(VT("/wv_4") 4.5e-09 5e-09) 1))	point	✓	
p_wv5_max	expr	value(VT("/wv_5") xmax(clip(VT("/wv_5") 4.5e-09 5e-09) 1))	point	✓	
p_wv0_min	expr	value(VT("/inppp") xmin(clip(VT("/inppp") 4.5e-09 5e-09) 1))	point	✓	
p_wv1_min	expr	value(VT("/wv_1") xmin(clip(VT("/wv_1") 4.5e-09 5e-09) 1))	point	✓	
p_wv2_min	expr	value(VT("/wv_2") xmin(clip(VT("/wv_2") 4.5e-09 5e-09) 1))	point	✓	
p_wv3_min	expr	value(VT("/wv_3") xmin(clip(VT("/wv_3") 4.5e-09 5e-09) 1))	point	✓	
p_wv4_min	expr	value(VT("/wv_4") xmin(clip(VT("/wv_4") 4.5e-09 5e-09) 1))	point	✓	
p_wv5_min	expr	value(VT("/wv_5") xmin(clip(VT("/wv_5") 4.5e-09 5e-09) 1))	point	✓	
wv0_amp	expr	(p_wv0_max - p_wv0_min)	point	✓	
wv1_amp	expr	(p_wv1_max - p_wv1_min)	point	✓	
wv2_amp	expr	(p_wv2_max - p_wv2_min)	point	✓	
wv3_amp	expr	(p_wv3_max - p_wv3_min)	point	✓	
wv4_amp	expr	(p_wv4_max - p_wv4_min)	point	✓	
wv5_amp	expr	(p_wv5_max - p_wv5_min)	point	✓	

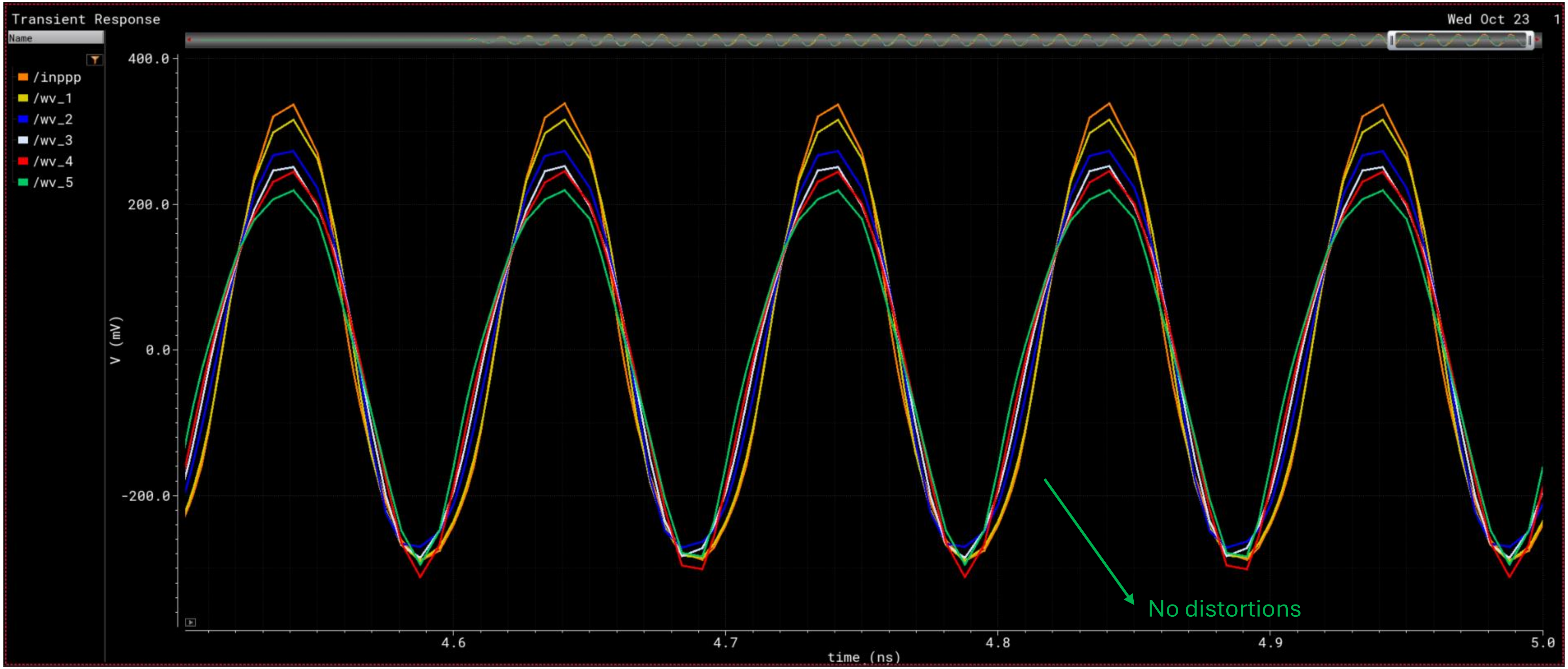
TB1:
Standing Wave Simulations

- Waveforms



TB1:
Standing Wave Simulations

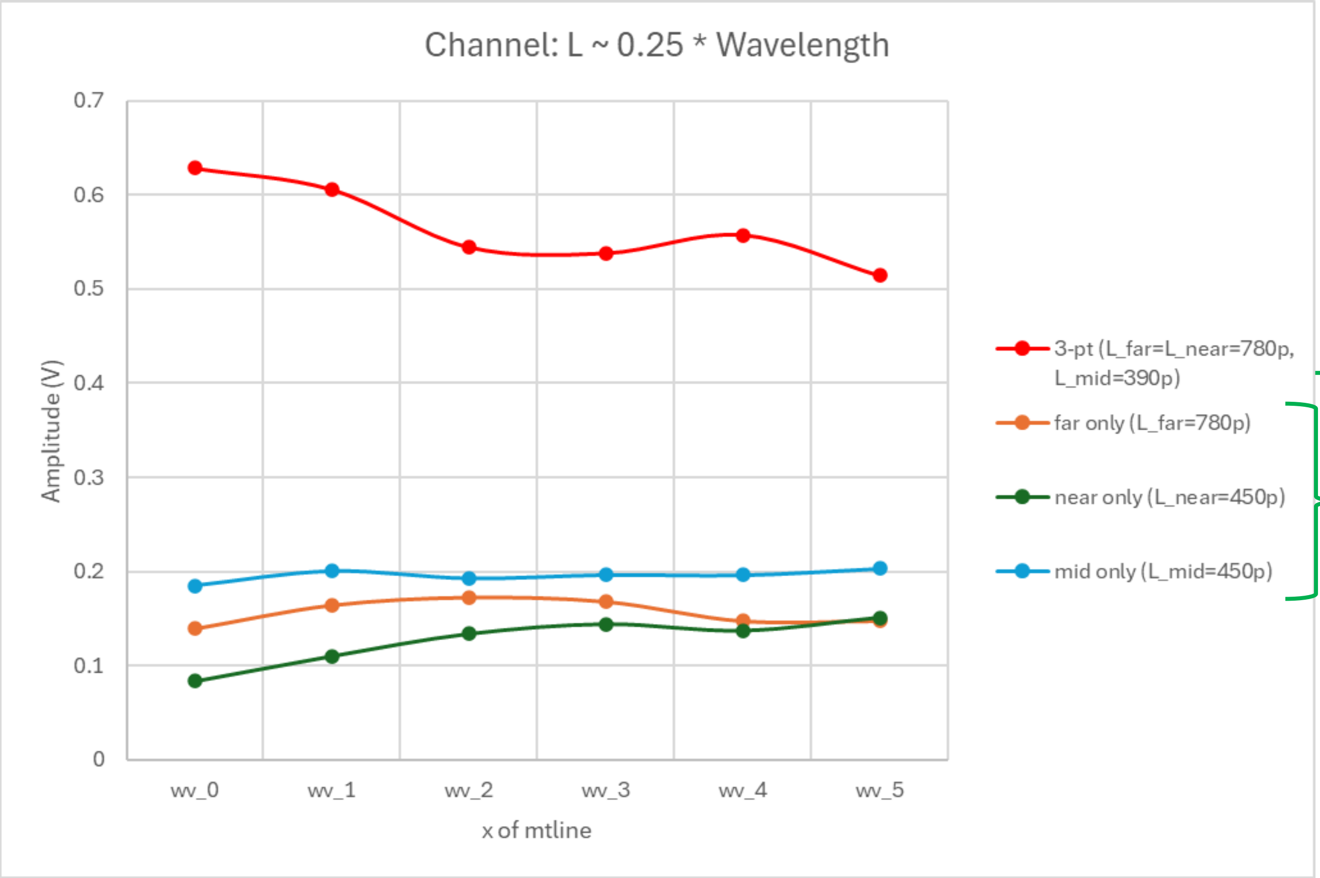
- Waveforms



TB1:
Standing Wave Simulations

- Results:
  Voltage Amplitudes at each point on the transmission line

$$L_{far\ end} = 780pH$$
$$L_{near\ end} = 780pH$$
$$L_{mid\ point} = 390pH$$



3 Ls used

1 L used at a time

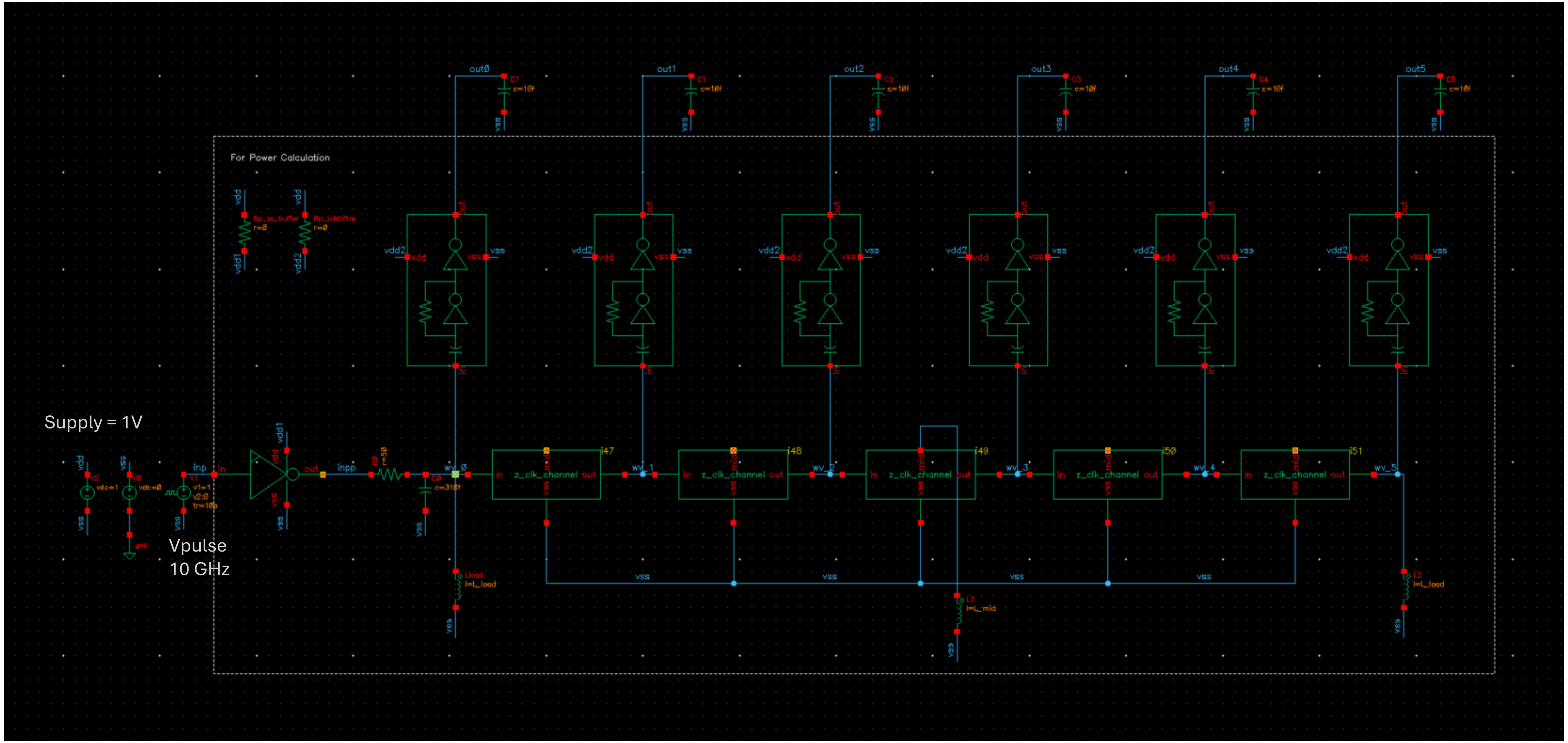
TB2:
Whole System Simulations

- Objective:

  - ➢ In TB2, the outputs of each node at each stage are monitored:
    - ➢ To ensure the amplitudes are large enough for the following stages (Inverters are sized to strengthen the signals)

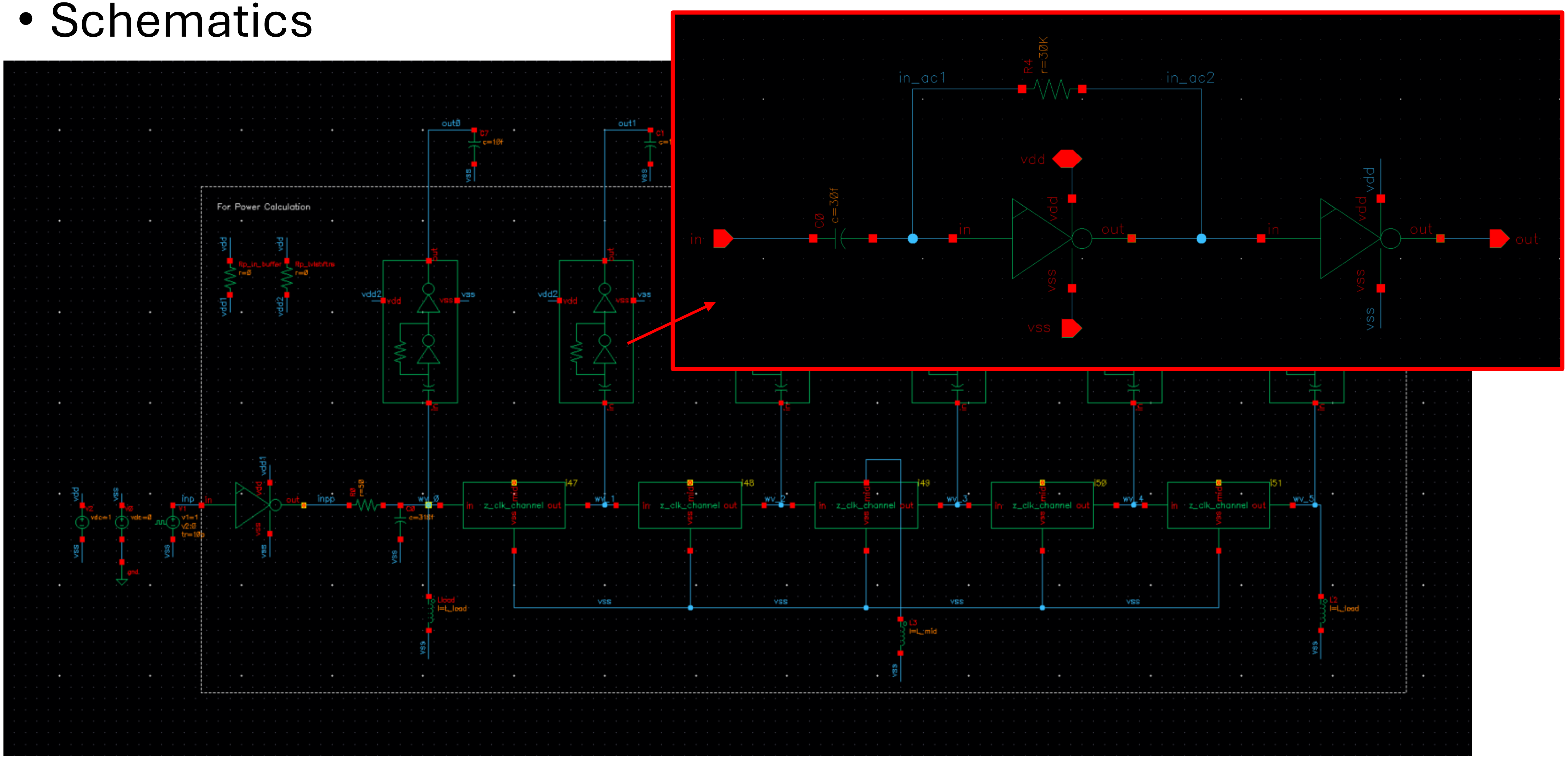
TB2:
Whole System Simulations

- Schematics



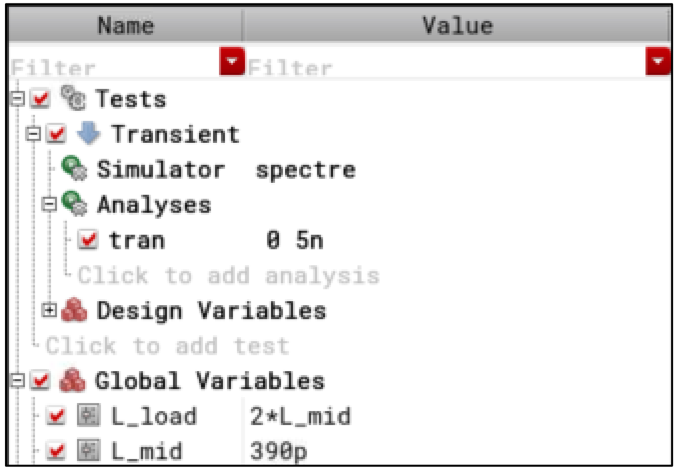
TB2:
Whole System Simulations

- Schematics



TB2:
Whole System Simulations

- Setup



TB2:
Whole System Simulations

- Measurements

Name	Type	Details	Spec
Filter	Filter	Filter	Filter
*** Transmission Line	expr		
	signal	/inp	
	signal	/inpp	
	signal	/wv_0	
	signal	/wv_1	
	signal	/wv_2	
	signal	/wv_3	
	signal	/wv_4	
	signal	/wv_5	
amp_wv0	expr	peakToPeak(clip(VT("/wv_0") 4.5e-09 5e-09))	> 0.5
amp_wv1	expr	peakToPeak(clip(VT("/wv_1") 4.5e-09 5e-09))	> 0.5
amp_wv2	expr	peakToPeak(clip(VT("/wv_2") 4.5e-09 5e-09))	> 0.5
amp_wv3	expr	peakToPeak(clip(VT("/wv_3") 4.5e-09 5e-09))	> 0.5
amp_wv4	expr	peakToPeak(clip(VT("/wv_4") 4.5e-09 5e-09))	> 0.5
amp_wv5	expr	peakToPeak(clip(VT("/wv_5") 4.5e-09 5e-09))	> 0.5

TB2:
Whole System Simulations

- Measurements

Name	Type	Details	Spec
Filter	Filter	Filter	Filter
*** Output Level-Shifters	expr		
	signal	/ilvlshftr0/in_ac1	
	signal	/ilvlshftr1/in_ac1	
	signal	/ilvlshftr2/in_ac1	
	signal	/ilvlshftr3/in_ac1	
	signal	/ilvlshftr4/in_ac1	
	signal	/ilvlshftr5/in_ac1	
amp_lvlshft0_ac1	expr	peakToPeak(clip(VT("/ilvlshftr0/in_ac1") 4.5e-09 5e-09))	> 0.5
amp_lvlshft1_ac1	expr	peakToPeak(clip(VT("/ilvlshftr1/in_ac1") 4.5e-09 5e-09))	> 0.5
amp_lvlshft2_ac1	expr	peakToPeak(clip(VT("/ilvlshftr2/in_ac1") 4.5e-09 5e-09))	> 0.5
amp_lvlshft3_ac1	expr	peakToPeak(clip(VT("/ilvlshftr3/in_ac1") 4.5e-09 5e-09))	> 0.5
amp_lvlshft4_ac1	expr	peakToPeak(clip(VT("/ilvlshftr4/in_ac1") 4.5e-09 5e-09))	> 0.5
amp_lvlshft5_ac1	expr	peakToPeak(clip(VT("/ilvlshftr5/in_ac1") 4.5e-09 5e-09))	> 0.5
	signal	/ilvlshftr0/in_ac2	
	signal	/ilvlshftr1/in_ac2	
	signal	/ilvlshftr2/in_ac2	
	signal	/ilvlshftr3/in_ac2	
	signal	/ilvlshftr4/in_ac2	
	signal	/ilvlshftr5/in_ac2	
amp_lvlshft0_ac2	expr	peakToPeak(clip(VT("/ilvlshftr0/in_ac2") 4.5e-09 5e-09))	> 0.5
amp_lvlshft1_ac2	expr	peakToPeak(clip(VT("/ilvlshftr1/in_ac2") 4.5e-09 5e-09))	> 0.5
amp_lvlshft2_ac2	expr	peakToPeak(clip(VT("/ilvlshftr2/in_ac2") 4.5e-09 5e-09))	> 0.5
amp_lvlshft3_ac2	expr	peakToPeak(clip(VT("/ilvlshftr3/in_ac2") 4.5e-09 5e-09))	> 0.5
amp_lvlshft4_ac2	expr	peakToPeak(clip(VT("/ilvlshftr4/in_ac2") 4.5e-09 5e-09))	> 0.5
amp_lvlshft5_ac2	expr	peakToPeak(clip(VT("/ilvlshftr5/in_ac2") 4.5e-09 5e-09))	> 0.5

TB2:
Whole System Simulations

- Measurements

Name	Type	Details	Spec
Filter	Filter	Filter	Filter
*** Outputs	expr		
	signal	/out0	
	signal	/out1	
	signal	/out2	
	signal	/out3	
	signal	/out4	
	signal	/out5	
amp_out0	expr	peakToPeak(clip(VT("/out0") 4.5e-09 5e-09))	> 0.5
amp_out1	expr	peakToPeak(clip(VT("/out1") 4.5e-09 5e-09))	> 0.5
amp_out2	expr	peakToPeak(clip(VT("/out2") 4.5e-09 5e-09))	> 0.5
amp_out3	expr	peakToPeak(clip(VT("/out3") 4.5e-09 5e-09))	> 0.5
amp_out4	expr	peakToPeak(clip(VT("/out4") 4.5e-09 5e-09))	> 0.5
amp_out5	expr	peakToPeak(clip(VT("/out5") 4.5e-09 5e-09))	> 0.5
freq_out0	expr	average(clip(freq(VT("/out0") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 3e-09 4e-09))	
freq_out1	expr	average(clip(freq(VT("/out1") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 3e-09 4e-09))	
freq_out2	expr	average(clip(freq(VT("/out2") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 3e-09 4e-09))	
freq_out3	expr	average(clip(freq(VT("/out3") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 3e-09 4e-09))	
freq_out4	expr	average(clip(freq(VT("/out4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 3e-09 4e-09))	
freq_out5	expr	average(clip(freq(VT("/out5") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 3e-09 4e-09))	
dutycycle_out0	expr	average(clip(dutyCycle(VT("/out0") ?mode "auto" ?xName "time" ?outputType "plot") 3e-09 4e-09))	range 47 | 53
dutycycle_out1	expr	average(clip(dutyCycle(VT("/out1") ?mode "auto" ?xName "time" ?outputType "plot") 3e-09 4e-09))	range 47 | 53
dutycycle_out2	expr	average(clip(dutyCycle(VT("/out2") ?mode "auto" ?xName "time" ?outputType "plot") 3e-09 4e-09))	range 47 | 53
dutycycle_out3	expr	average(clip(dutyCycle(VT("/out3") ?mode "auto" ?xName "time" ?outputType "plot") 3e-09 4e-09))	range 47 | 53
dutycycle_out4	expr	average(clip(dutyCycle(VT("/out4") ?mode "auto" ?xName "time" ?outputType "plot") 3e-09 4e-09))	range 47 | 53
dutycycle_out5	expr	average(clip(dutyCycle(VT("/out5") ?mode "auto" ?xName "time" ?outputType "plot") 3e-09 4e-09))	range 47 | 53

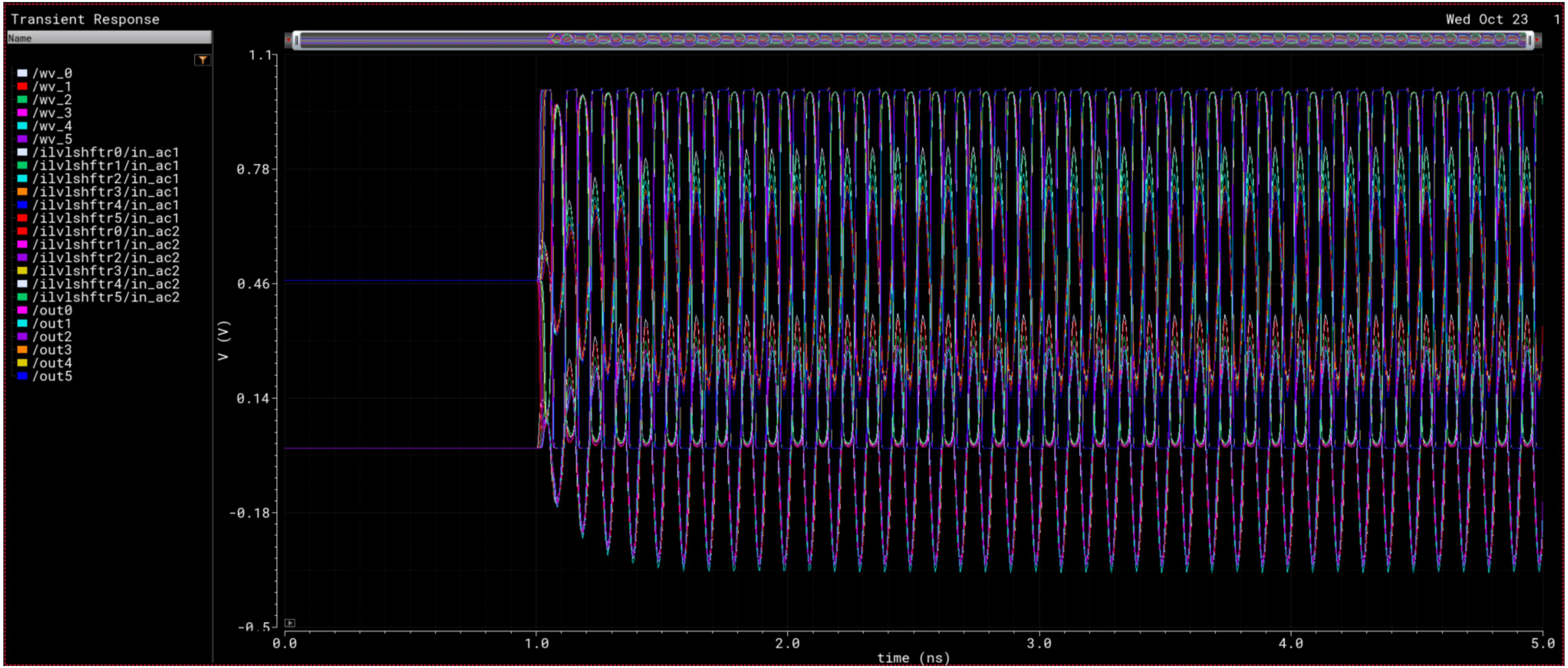
TB2:
Whole System Simulations

- Measurements

Name	Type	Details	Spec
Filter	Filter	Filter	Filter
*** Powers	expr		
/Rp_in_buffer/PLUS_I	signal …	/Rp_in_buffer/PLUS	
/Rp_lvlshftrs/PLUS_I	signal …	/Rp_lvlshftrs/PLUS	
Current_in_buffer	expr	average(IT("/Rp_in_buffer/PLUS"))	
Current_out_lvl_shftrs	expr	average(IT("/Rp_lvlshftrs/PLUS"))	

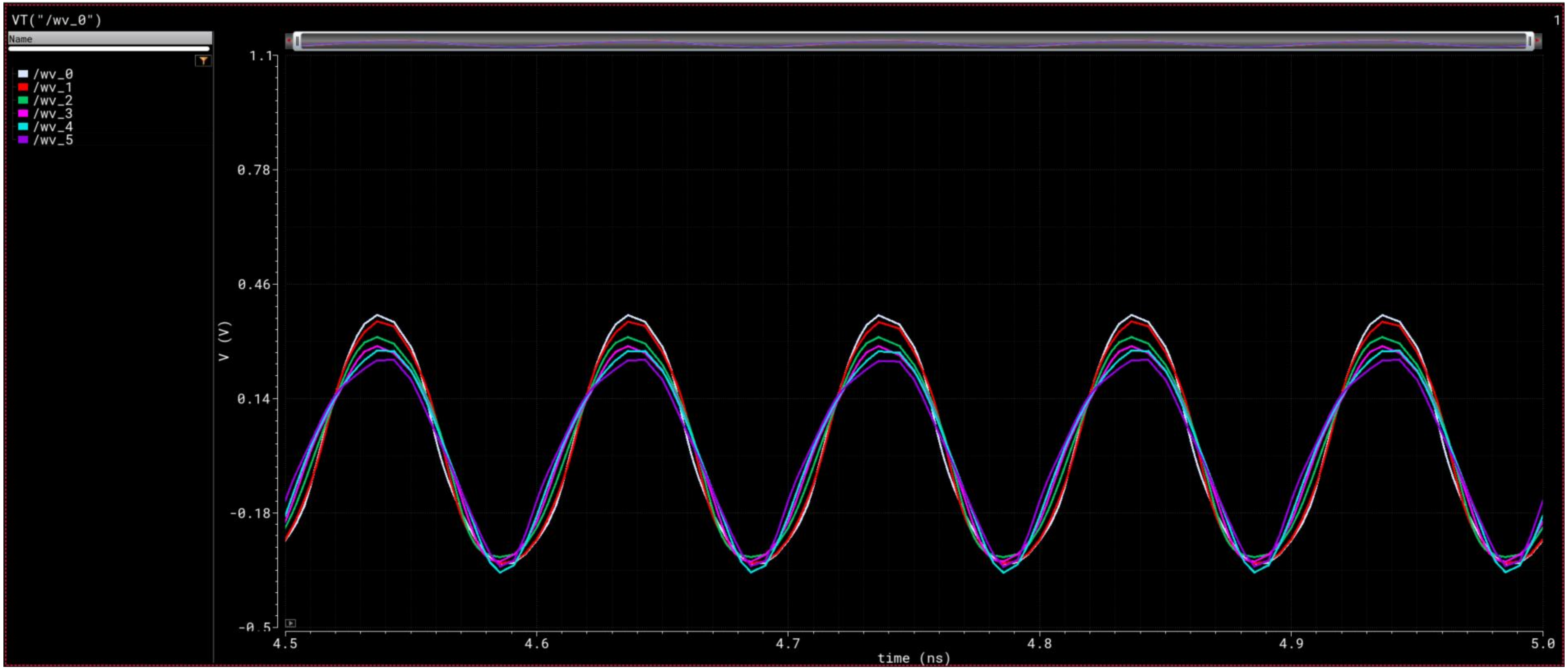
TB2:
Whole System Simulations

- Waveforms



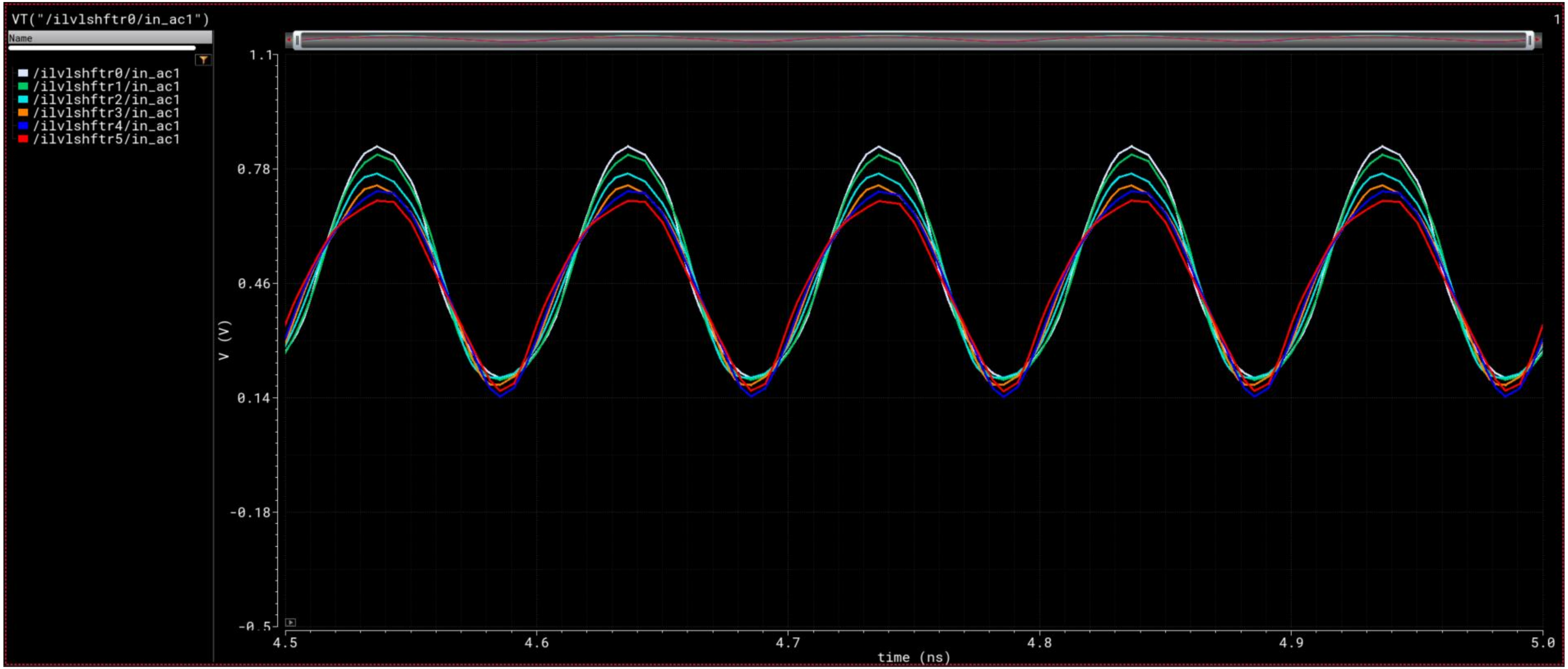
TB2:
Whole System Simulations

- Waveforms (Outputs of the channel)



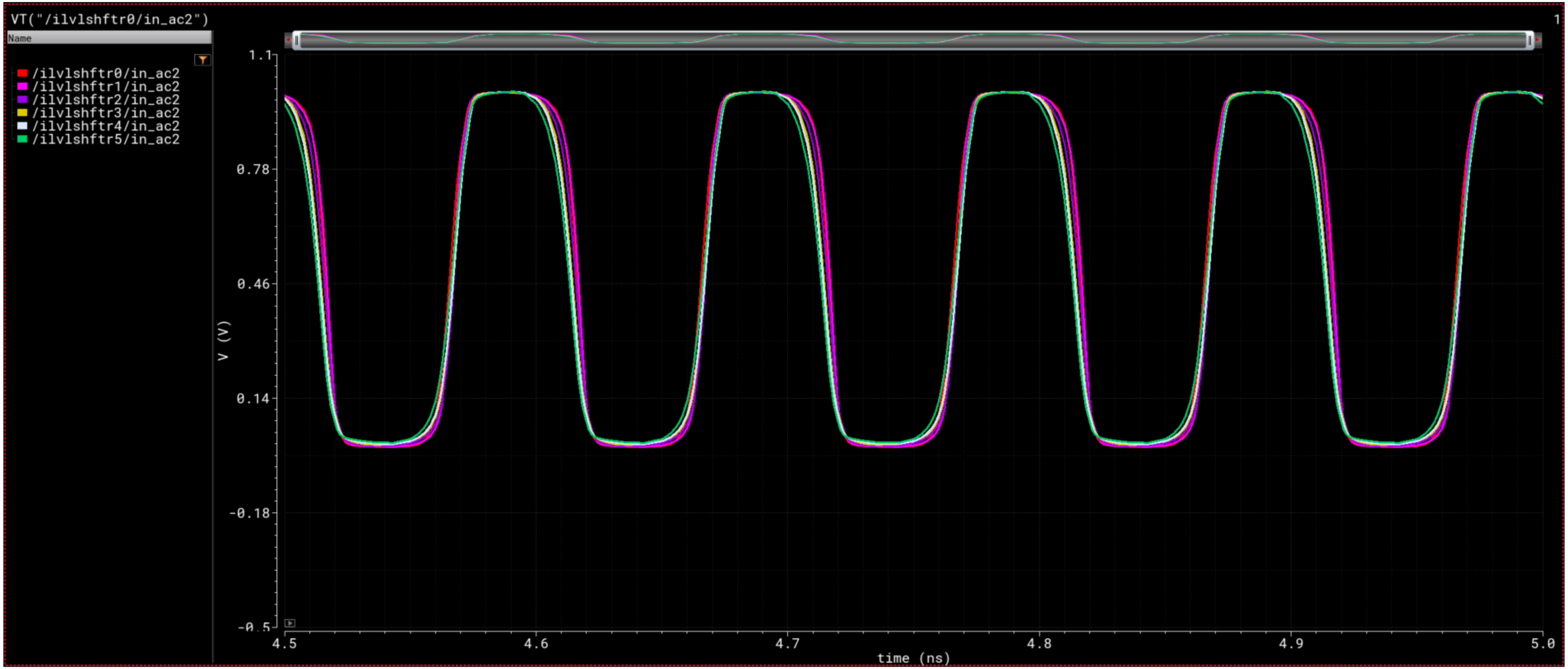
TB2:
Whole System Simulations

- Waveforms (After Coupling Caps)



TB2:
Whole System Simulations

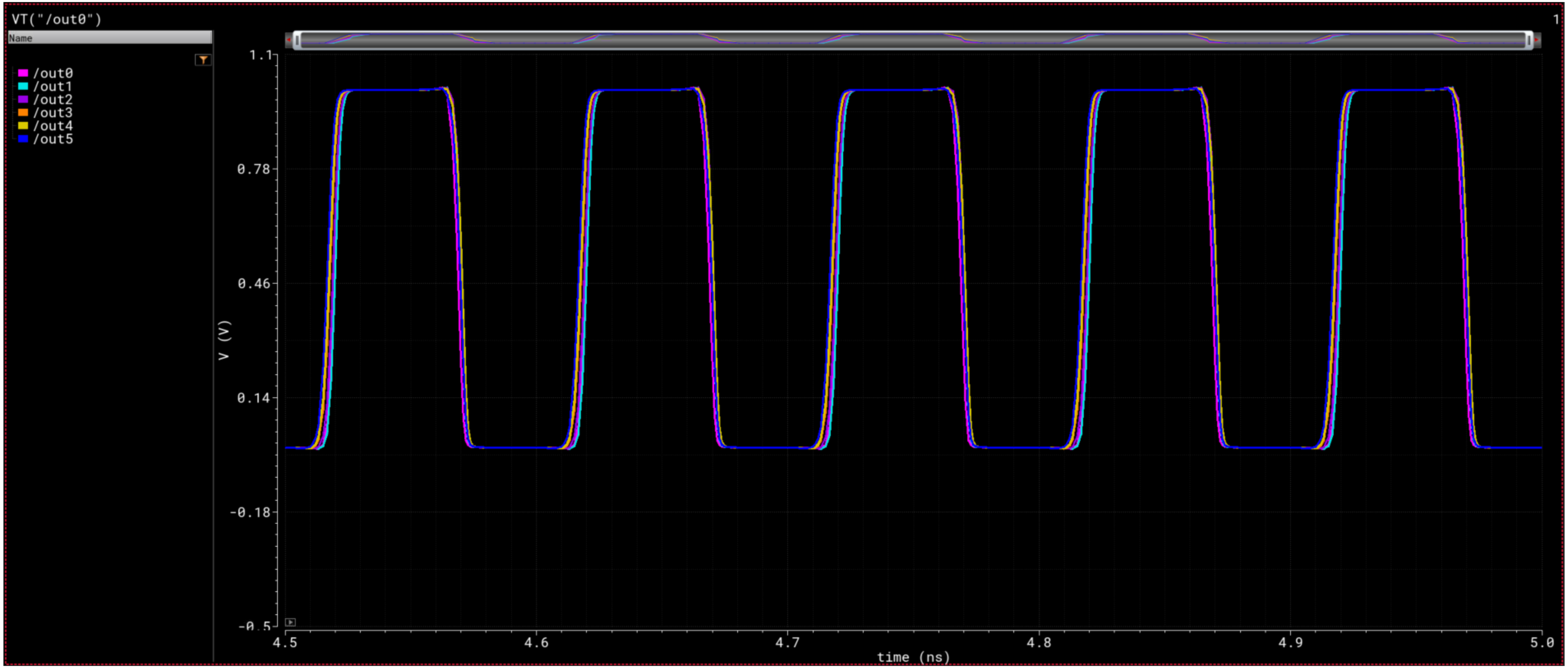
- Waveforms (After 1st Inverter of the output stage)



TB2:

Whole System Simulations

- Waveforms (After 2nd Inverter of the output stage)



TB2:
Whole System Simulations

- Results:

		Voltage Amplitudes (V)			
	SPEC (V)	Outputs of transmission line	After Coupling Caps	After 1st INV (Output stage)	After 2nd INV (Output stage)
N0	500m	696.5m	647.7m	989.3m	1.01
N1	500m	676.8m	629.9m	988.9m	1.01
N2	500m	615.4m	570.9m	985.9m	1.008
N3	500m	602.6m	558.5m	984.8m	1.008
N4	500m	621m	575.3m	984.7m	1.007
N5	500m	579.1m	533.1m	980.8m	1.006

TB2:
Whole System Simulations

- Results:

		Frequency (Hz)
	SPEC (Hz)	After 2nd INV (Output stage)
N0	10G	10G
N1	10G	10G
N2	10G	10G
N3	10G	10G
N4	10G	10G
N5	10G	10G

		Duty-Cycle (%)
	SPEC (%)	After 2nd INV (Output stage)
N0	47 ~ 53	49.36
N1	47 ~ 53	49.85
N2	47 ~ 53	51.06
N3	47 ~ 53	52.18
N4	47 ~ 53	52.58
N5	47 ~ 53	52.63

	Current Consumption (A)
Input Buffer	2.443 mA
Output Level-Shifters	6 x 0.55 mA
Total	**5.743 mA**

TB3:
Jitter Simulations

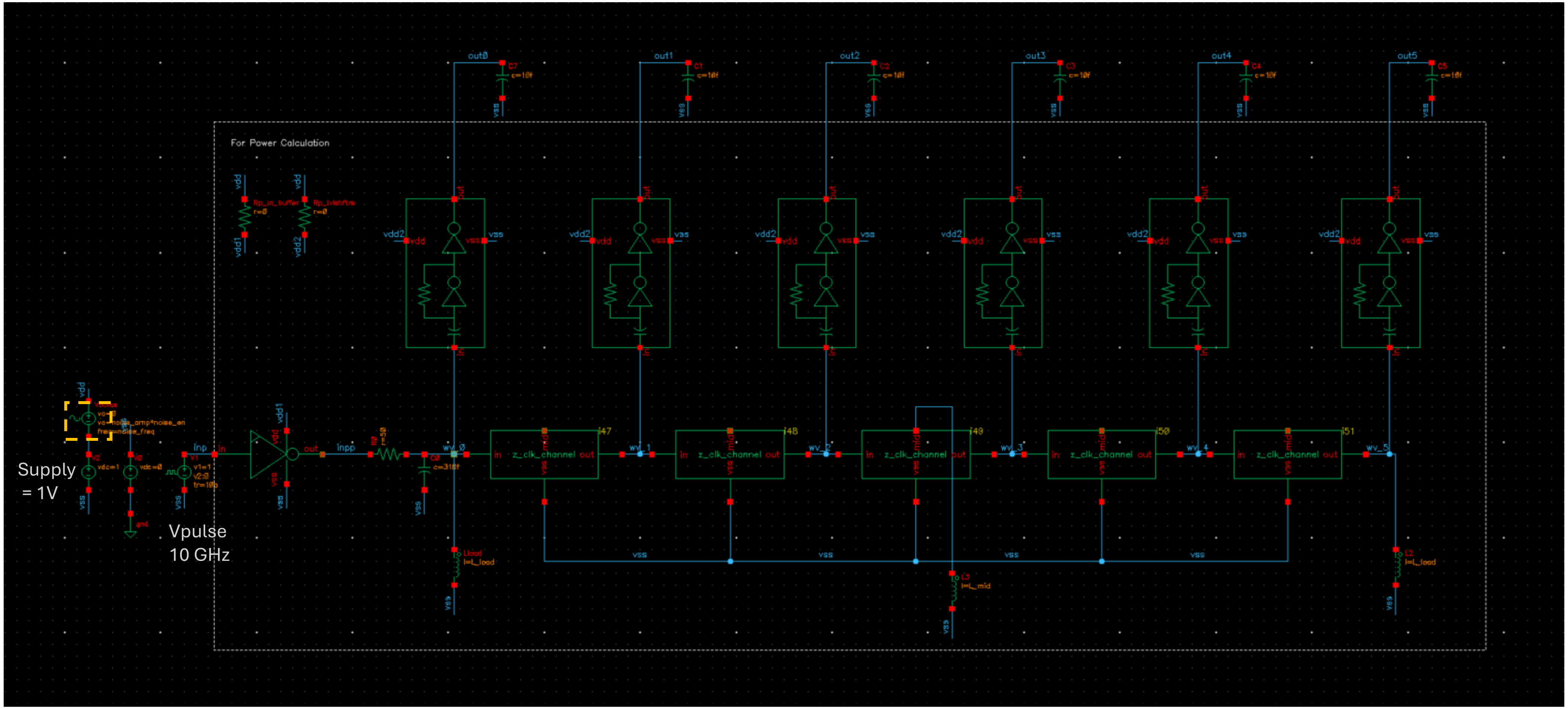
- Objective:

  - In TB3, the jitters are observed at the outputs for each lane.

TB3:

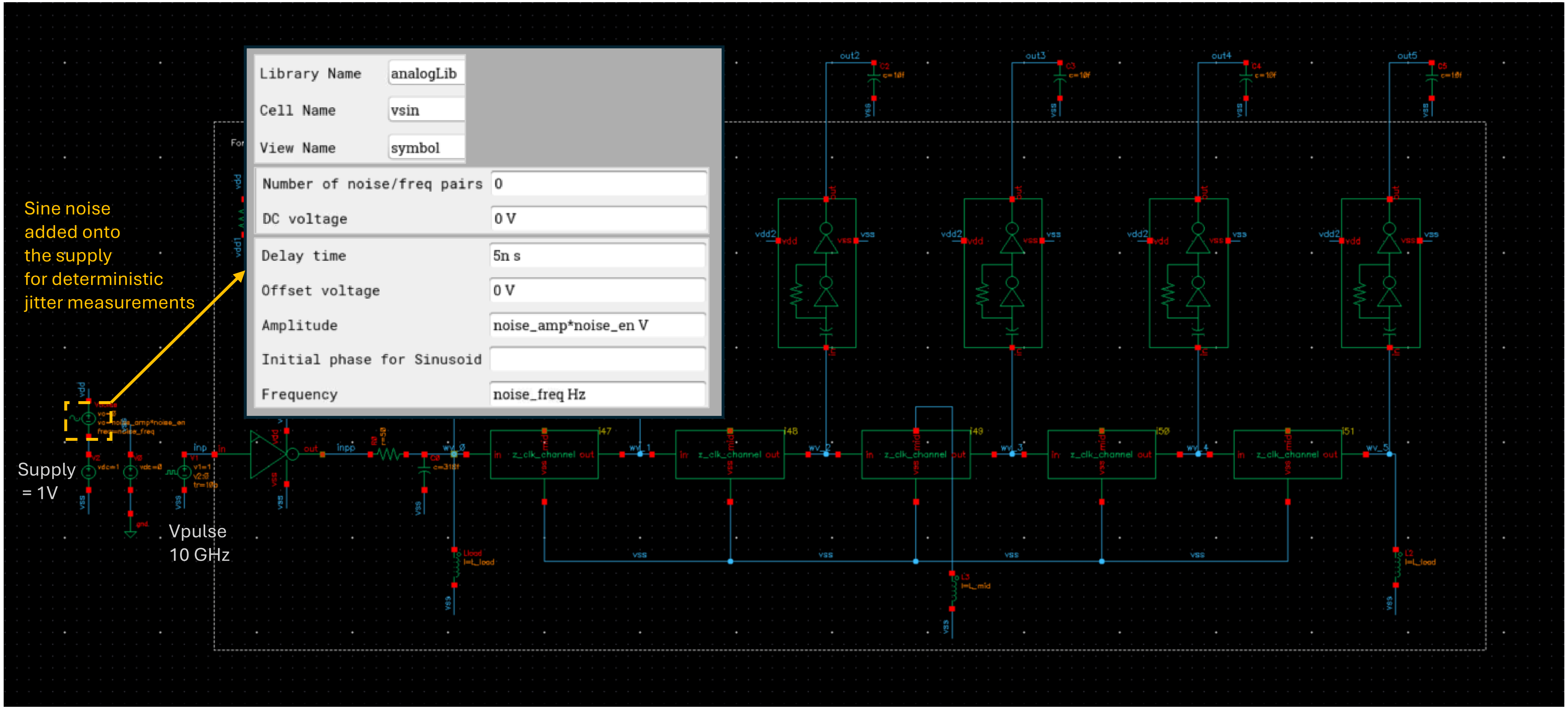
Jitter Simulations

- Schematics



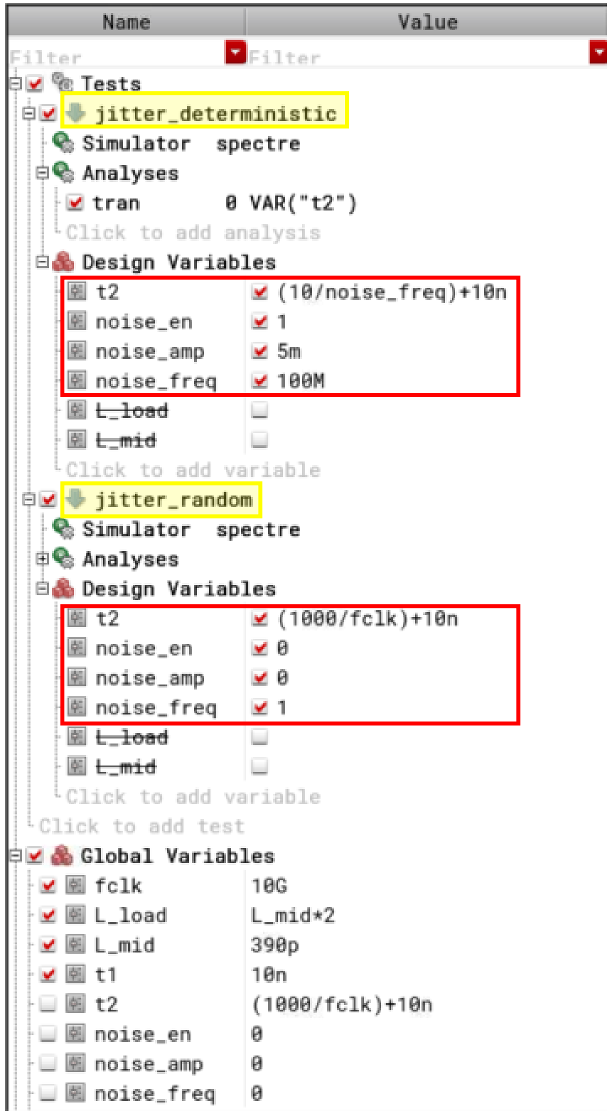
TB3:
Jitter Simulations

- Schematics



TB3:
Jitter Simulations

- Setup



TB3:
Jitter Simulations

- Measurements

Test	Name	Type	Details	EvalType
Filter	Filter	Filter	Filter	Filter
jitter_deterministic	*** DJs	expr		point
jitter_deterministic		expr	abs_jitter(clip(VT("/out0") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_deterministic		expr	abs_jitter(clip(VT("/out1") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_deterministic		expr	abs_jitter(clip(VT("/out2") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_deterministic		expr	abs_jitter(clip(VT("/out3") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_deterministic		expr	abs_jitter(clip(VT("/out4") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_deterministic		expr	abs_jitter(clip(VT("/out5") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_deterministic	dj_out0	expr	peakToPeak(abs_jitter(clip(VT("/out0") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_deterministic	dj_out1	expr	peakToPeak(abs_jitter(clip(VT("/out1") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_deterministic	dj_out2	expr	peakToPeak(abs_jitter(clip(VT("/out2") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_deterministic	dj_out3	expr	peakToPeak(abs_jitter(clip(VT("/out3") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_deterministic	dj_out4	expr	peakToPeak(abs_jitter(clip(VT("/out4") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_deterministic	dj_out5	expr	peakToPeak(abs_jitter(clip(VT("/out5") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_random	*** RJs	expr		point
jitter_random		expr	abs_jitter(clip(VT("/out0") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_random		expr	abs_jitter(clip(VT("/out1") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_random		expr	abs_jitter(clip(VT("/out2") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_random		expr	abs_jitter(clip(VT("/out3") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_random		expr	abs_jitter(clip(VT("/out4") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_random		expr	abs_jitter(clip(VT("/out5") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk")))	point
jitter_random	rj_out0	expr	stddev(abs_jitter(clip(VT("/out0") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_random	rj_out1	expr	stddev(abs_jitter(clip(VT("/out1") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_random	rj_out2	expr	stddev(abs_jitter(clip(VT("/out2") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_random	rj_out3	expr	stddev(abs_jitter(clip(VT("/out3") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_random	rj_out4	expr	stddev(abs_jitter(clip(VT("/out4") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point
jitter_random	rj_out5	expr	stddev(abs_jitter(clip(VT("/out5") VAR("t1") VAR("t2")) "rising" 0.5 ?xUnit "cycle" ?yUnit "s" ?Tnom (1 / VAR("fclk"))))	point

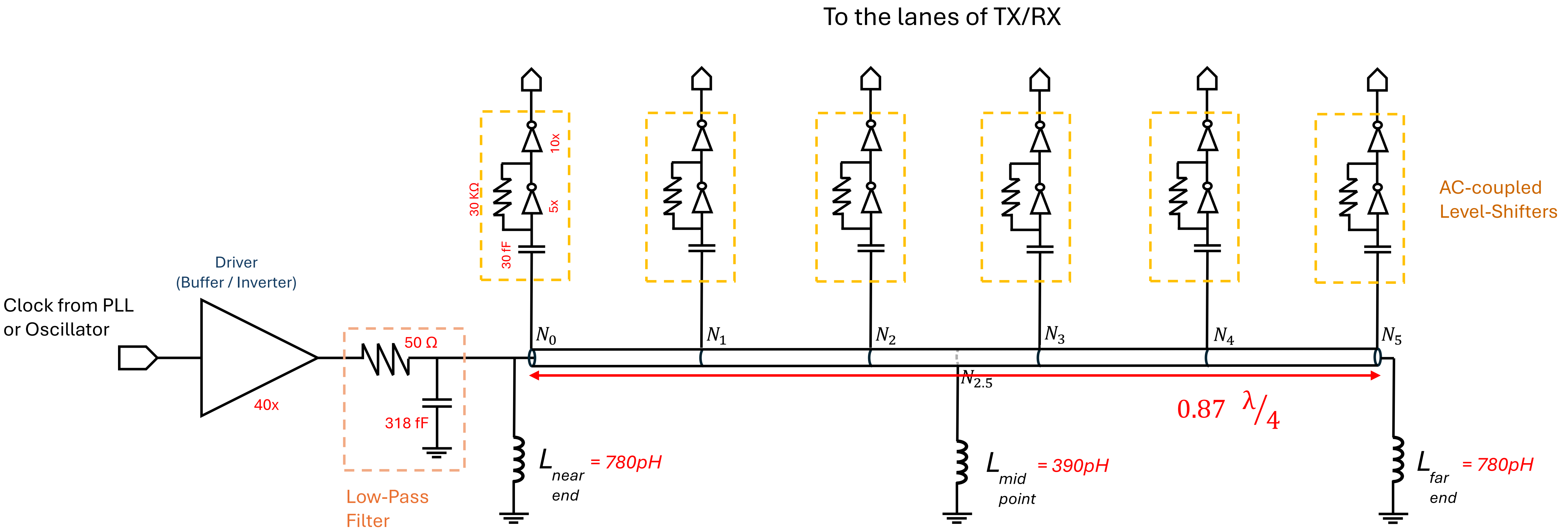
TB3:
Jitter Simulations

- Results

With 10mV pk2pk, 100MHz noise

		DJ (s)	RJ (s)
N0	out0	81.33f	9.44f
N1	out1	75.8f	5.944f
N2	out2	78.74f	2.564f
N3	out3	83.85f	5.268f
N4	out4	82.28f	5.452f
N5	out5	89.94f	4.462f

Final Design Values



Conclusion

- This project studies the idea of a standing wave-based clock distribution network. This report demonstrates the thought process & testbenches used to explore this concept for a 10 GHz clock input.