Standing Wave Based Clock Distribution Technique with Application to a 10×11 Gbps Transceiver in 28 nm CMOS

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***Abstract*—Clock distribution becomes a challenge as clock frequency and chip size keep increasing at the same time. Meanwhile, the distributed effects of the clock channel often show up where clock frequency is high and/or it drives large capacitive loading. In these cases, a standing wave-based structure becomes an attractive technique to deliver a low-jitter clock over a long distance with low power consumption. This paper will explore the properties of a standing wave resonator and its applications in clock distribution. The introduced technique was demonstrated with a design that delivers $5.5GHz$ quadrature clock to ten lanes of TX/RX and only consumes $12mW$. The ten lanes, each running at $11Gbps$, showed consistent and excellent jitter performance in measurement, verifying the proposed technique.**

I. Introduction

Clock distribution becomes a challenge as clock frequency and chip size keep growing simultaneously [1]. Running at the highest frequency and driving the heaviest load, clock distribution often accounts for a significant portion of a system's power budget. Besides, time-interleaved and parallel structures often share the same frequency synthesizer and require that clocks be distributed to all blocks with low jitter and low skew. Thus each buffer often needs to drive a channel as long as possible to reduce the number of buffer stages.

On the other hand, the distributed effect of circuit components comes into play as a result of increasing chip size and clock frequency. For instance, the phase velocity v_p of electromagnetic (EM) wave in a typical CMOS process, whose dielectric is assumed to have a relative permittivity of $\epsilon_r = 4$, is $1.5 \times 10^8 m/s$. Thus, the wavelength of a $30GHz$ signal is only $\lambda = 5mm$. Moreover, loading capacitors may increase the unit length capacitance of the clock channel, and reduce v_p and λ significantly. As a result, distributed effect may show up at GHz frequencies over a dimension of a few millimeters.

These factors make a standing wave based structure attractive [2]. The power consumption can be reduced significantly, because a resonator recycles energy that charges capacitors by converting it between electrical and magnetic fields periodically. In addition, a standing wave has the property that the resonant signal is in phase along the resonator. This means that even blocks that are far apart can be synchronized.

However, previously published methods based on *standing wave oscillator* [2] have the potential issue of multiple oscillation modes, which may lead to phase and frequency uncertainty. Besides, signal amplitude changes significantly along a standing wave resonator when it approaches quarter wavelength. In this paper, we will present a design that solves these problems. Amplitude variation is reduced significantly by loading clock channel with inductors at multiple points. And the standing wave resonator is driven by a buffer, instead of being configured as self-sustained oscillator. This avoids resonant mode uncertainty. We will first study the properties of a standing wave resonator, and then present a clock distribution circuit that delivers $5.5GHz$ quadrature clocks to ten lanes of TX/RX, each running at $11Gbps$. The clock channel spans $2.8mm$, and the heavy capacitive loading makes it close to a quarter wavelength. Our proposed resonator is able to deliver clock to the ten lanes with roughly the same phase and amplitude. Each clock phase drives a total capacitance of $1.75pF$, and the four-phase clock distribution only consumes $12mW$ power. The ten lanes show consistent and excellent jitter performance in measurement, which verified the design.

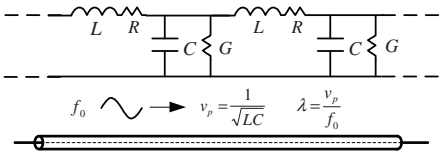

Fig. 1. Clock channel: lumped (top) and transmission line models (bottom).

II. Standing Wave Resonator

A clock channel can be modeled as transmission line, as in Fig. 1. L and C are unit-length inductance and capacitance; R and G are unit-length series resistance and shunt conduction that represent the loss of the line. The electromagnetic signal at frequency f_0 travels along the line at its phase velocity $v_p = \frac{1}{\sqrt{LC}}$, and has a wavelength of $\lambda = \frac{v_p}{f_0}$ [3]. It is worth noting that C includes not only that of metal traces but also loading capacitors. As a result, phase velocity v_p can be much smaller than the speed of light, and the wavelength λ is also reduced significantly. This makes transmission-line effect manifest at GHz frequency over mm distance.

A. Standing Wave Resonator without Loss

EM waves might circulate in the transmission line if certain boundary conditions are satisfied, and thus make a resonator. For instance, Fig. 2 shows an open-ended $\frac{1}{2}\lambda$ resonator. Consider an incident wave of $V^+ = V_0$ injected at $x = 0$. It accumulates a phase shift of 2π after a round trip with two full reflections at the two ends. Thus, it coincides with the incident wave and resonates. The voltage along the line is given by the sum of waves in both directions [3]. It is clear that the whole line resonates in phase but the amplitude varies

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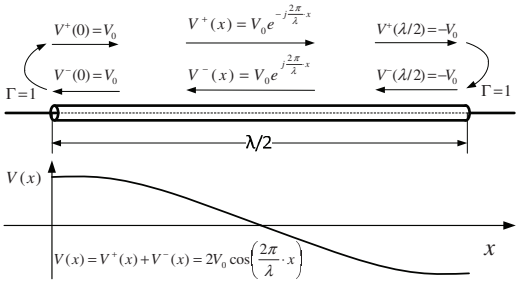

Fig. 2. Illustration of $\frac{1}{2}\lambda$ resonator, with two open ends.

along the line. The general case of a standing wave resonator can be analyzed in the same way.

However, the clock to be delivered is seldom at such frequencies that the clock channel is an integer multiple of half-wavelength. In this case, we need to terminate the line properly so that the reflections at the two ends make up the total phase shift needed. Fig. 3 shows an example where the channel is slightly shorter than half-wavelength. Looking to the left from $x = T_1$, the wave would have seen a line of length T_1 in a $\frac{1}{2}\lambda$ line resonator. The missing part is approximately equivalent to a capacitor of $C{\cdot}T_1$. Thus, by terminating the line with $C{\cdot}T_1$ and $C{\cdot}T_2$, we can truncate the standing wave at the two ends and keep the middle portion untouched. Similarly, Fig. 4 illustrates a case in which the line is slightly longer than half-wavelength. In this case, the reactance of the extra line, which is about $C \cdot T_1$ and $C \cdot T_2$, needs to be resonated away so that the middle $\frac{1}{2}\lambda$ portion sees an open circuit at its two ends. Thus, the line needs to be terminated by proper inductors L_1 and L_2.

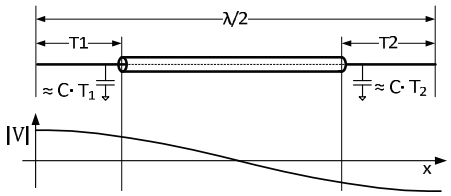

Fig. 3. Illustration of standing wave resonator with capacitive termination.

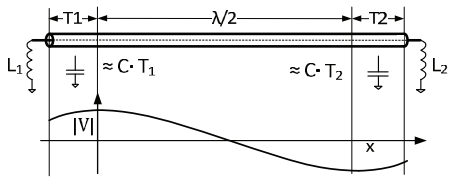

Fig. 4. Illustration of standing wave resonator with inductive termination.

As a general rule, the termination should be inductive if it first sees an anti-node (i.e., a point with maximum voltage swing) along the line, and capacitive if it first sees a node (i.e., a point with zero voltage swing). By tuning the termination capacitors and/or inductors at the two ends, one can truncate the standing wave and get the desired resonant pattern.

B. Standing Wave Resonator with Loss

Resonance signal decays due to energy loss in a real resonator, and it can only sustain when loss is compensated by a driver. Consider a resonator that is terminated properly at x_1 and x_2, and a current source I_s that drives the resonator at x_s. Without loss of generality, assume the series resistor in Fig. 1 dominates loss and it is small enough that the standing wave pattern is not altered. The total loss is $P_{loss} = \frac{1}{2}\int_{x_1}^{x_2} |I(x)|^2 R dx$. On the other hand, current source I_s at x_s injects power of $P_{inj} = \frac{1}{2}\Re\{I_s V^*(x_s)\}$, where $V^*(x_s)$ is the complex conjugate of resonant voltage at x_s. In steady state, loss is equal to compensation, i.e. $P_{loss} = P_{inj}$. Noting that I_s and $V(x_s)$ are in phase at resonant frequencies, it is straightforward to solve the resonate voltage as follows:

$$V(x) = |I_s| \cdot \frac{L}{CR} \cdot \frac{2|\cos\left(\frac{2\pi}{\lambda}x_s\right)| \cdot \cos\left(\frac{2\pi}{\lambda}x\right)}{(x_2 - x_1) - \frac{\lambda}{4\pi}\left(\sin\frac{4\pi x_2}{\lambda} - \sin\frac{4\pi x_1}{\lambda}\right)}. \quad (1)$$

This equation provides the design guidelines. The first term shows the linear relation between the driver's current and the voltage swing it can stimulate. The second term shows that $\frac{L}{RC}$ should be maximized in order to stimulate the largest voltage swing. Intuitively, small C and large L requires less charge to be disposed along the line and thus provides smaller loss due to resonant current; and small series resistance R also means less power loss. By making metal wider, one gets larger C, and smaller L and R. But these parameters change nonlinearly with metal width, especially if load capacitors contribute a significant portion of C. The optimization would require a few iterations based on electromagnetic simulation.

The third term of (1) shows the effect the line's lateral configuration. First of all, the current should be injected to a point with the largest $\cos\left(\frac{2\pi}{\lambda}x_s\right)$, i.e., the point with the largest voltage swing. This is because current delivers the most energy when it is injected against the largest voltage. On the other hand, considering the nonuniform voltage amplitude, it is desirable to also put the load at a point with the largest swing. Since the locations of driver and load are constrained by the top-level floor plan, these two conditions might not be satisfied at the same time and designers need to make a balance. This will be illustrated by an example in Section III.

III. Example Design and Measurement

In the following example, we will apply the techniques developed in the previous section to a design that delivers $5.5GHz$ clock to ten lanes of TX/RX. Each lane is the same as that in [4], and the ten lanes share the same PLL and clock buffer shown in Fig. 5. Every two lanes share a vertical clock channel to reduce total routing capacitance. The clock channel and its loading can be represented by a five-segment lumped model, as shown in the middle of Fig. 5. $C = 350fF$ includes $160fF$ from the loading of two TX/RX lanes and $190fF$ from horizontal and vertical interconnects. $L = 180pH$ and $R = 4.5\Omega$ are the series inductance and resistance per segment based on EM simulation. The width and spacing of metal traces are optimized such that $\frac{L}{RC}$ is maximized, as

discussed in Section II. It is easy to calculate that each segment has a phase shift of $2\pi f_0\sqrt{LC} = 0.0437 \times 2\pi$ for signal at $f_0 = 5.5GHz$, and five segments have a total phase shift of $0.87 \times \frac{\pi}{2}$. Thus, the clock channel can be simplified as a transmission line that has an electrical length of $0.87 \times \frac{\lambda}{4}$, as shown on the bottom of Fig. 5, where λ is the wavelength.

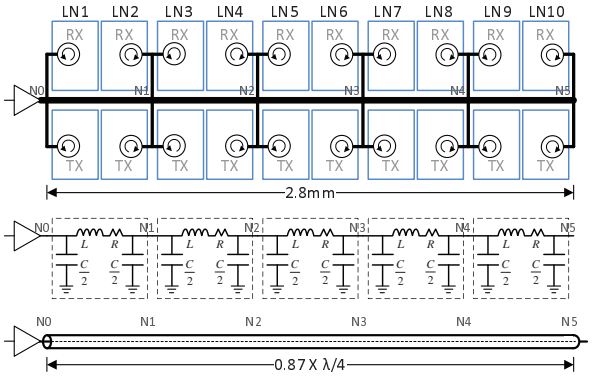

Fig. 5. Clock distribution for 10 lanes of TX/RX: floor plan (top), lumped model (middle) and transmission line model (bottom) of clock channel.

Next we need to design a resonator and tune it to $5.5GHz$. A conventional way is to put an inductor just next to the buffer to resonate with the capacitance of the clock channel, and leave the far end open, as shown in Fig. 6. However, a closer examination reveals two problems with this method in our scenario. First, there is significant voltage variation along the channel that is close to quarter-wavelength. In theory, the resonant voltage at $N0$ is only $\cos(0.87 \times \frac{\pi}{2}) = 0.2$ times that at the far end node $N5$. This large variation is not acceptable here. Besides, the clock buffer inject current to node $N0$ which has the smallest voltage swing along the line. Based on Section II, this is the least efficient point to inject current.

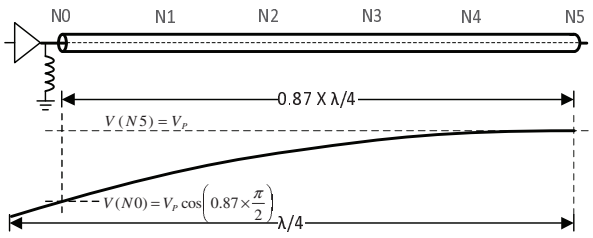

Fig. 6. Conventional near-end-tuned scheme. The driver sees smallest voltage swing, and voltage swing varies by 80% along the clock channel.

Another possibility is to terminate the far end with the proper inductor, as shown in Fig. 7. In this way, the near end sees the largest voltage swing. Thus, the same current can stimulate much larger resonant voltage in this circuit than the one in Fig. 6. However, it still has the problem of a large voltage variation along the clock channel.

In order to reduce voltage variation, we must cut the nearly-quarter-wavelength line into smaller segments, and only use the portion with large amplitude in the standing wave pattern. One possibility is shown in Fig. 8. The line is divided into two

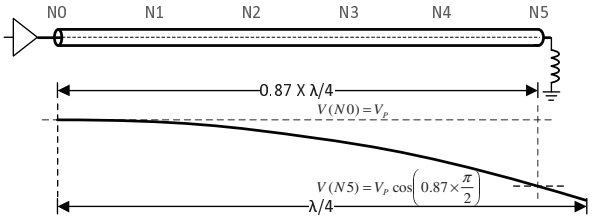

Fig. 7. Conventional far-end-tuned scheme. The driver sees peak voltage swing, but voltage swing has 80% variation along the line.

segments, each with a length of $0.44 \times \frac{\lambda}{4}$. We make a resonator of the left portion by leaving $N0$ open and terminating $N_{2.5}$ with the proper inductor. The standing wave pattern peaks at $N0$ and drops to $\cos(0.44 \times \frac{\pi}{2}) = 0.77$ times the peak voltage at $N_{2.5}$. We can do the same thing with the right portion, and the two inductors at $N_{2.5}$ can be implemented as a single one. Thus we stitch together two pieces of standing wave patterns to cover the whole clock channel. The voltage variation along the channel is reduced to 23% from 80% previously.

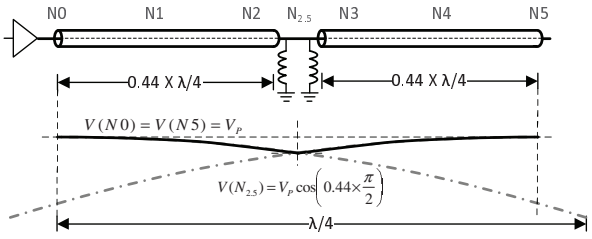

Fig. 8. Illustration of mid-tuned scheme. The driver sees peak voltage swing, and voltage variation is reduced to 23%.

Further reduction of voltage variation involves cutting the line into even smaller pieces. Fig. 9 shows the one we implemented. The line is cut into four pieces, each with a length of $0.22 \times \frac{\lambda}{4}$. Each piece has one end open and the other terminated with L so as to resonate at $5.5GHz$. The two Ls at $N_{2.5}$ can be implemented as one $L/2$. The resulting standing wave pattern at most drops to $\cos(0.22 \times \frac{\pi}{2}) = 0.94$ times its peak value, which is only 6% variation.

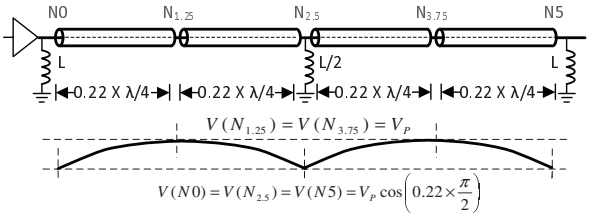

Fig. 9. Proposed three-point-tuned scheme. Voltage variation is significantly reduced to 6% along the clock channel.

The above analysis was verified by simulation. The four resonators in Fig. 6-Fig. 9 were tuned to $5.5GHz$ with proper inductors and driven by $3mA$ current source at $5.5GHz$. Fig. 10 shows the voltage swing at the five tap points. As expected, the near-end-tuned scheme in Fig. 6 shows very low

voltage swing due to inefficient current injection. The far-end-tuned scheme in Fig. 7 has larger amplitude, but large variation along the channel. The mid-point-tuned scheme in Fig. 8 has much-reduced voltage variation. The three-point-tuned scheme in Fig. 9 has the largest amplitude and the smallest voltage variation. The amplitude drop toward the far end is mostly determined by the loss of the clock channel.

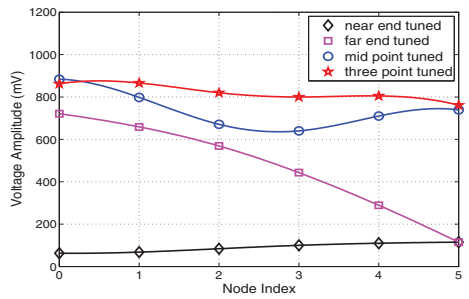

Fig. 10. Simulation results of the four resonators in Fig. 7-9.

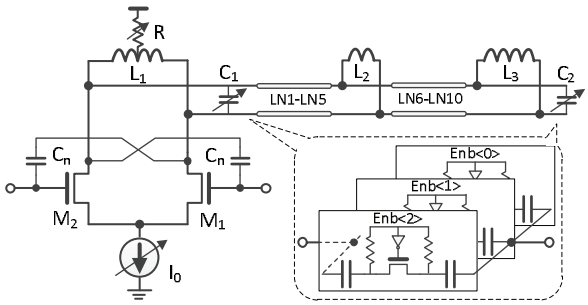

Fig. 11. Schematic of the proposed clock distribution network. Two identical circuits are implemented to distribute I/IB and Q/QB clocks, respectively.

Fig. 12. Die photo of clock channel driving ten lanes of TX/RX.

The scheme in Fig. 9 was implemented in a 28nm CMOS process to distribute $5.5GHz$ quadrature clocks to ten lanes of TX/RX. The schematic and die photo are shown in Fig. 11 and Fig. 12, respectively. The driver is a differential pair, with Cgd of transistors being canceled by C_n. This significantly improves the reverse isolation from the clock distribution network to the clock source. Resistor R is used to adjust the common mode voltage at the output. Inductor L_1 plays a dual role of DC current path and near-end termination. Two other inductors L_2 and L_3 are put in the middle and at the end of the clock channel, which can also be seen from the die photo in Fig. 12. The three inductors were designed such that $L_1 = L_3 = 2L_2$. Two tunable capacitors C_1 and C_2 were put at the two ends of the clock channel to fine tune the

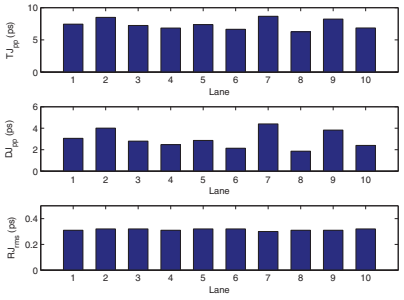

Fig. 13. Measured jitter at TX outputs at $11Gbps$. The ten lanes show consistent jitter performance, including random jitter (RJ_{rms}), deterministic jitter (DJ_{pp}) and total jitter (TJ_{pp}).

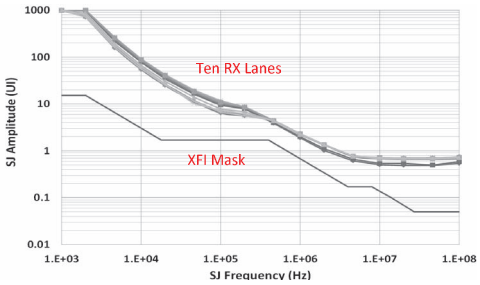

Fig. 14. Measured jitter tolerance at 11Gbps. Ten RX's show consistent result.

center frequency from $4.25GHz$ to $5.75GHz$. Each capacitor consists of three binary weighted switched capacitors. Each clock phase drives a total loading of $1.75pF$, and the whole quadrature clock distribution circuit only consumes $12mW$.

In each $11Gbps$ TX/RX lane, the $5.5GHz$ quadrature clock drives multiple phase interpolators that generate local clocks [4]. Clock jitter was measured through the ten TX outputs, and summarized in Fig. 13. Jitter tolerance of the ten RX's was also measured and showed in Fig. 14. In both measurements, the ten lanes showed excellent and consistent results. This verifies the proposed design delivers low-jitter low-skew clock to all ten lanes with roughly the same amplitude.

IV. Conclusion

In this paper, we presented the theory and design of a standing wave-based clock distribution network. The presented technique was verified with a design that drives $5.5GHz$ quadrature clock to ten lanes of TX/RX with only $12mW$ and achieves excellent jitter and skew performance.

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