Global Clock Distribution on Standing Wave with CMOS Active Inductor Loading

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***Abstract*—In this paper, an X-tree clock distribution topology based on standing wave oscillator is introduced. To increase output amplitude at the loading point and saving chip area, a novel CMOS active inductor is designed and applied to each loading points of the network. The cascoded differential active inductor is 1 nH with $Q = 344$ at 10 GHz. This makes the two stage, 6.2 mm x 6.2 mm dimensional standing wave based clock distribution network perfectly convey clock signals everywhere on the chip without taking much of the chip area while keeping a relatively high output voltage swing. The clock jitter introduced by active inductor loading is 0.139 ps and almost zero clock skew.**

I. Introduction

Global clock distribution design is becoming an increasingly challenge task for multi GHz microprocessors. Clock skew and jitter requirement are becoming more and more stringent as clock frequency increases. For traditional clock distributions, skew and jitter are proportional to latency, which is dominated by a series of resistive-capacitance delay and does not scale with clock period. Moreover, the resistive-capacitance wire-load consumes a significant amount of power.

As an alternative, resonant clock is applied to reduce dynamic power and achieve better control of clock skew and jitter. There are three approaches to create resonant clocks, standing wave [1], traveling wave [2], and L-C tank resonant [3]. Among these approaches, standing wave clock scheme has uniform phase across the entire clock network, which yields almost zero skew in global clock distribution. But its voltage and current vary spatially. Furthermore, the voltage swing at the loading point (the end of a transmission line) usually reduces to zero.

To overcome the position-dependent amplitude variation and low output swing issue, passive inductive loading is proposed [4], where uniform phase and almost uniform amplitude standing wave is realized. In this paper, we extend the idea of inductive loading further by applying CMOS active inductor as inductive loading. Compared to passive inductor design, active inductor can potentially achieve tunable design with reduced area overhead and high Q value. A novel differential cascoded active inductor circuit is proposed with high Q value. The design is employed in an improved X-tree clock distribution network to distribute low skew, low jitter clock across the chip. The rest of the paper is divided as the following: section II first introduces the background of standing wave resonance and passive inductor loading. Then an inductive loading X-tree clock distribution network is elaborated. Section III summarizes the Gyrator-C active inductor design and introduces a novel CMOS active inductor structure that is used in this design. Section IV shows the simulation results of the overall X-tree clock distribution network. Section V is the conclusion.

II. Global Clock Distribution with Active Inductor Loading

A. Standing Wave Oscillation on Tansmission Line

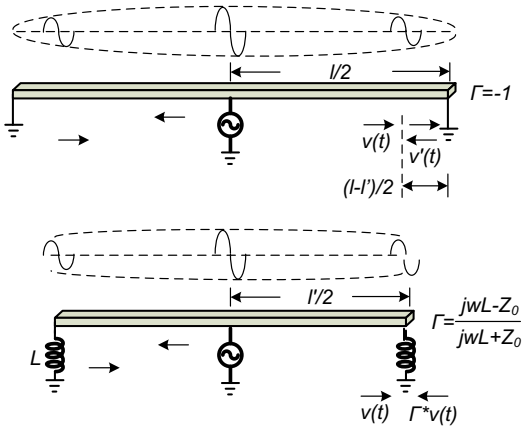

Fig. 1. Standing wave oscillator on short-ended and inductive loading transmission line

Standing wave occurs when two waves of the same frequency and amplitude propagates in opposite directions. Take the transmission line as an example, there are three cases of line terminations that can lead to standing wave, when the length of the transmission line equals to integer number of quarter wave length

- short circuit, with $Z_L = 0,\ \Gamma(0) = -1$
- open circuit, with $Z_L = \infty,\ \Gamma(0) = 1$
- reactance loaded, with $Z_L = jX_L,\ |\Gamma(0)| = 1$

Where Z_L is loading impedance and Γ is reflection coefficient. Figure 1 shows an example of standing wave oscillator with short-ended and inductive loading transmission line.

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B. Inductive loading on Transmission Line

In conventional standing-wave clock distribution scheme, the output amplitude varies with its position in the transmission line and becomes zero at the end of the line. To overcome this issue, inductive loading is proposed [4]. The idea is to use inductor as termination to maintain the reflection with the same phase/amplitude at the position accordingly, while effectively shorten the transmission line. Assume l is the length of short-ended transmission line length, l' is the length of inductive loaded transmission line.

At the inductor loading point, the reflection coefficient Γ can be expressed as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{j\omega L - Z_0}{j\omega L + Z_0} \tag{1}$$

$$\angle\Gamma = \pi - 2tan^{-1}\frac{\omega L}{Z_0} \tag{2}$$

Equation 2 denotes incident wave and reflected wave differs $\angle\Gamma$ in phase at the inductor loading point, but with same amplitude. Given the same incident wave, the phase of the reflected wave should be equal in both cases as in Figure 1

$$\pi - 2\beta(\frac{l - l'}{2}) = \angle\Gamma \tag{3}$$

Where β is phase velocity, which can be expressed as $2\pi/\lambda$ (λ is electrical wave length). From equation 3, assume $l = n\lambda/4$, n=1,2,3,4..., length l' can be expressed in term of length l as:

$$l' = \frac{n\lambda}{4} - \frac{\lambda}{\pi}tan^{-1}\frac{\omega L}{Z_0} \tag{4}$$

It can be seen that the standing wave amplitude at the inductor load point is the same as the l' position in short-ended transmission line. Therefore, by controlling the length and inductance, a larger voltage swing is obtained at the expense of a shorter transmission line.

C. Global Clock Network with Active Inductor Loading

As a natural extension, the passive inductor loading can be replaced by CMOS active inductor. Compared to passive inductors, which usually implements as spiral inductor, CMOS active inductor is area saving, inductance tunable and can achieve relatively high quality factor. Moreover, it is compatible with CMOS technology process and easily integrated into chip-sets. In the following, we use an X-tree clock distribution topology, along with active inductor loading, where the clock signal is passed through transmission lines in the form of standing wave, as shown in Figure 2. A 10GHz clock distribution is used as a design example. Active inductor load of 1nH is chosen as a tradeoff between output voltage swing and achievable clock network dimension.

III. CMOS Active Inductor

A. Active Inductor Topology

CMOS active inductors are typically implemented by using operational transconductance amplifier (OTA) with gyrator-C

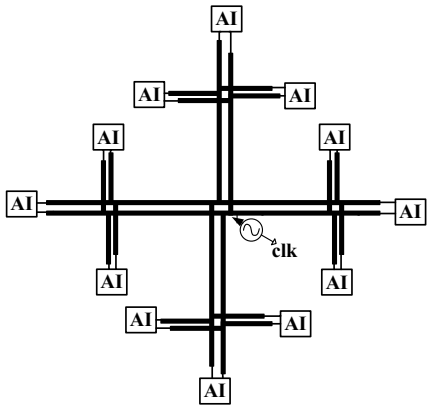

Fig. 2. Full Global Clock Distribution Networking with Active Inductor Loading Circuit Schematic

structure [5]. As shown in Figure 3, a gyrator-C structure is composed of two back-to-back connected OTAs.

g_{m1} and g_{m2} are transconductance of OTA- and OTA+ respectively. The back-to-back connected OTA+ and OTA- provides 180° phase shift while the parasitic capacitor offers a -90° phase shift, both together gain a 90° phase shift between voltage and current. As a result, an active inductor is formed with the inductance of

$$L_{eq} = \frac{C}{g_{m1}g_{m2}} \tag{5}$$

Ideal OTA with infinite input and output impedance can achieve perfect Q value. In reality, circuit implementation with single transistor amplifier suffers from low input or output impedance and affects quality factor value. To improve Q, various techniques has been proposed, e.g. cascode [5], feedback resistor [6], etc. The requirement of opposite

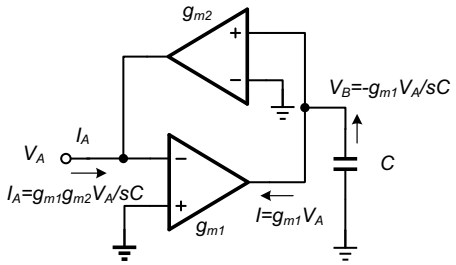

Fig. 3. Ideal Model of Single Ended Gyrator-C Active Inductor

output current directions limits circuit topology design. On the contrary, differential structure have inputs(outputs) of opposite phases, this feature enables the flexibility of OTA choices for active inductor, e.g. an active inductor can be composed by two OTA- or two OTA+. Therefore, common source amplifier with high input/output impedance can be applied to achieve better performance. Moreover, compared with its single counterparts, differential active inductor has two attractive advantages: rejection of common-mode disturbances due to differential configuration and double of voltage swing.

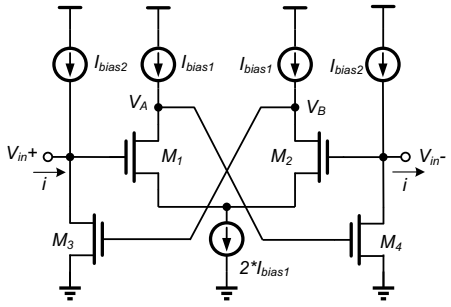

Fig. 4. Circuit Schematic of Differential Active Inductor

B. Differential Active Inductor Design

As addressed previously, in contrast to conventional differential active inductor, which is made up of two differential OTAs or two single ended active inductors, the proposed design explores the availability of inout signals with both phase and eliminates the limitation on OTA choices. Simple circuit with relatively high input/output impedance is employed in the design, as shown in Figure (4).

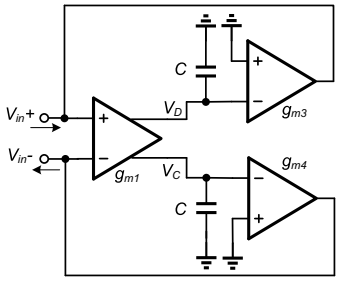

Fig. 5. Circuit Topology of Differential Active Inductor

Its equivalent circuit topology is shown in figure (5). It is made up of a differential pair and two single OTA-. Half equivalent circuit and corresponding small signal model are listed in Figure (6) and Figure (7).The input admittance of the active inductor and its RLGC model is given by:

$$Y = \frac{sC_{gs2}}{2} + \frac{g_{ds4}}{2} + \frac{g_{m1}g_{m4}}{2sC_{gs4} + g_{ds1}} \quad (6)$$

$$L = \frac{2C_{gs4}}{g_{m1}\ g_{m4}} \quad (7)$$

$$R_s = \frac{2g_{ds1}}{g_{m1}\ g_{m4}} \quad (8)$$

$$C_p = \frac{C_{gs2}}{2} \quad (9)$$

$$R_p = \frac{2}{g_{ds4}} \quad (10)$$

$$Q \approx \frac{\omega L}{R_s} = \frac{\omega C_{gs4}}{g_{ds1}} \quad (11)$$

From Equation 6, R_s is determined by g_{ds1}, g_{m1} and g_{m4}. Roughly, $g_{m1} \approx 10g_{ds1}$, $R_s \approx 2/10g_{m4}$, thus R_s can not be designed too small to enlarge Q. For a 1nH inductor

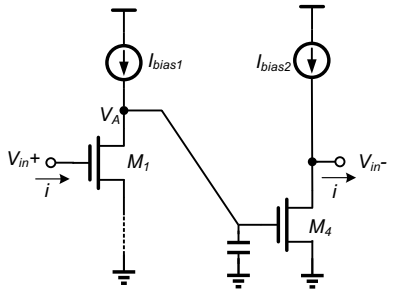

Fig. 6. Half equivalent circuit of Differential Active Inductor

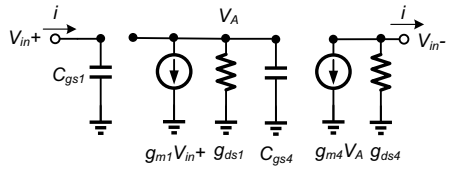

Fig. 7. Half small signal model of Differential Active Inductor

we would like to apply in global clock distribution network, Q is determined mostly by the relatively high R_s. Thus $Q \approx \omega L/R_s$. To further improve Q, R_s needs to be reduced, i.e. to increase C_{gs4} or decrease g_{ds1}. One way to improve g_{ds1} performance is to use cascode differential pair to reduce conductance.

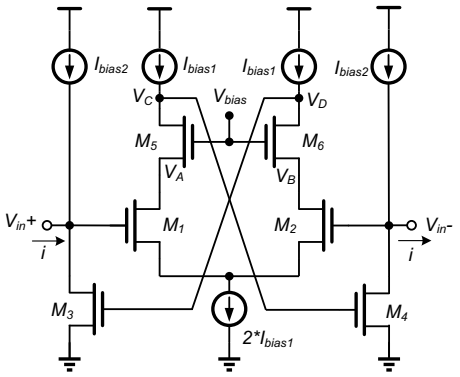

Fig. 8. Circuit Schematic Model of Cascoded Differential Active Inductor

Figure 8 shows this implementation. M_1, M_2, M_3 and M_4 formed two active inductors. By cascoding M_5 and M_6 on M_1 and M_2 separately, output conductance is lowered to $g_{ds1}g_{ds5}/g_{m5}$ compared with g_{ds1} without cascoding.

The equivalent half circuit model is shown in Figure 9 and small signal analysis in Figure 10. In this case, Q is improved to

$$Q \approx \frac{\omega C_{gs4}g_{m5}}{g_{ds1}g_{ds5}} \quad (12)$$

For a 1nH active inductor, we use $(W/L)_{1-4} = 2.4\mu m/60nm$ $(W/L)_{5,6} = 1.44\mu m/60nm$. Figure (11) shows simulation results of the circuit topology, from which,

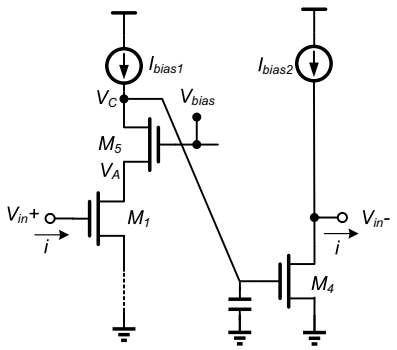

Fig. 9. Equivalent Half Circuit Model of Cascoded Differential Active Inductor

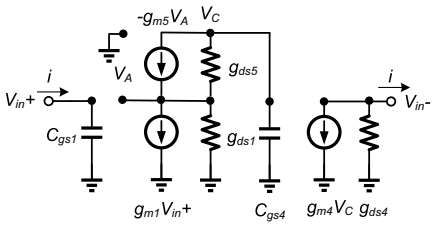

Fig. 10. Small signal Model of Cascoded Differential Active Inductor

the inductance is about 1 nH at 10 GHz with Q around 344. Power consumption of each active inductor is 9.3mW.

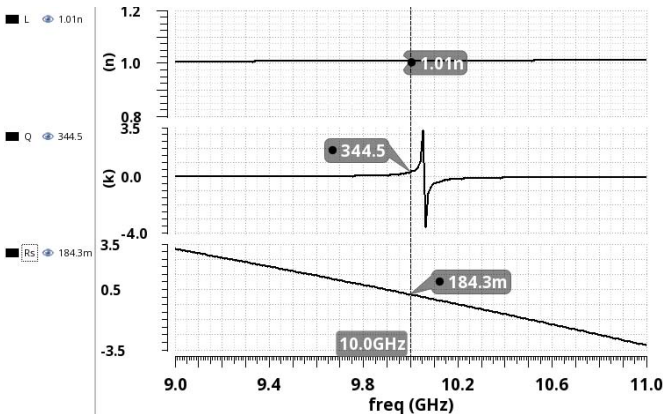

Fig. 11. Simulation results of Cascoded Differential Active Inductor

IV. Simulation results of A 10-GHz Clock Design

As shown in section II-B, active loading reduces the overall transmission line length. As part of the global clock network, the length of l' affects the span of the clock network and a larger value of l' is more desired. Assuming a 1nH inductor is used in a 10GHz clock distribution network, with the transmission line generating standing wave at half λ, from equation 4, $l' \approx 0.84l = 0.42\lambda = 6.15mm$, which is good enough to cover the entire chip for die size less than $6mm * 6mm$.

By applying differential active inductor with the proposed cascoded differential active inductor into clock distribution network, Figure 12 shows eye diagram and its cross section. Clock jitter introduced by active inductor is 0.139ps.

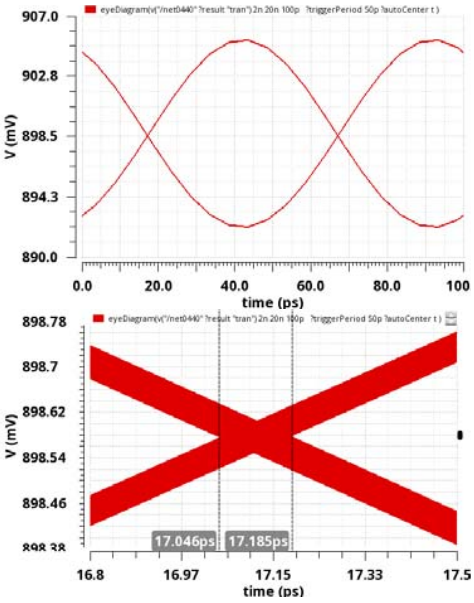

Fig. 12. Eye Diagram with its crossing zoomed in

V. Conclusion

This paper proposed an CMOS active inductive loading X-tree global clock distribution network using standing wave resonance. The proposed scheme benefits from the uniform phase property of standing waves. Additionally, active inductor loading improves the output voltage swing, reduce the area overhead and provides tunability. The proposed clock distribution network scheme can effectively relax the buffer balance requirement of the local clock distribution due to its low clock skew and jitter. A 10GHz clock network is designed and simulated to prove its viability.

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