High-Speed Serial Interface Circuits and Systems

Design Exercise 8 –

Continuous-Time Linear Equalizer (CTLE)

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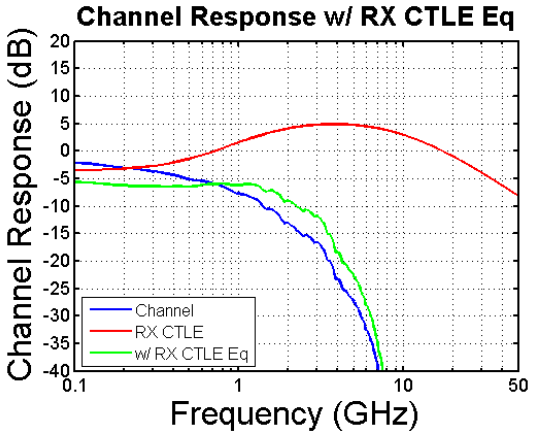
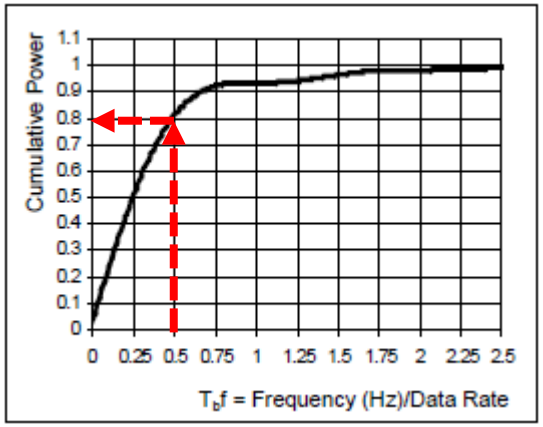


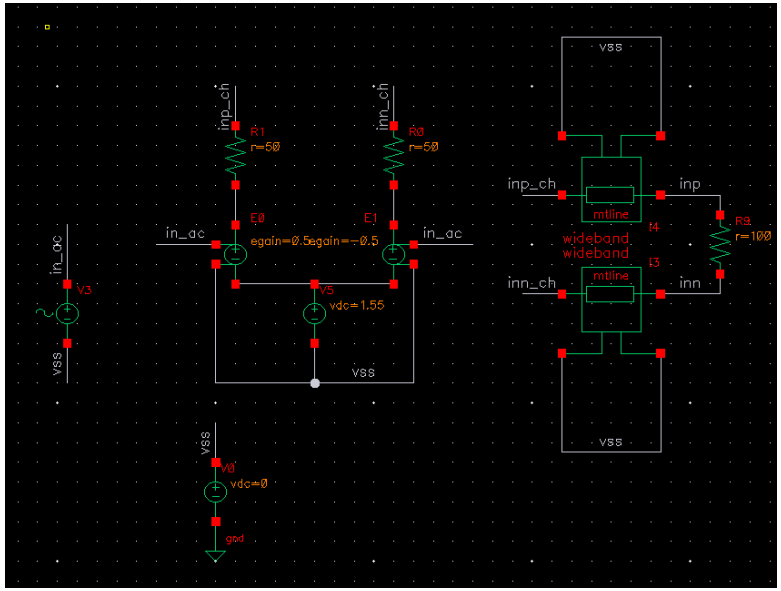
<Frequency response flattening>

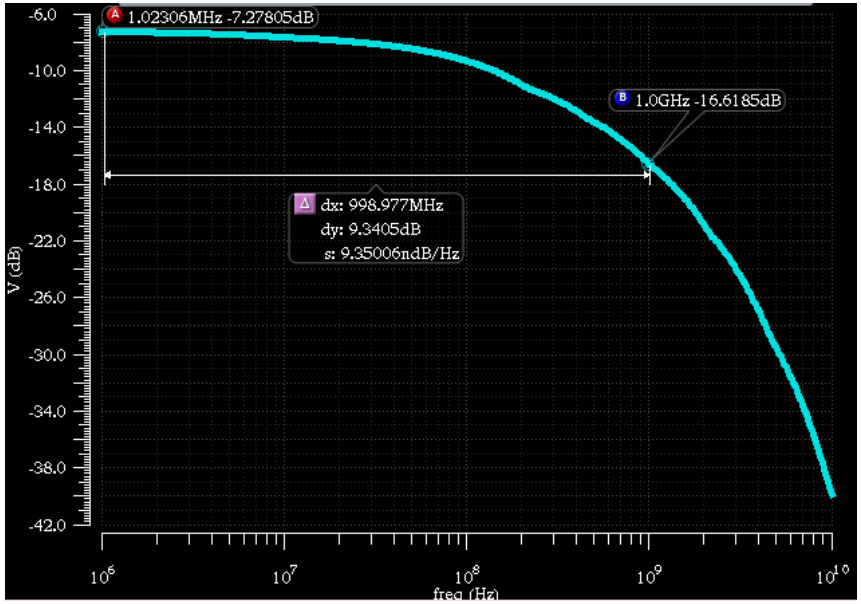


<Integrated power spectrum of NRZ data>

- Until what frequency..??
  - Nyquist frequency:
    In order to recover data,
    it is necessary to have bandwidth *at least half of data rate*
    ex) 2Gbps ➔ 1GHz 3-dB bandwidth required

Channel Characteristic



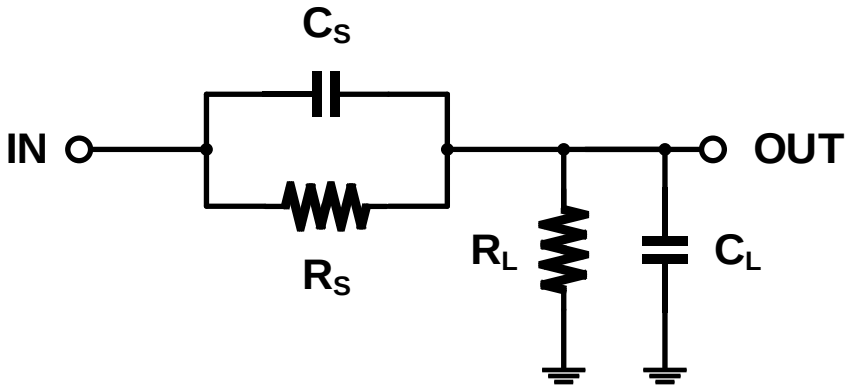


- mtline (microstrip)
  -Dielectric const.: 4.8
  -Dielectric layer thickness: 360u (m)
  -Signal line width: 625u (m)
  -Signal line thickness: 17.78u (m)
  -Physical length: 8 (m)

- Channel characteristics
  - DC loss = - 7.2 dB (Termination loss + @)
  - High freq. loss relative to DC @ 1 GHz = - 9.3 dB

- At least 6.3dB of boost at 1 GHz required to satisfy the Nyquist frequency

Passive CTLE



$$H(s) = \frac{R_L}{R_S + R_L} \frac{sR_SC_S + 1}{s\left(R_S \parallel R_L\right)\left(C_S + C_L\right) + 1}$$

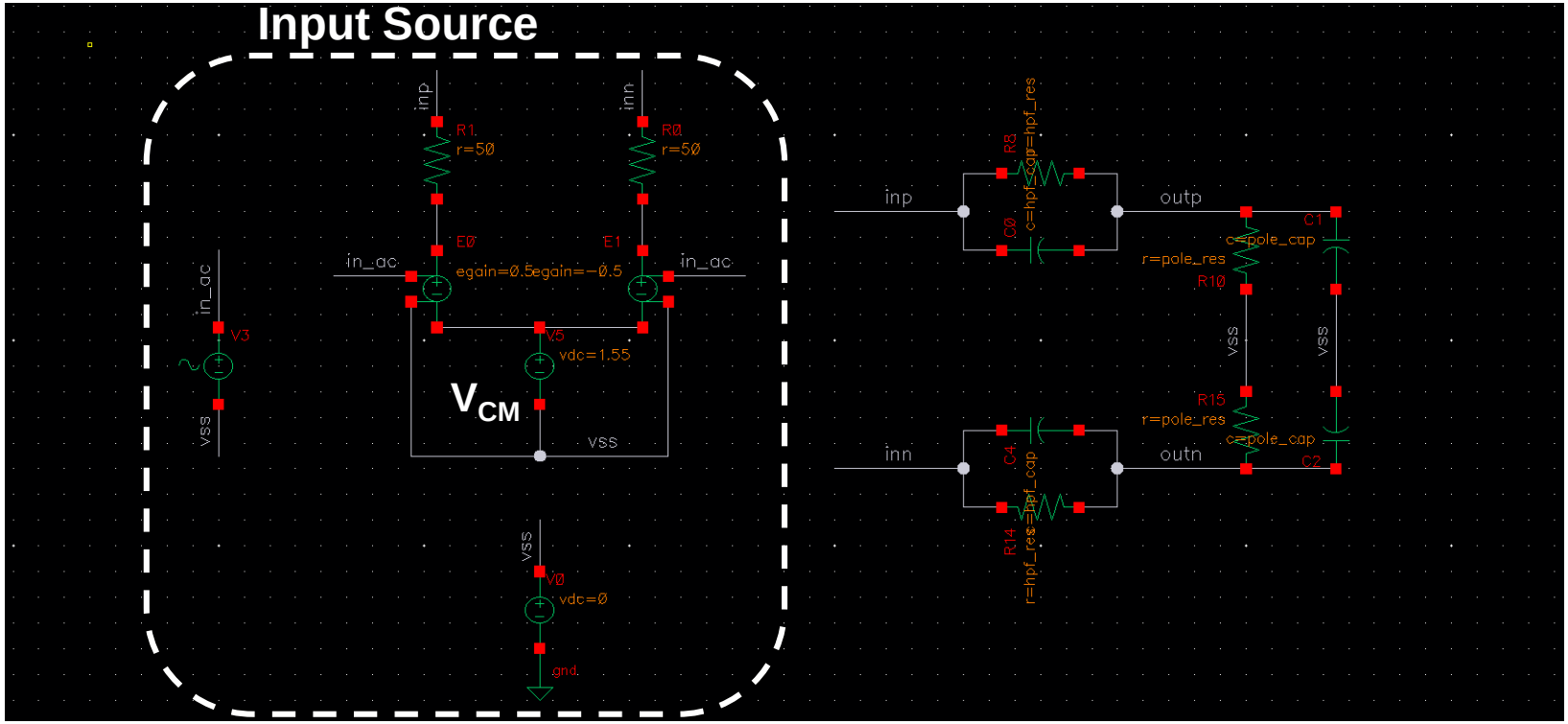
$$\text{Zero} = \frac{1}{R_SC_S}$$

$$\text{Pole} = \frac{1}{\left(R_S \parallel R_L\right)\left(C_S + C_L\right)}$$

$$\text{Peaking gain} = \left(1 + \frac{R_S}{R_L}\right)\left(\frac{C_S}{C_L + C_S}\right)$$

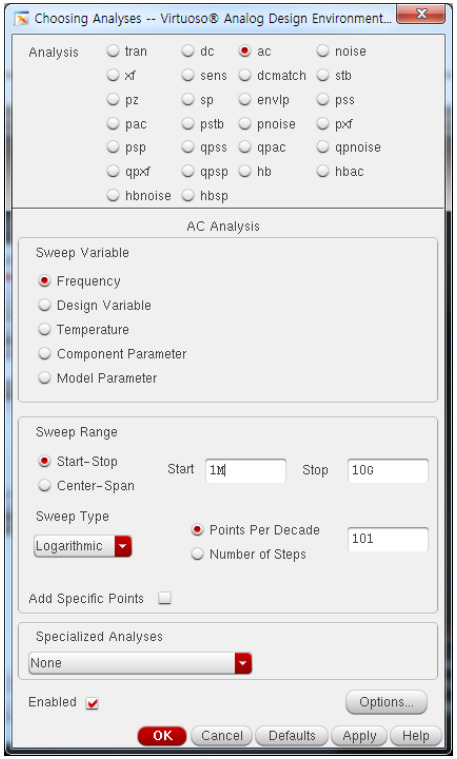
- Goal: Boost at least 6.3dB @ 1GHz
  ➔Equalize 2Gbps data transmission
- 1 pole, 1 zero filter → HPF

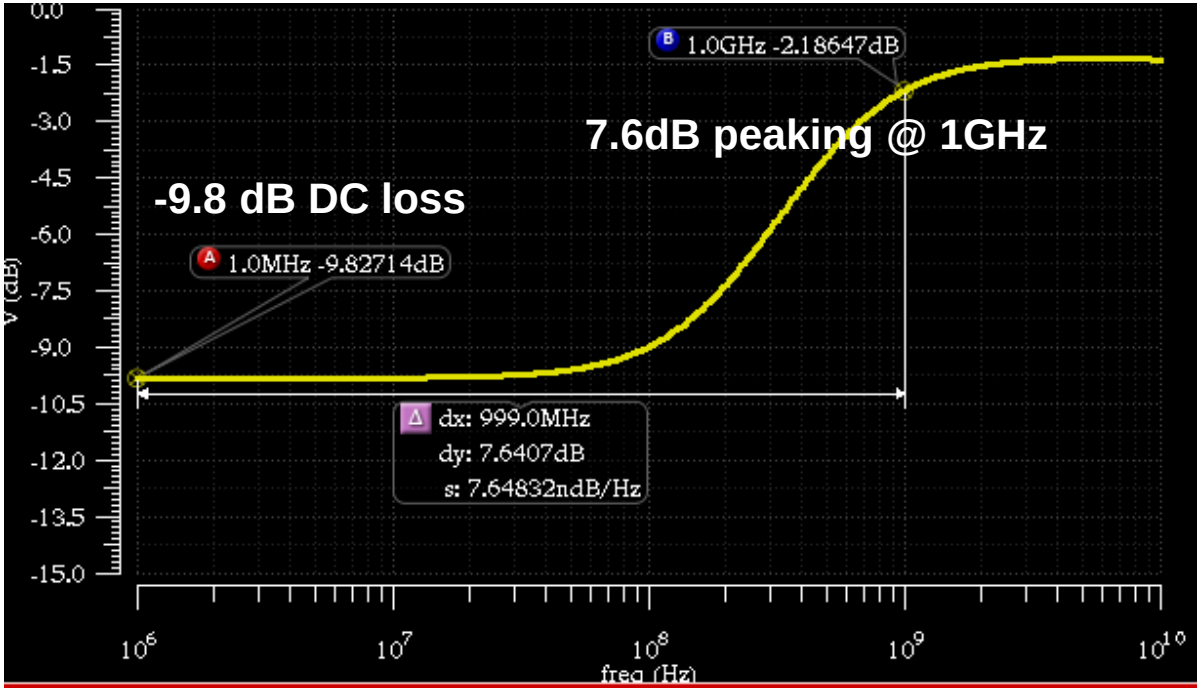
Passive CTLE AC Simulation



- Input source
  - -vcvs gain: ±0.5
  - -V_{CM} : 1.55V
  - -Input resistor: 50 Ohm
  - -Vsin: 1V ac magnitude
- Passive elements
  - -R_S: 1 KΩ
  - -C_S: 800 fF
  - -R_L: 500 Ω
  - -C_L: 50 fF

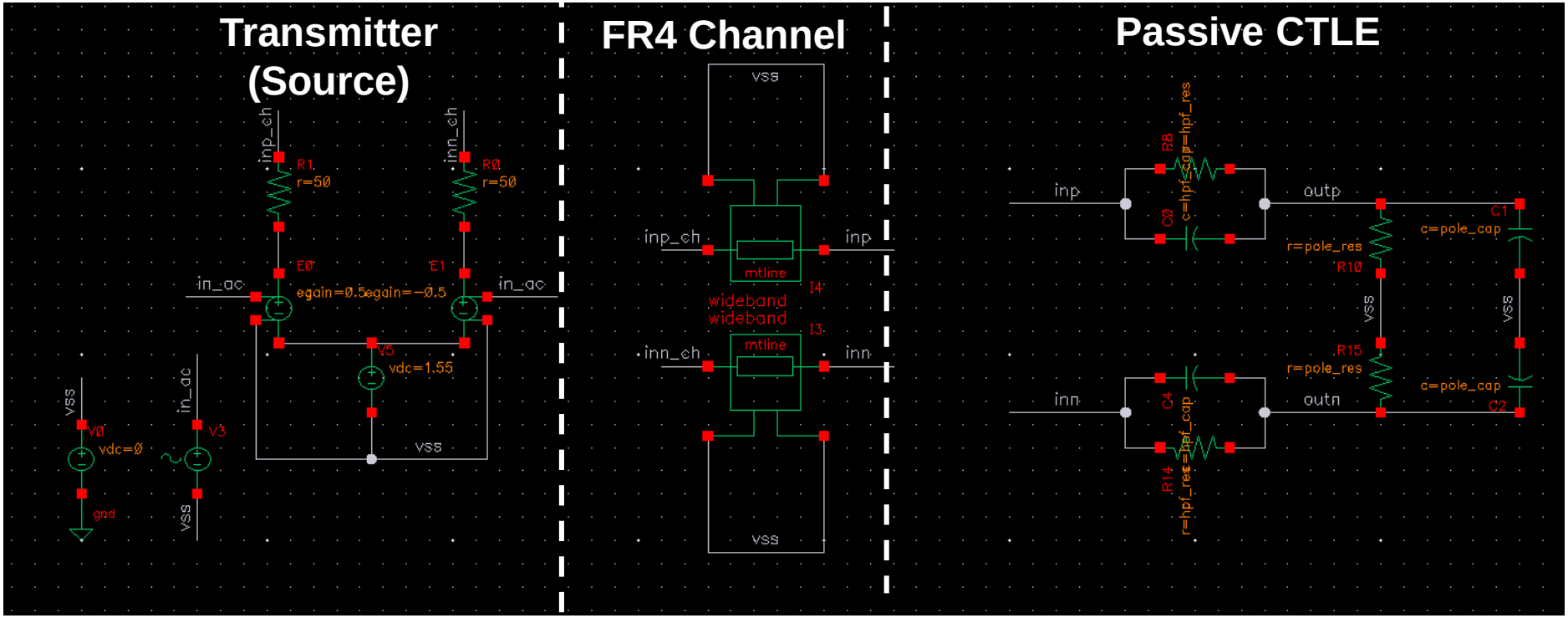
Simulation Results



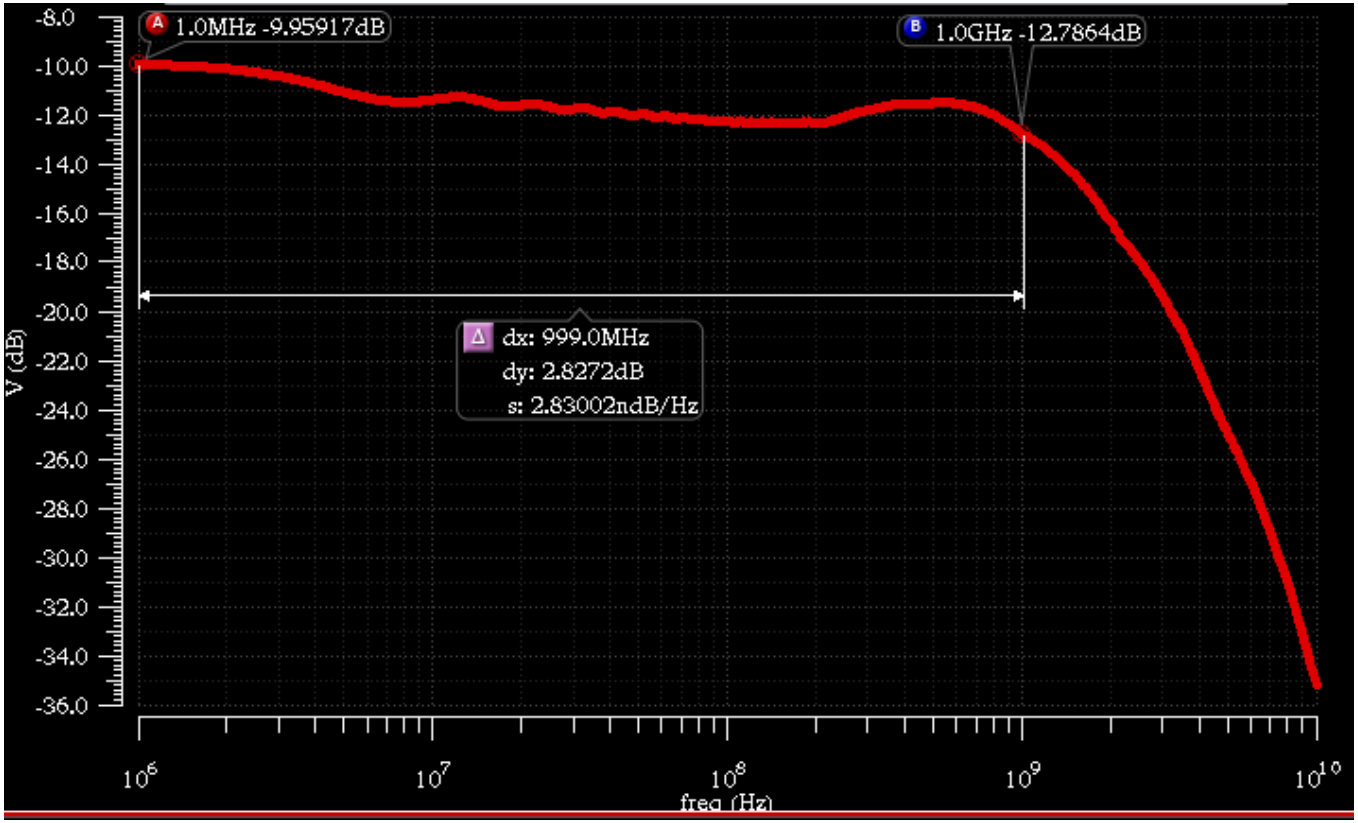


- 1M~10G, logarithmic, 101points
- DC loss : -9.8 dB
- 7.6dB peaking @ 1 GHz (Nyquist frequency)

Simulation setup

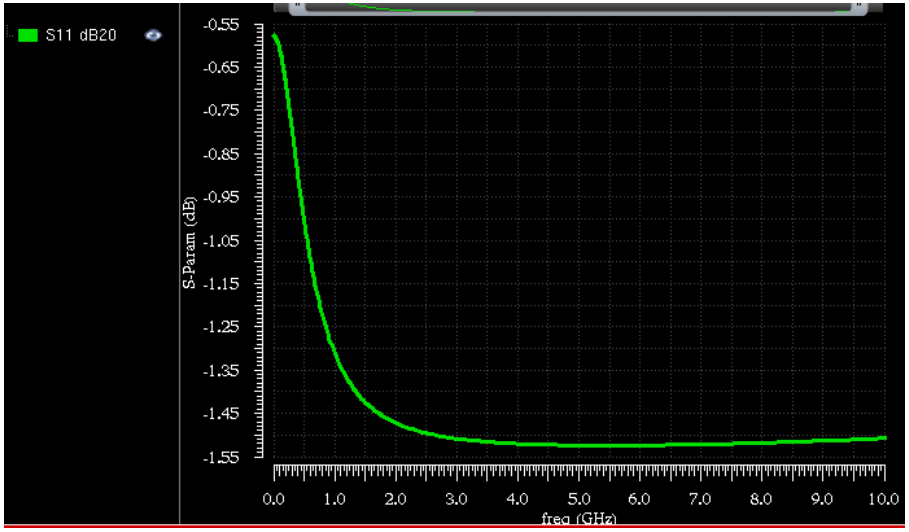


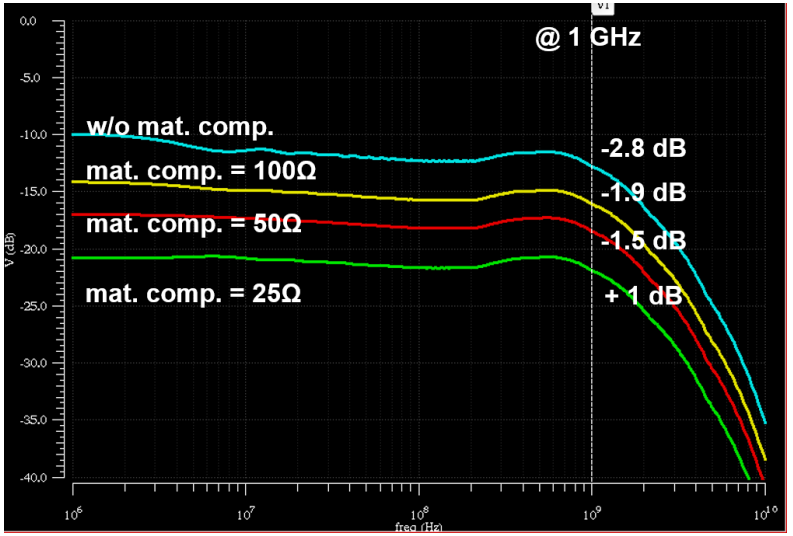
Simulation Results (w/o EQ)



- Expected compensated channel loss @ 1 GHz = -9.3 + 7.6 = - 1.7 dB
- Simulated compensated channel loss @ 1 GHz = - 2.8 dB ???

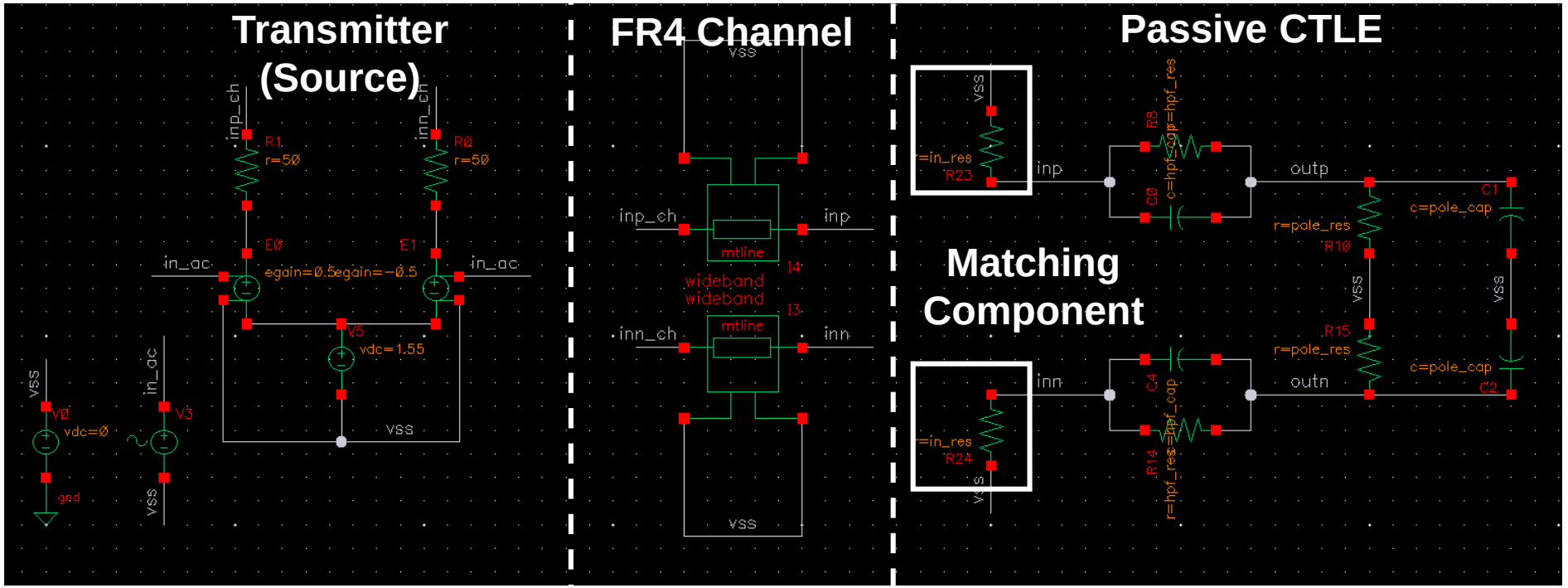
Passive EQ impedance problem



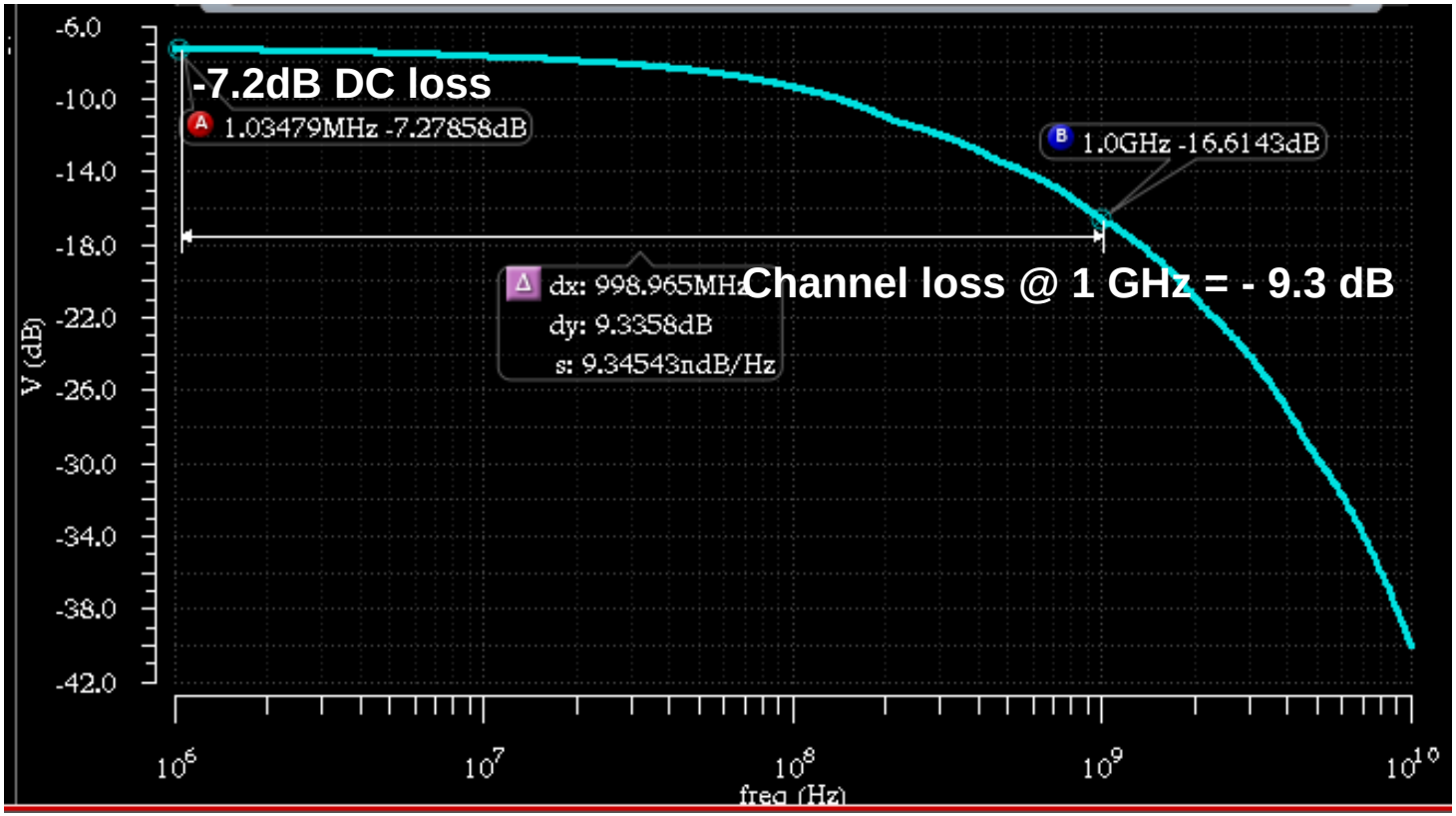


- Input impedance is not well matched!
- To alleviate this problem, additional matching component is needed.
- In practical design, each passive element must be carefully set for impedance matching.

Modified simulation setup



Simulation Results (w/o EQ)

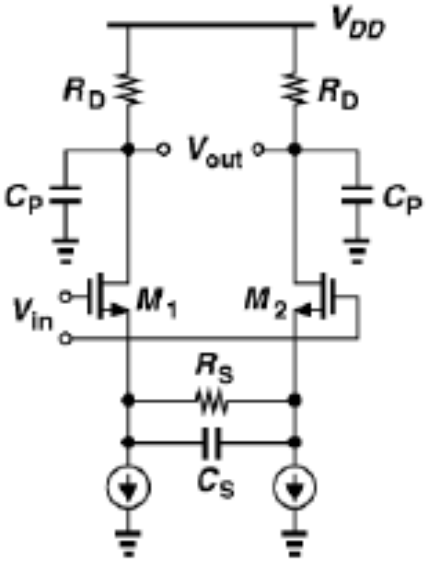


- DC loss = - 6 - 1.2 = - 7.2 dB
- Channel loss @ 1 GHz = - 9.3 dB

Simulation Results (w/ EQ)

- DC loss = -6 - 1.2 - 9.8 = - 17 dB
- Channel loss @ 1 GHz = -9.3 + 7.6 + @ = - 1.5 dB

Active CTLE – Source Degeneration

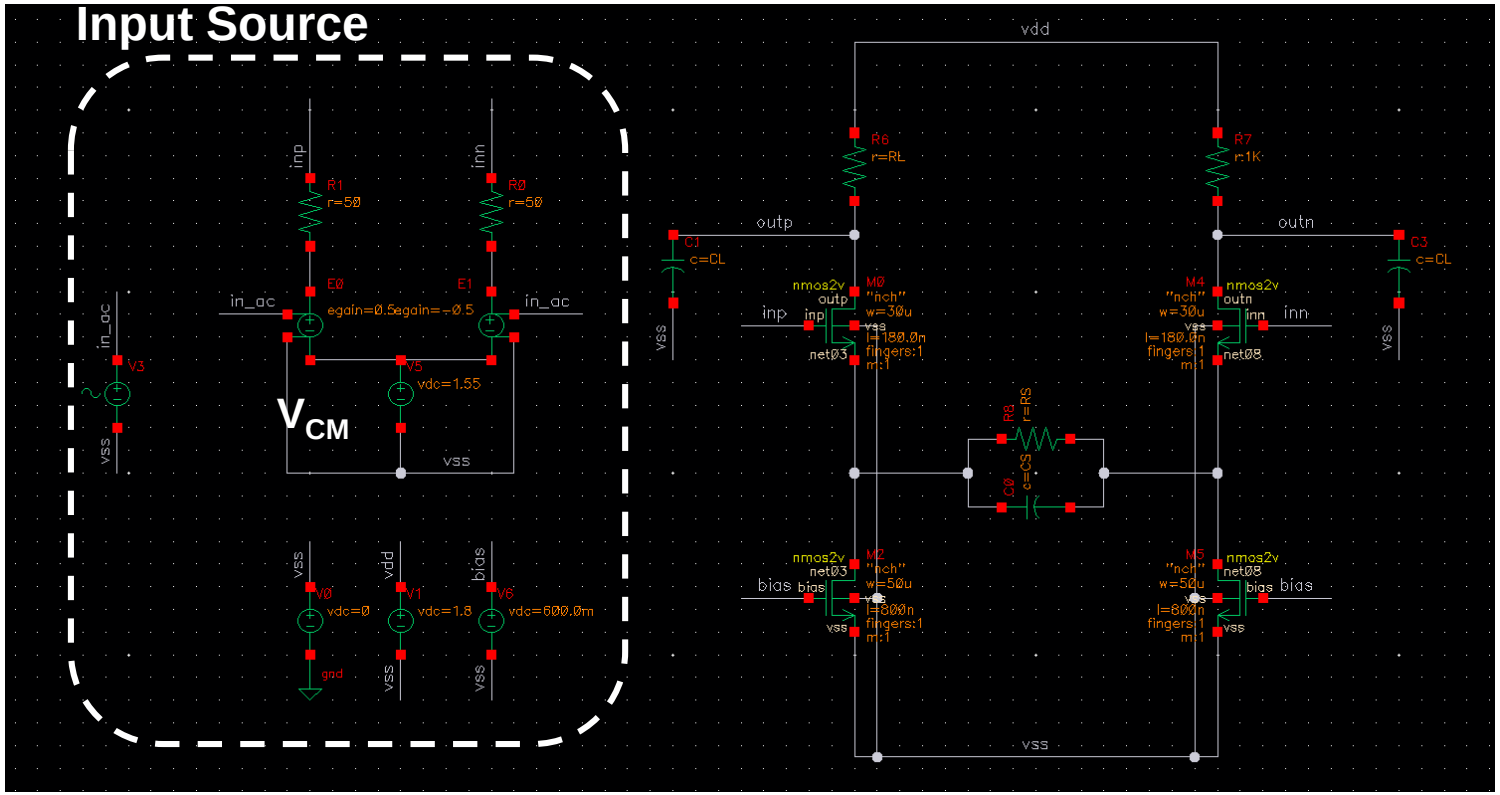


$$H(s) = \frac{g_m}{C_p} \frac{\overbrace{s + \frac{1}{R_S C_S}}^{1^{st}\text{ zero}}}{\underbrace{(s + \frac{1 + \frac{g_m R_S}{2}}{R_S C_S})}_{1^{st}\text{ pole}} \underbrace{(s + \frac{1}{R_D C_p})}_{2^{nd}\text{ pole}}}$$

$$\text{Peaking gain} = 1 + \frac{g_m R_S}{2}$$

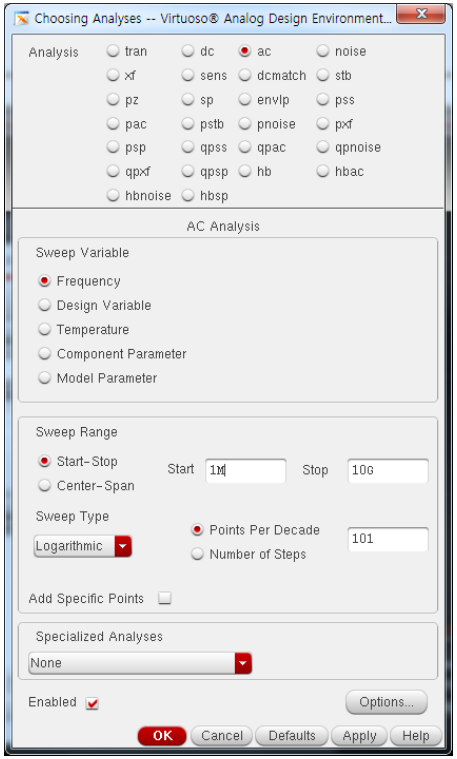
- Goal: Boost at least 6.3dB @ 1GHz
  ➔Equalize 2Gbps data transmission
- 2 pole, 1 zero change with R,C tuning

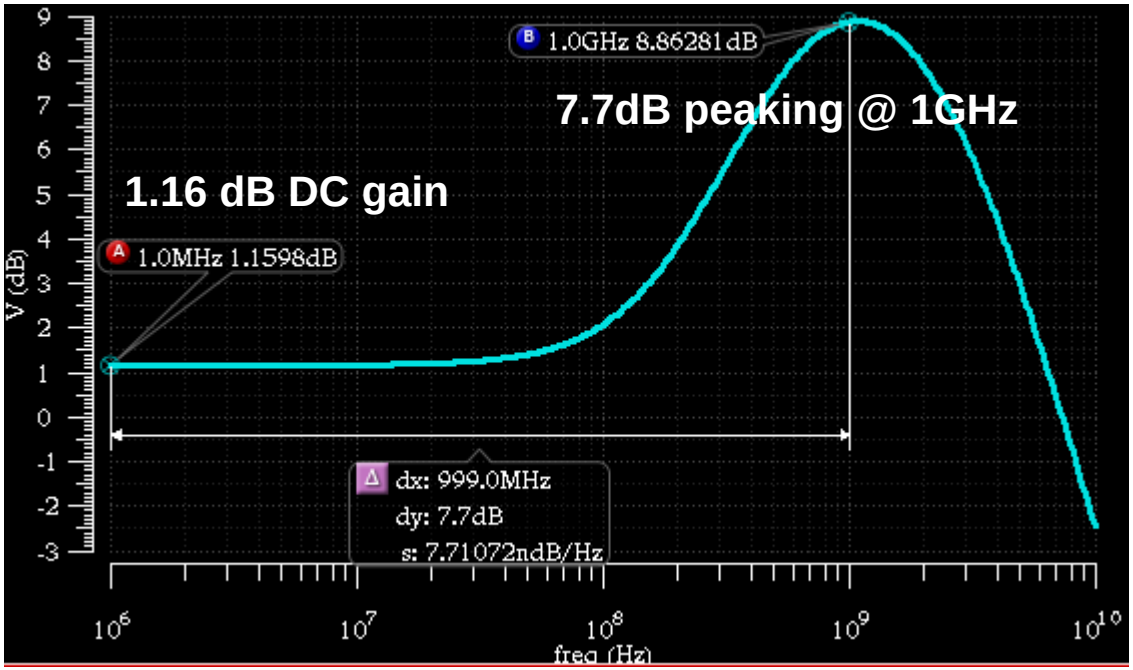
Active CTLE AC Simulation



- Input source
  - -vcvs gain: ±0.5
  - -V_{CM} : 1.55V
  - -Input resistor: 50 Ohm
  - -Vsin: 1V ac magnitude
- CTLE
  - -Input MOSFETs: 30u/180n
  - -Tail MOSFETs: 50u/800n
  - -Load resistors: 1 KΩ
  - -Load capacitor: 50 fF
- Degeneration Filter
  - -R_{deg}: 1 kΩ
  - -C_{deg}: 800 fF
  - -Tail MOSFET bias: 0.6 V

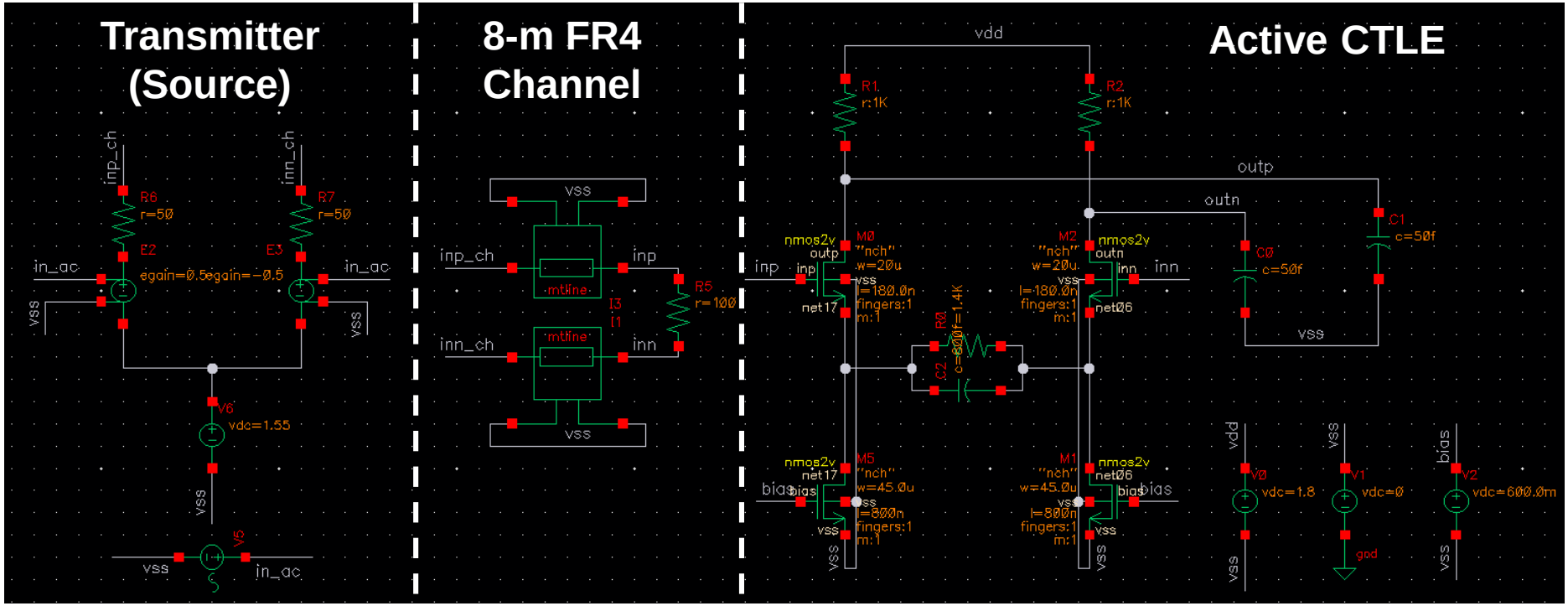
Simulation Results



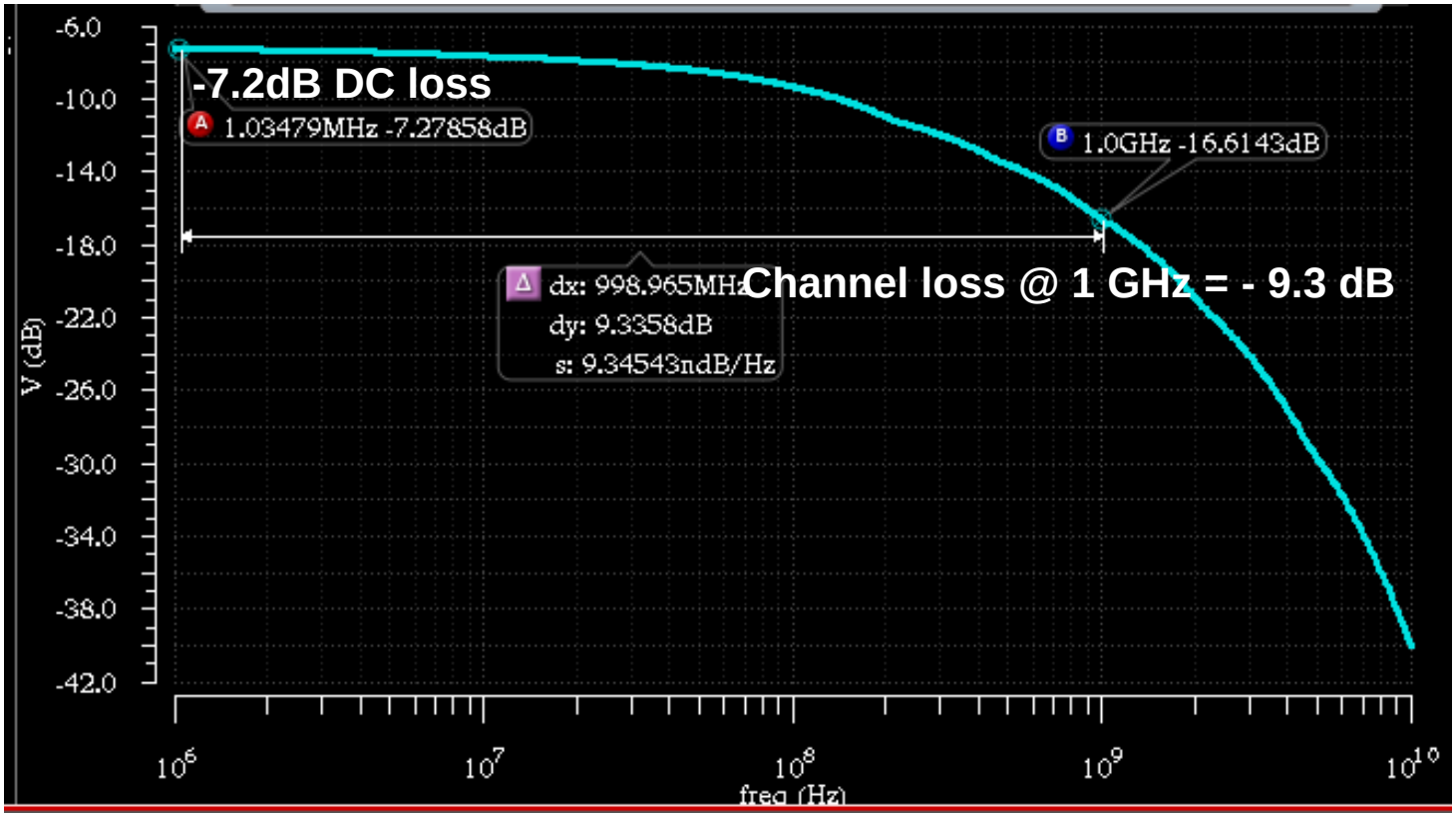


- 1M~10G, logarithmic, 101points
- DC gain : 1.1 dB
- 7.7dB peaking @ 1 GHz (Nyquist frequency)

Channel + CTLE AC Simulation

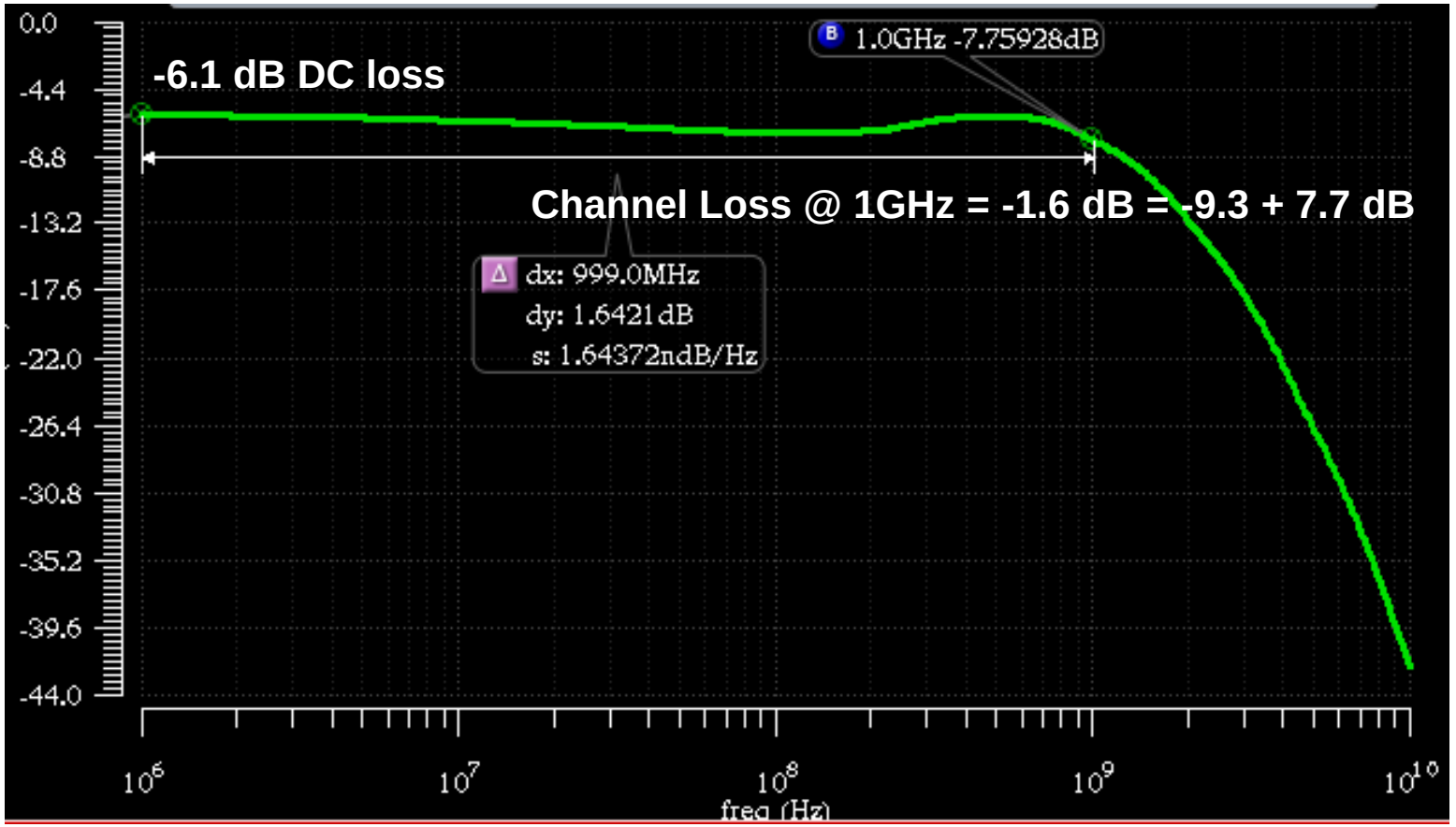


Simulation Results (w/o EQ)



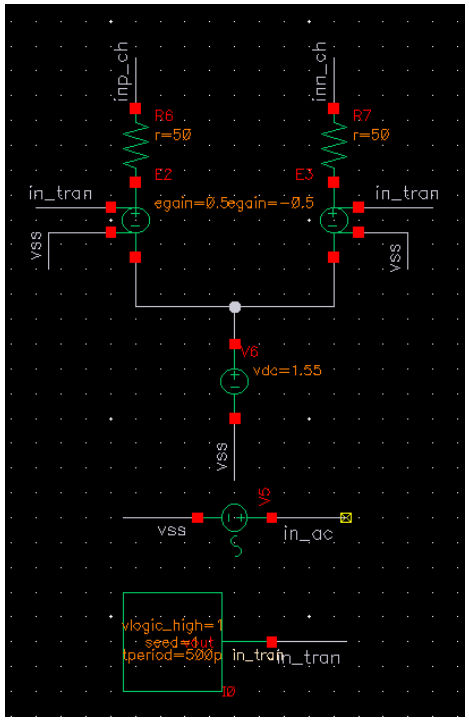
- DC loss = - 6 - 1.2 = - 7.2 dB
- Channel loss @ 1 GHz = - 9.3 dB

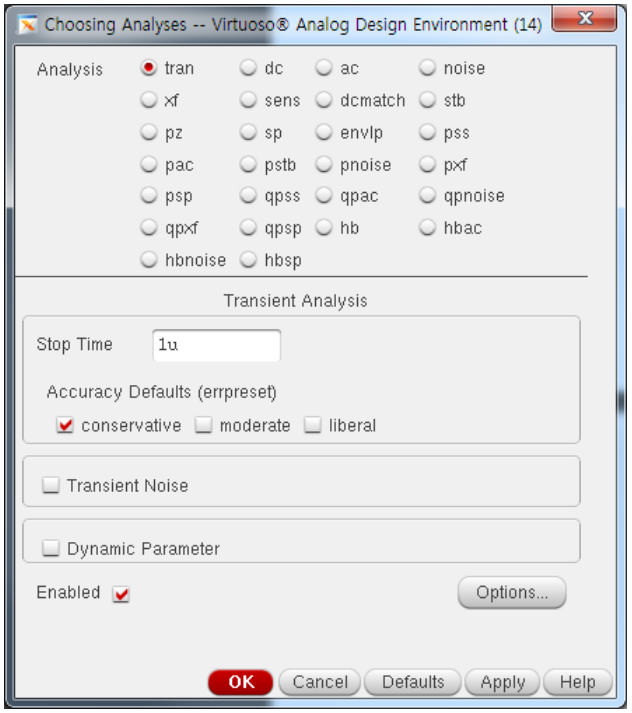
Simulation Results(Channel + CTLE)



- DC loss = -6 - 1.2 + 1.1 = - 6.1 dB
- Channel loss @ 1 GHz = -9.3 + 7.7 = - 1.6 dB

Channel + CTLE Transient Simulation





- Random bit stream

  -Period: 1/2Gbps = 500ps

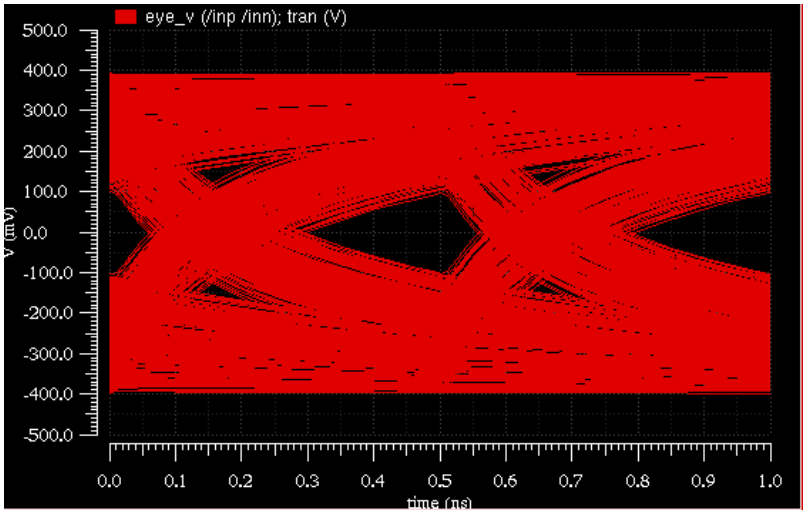
  -seed: 1

  -vlogic_high, low = 1, -1 ➔ 500mV swing to Rx

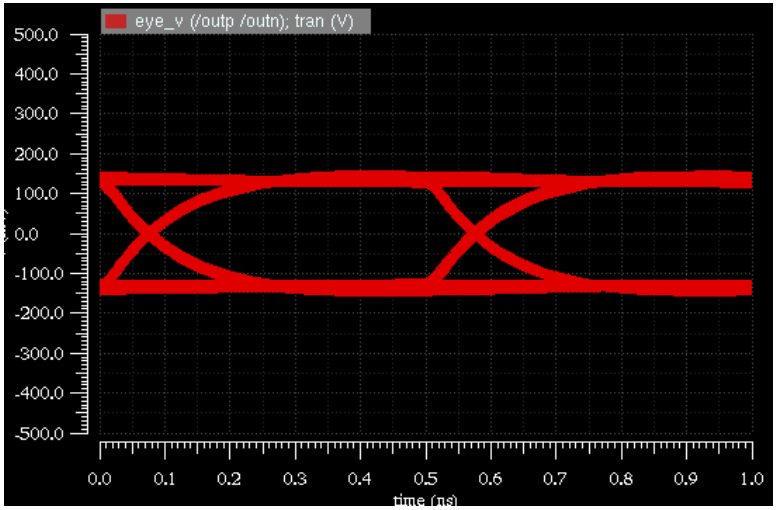
  -trise, tfall = 20p

Simulation Results(Channel + CTLE)

- **Passive CTLE**



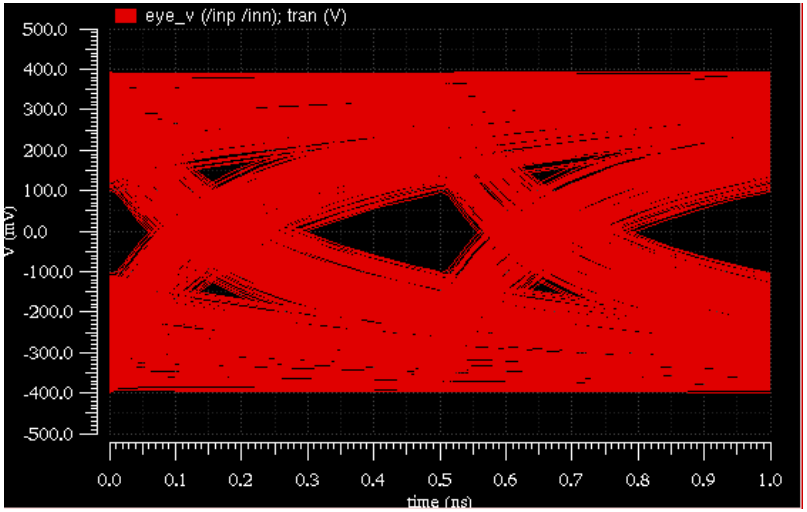
<Before EQ>



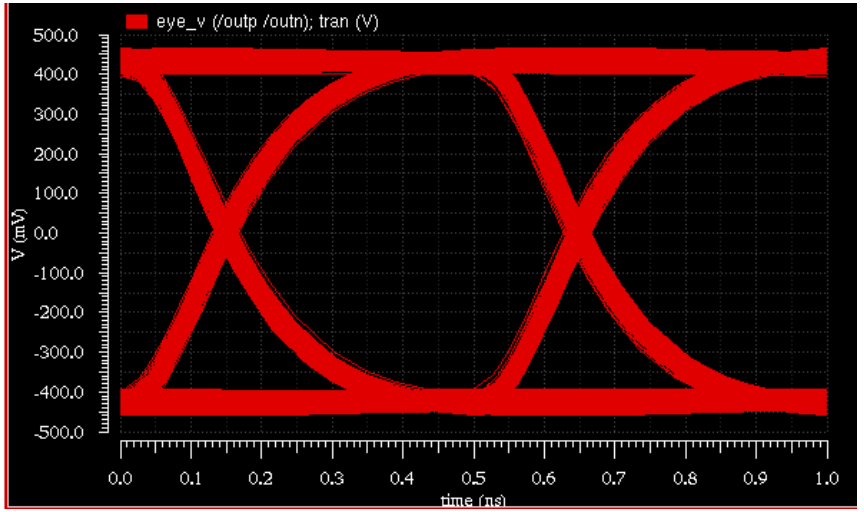
<After EQ>

Simulation Results(Channel + CTLE)

- **Active CTLE – Source degeneration**

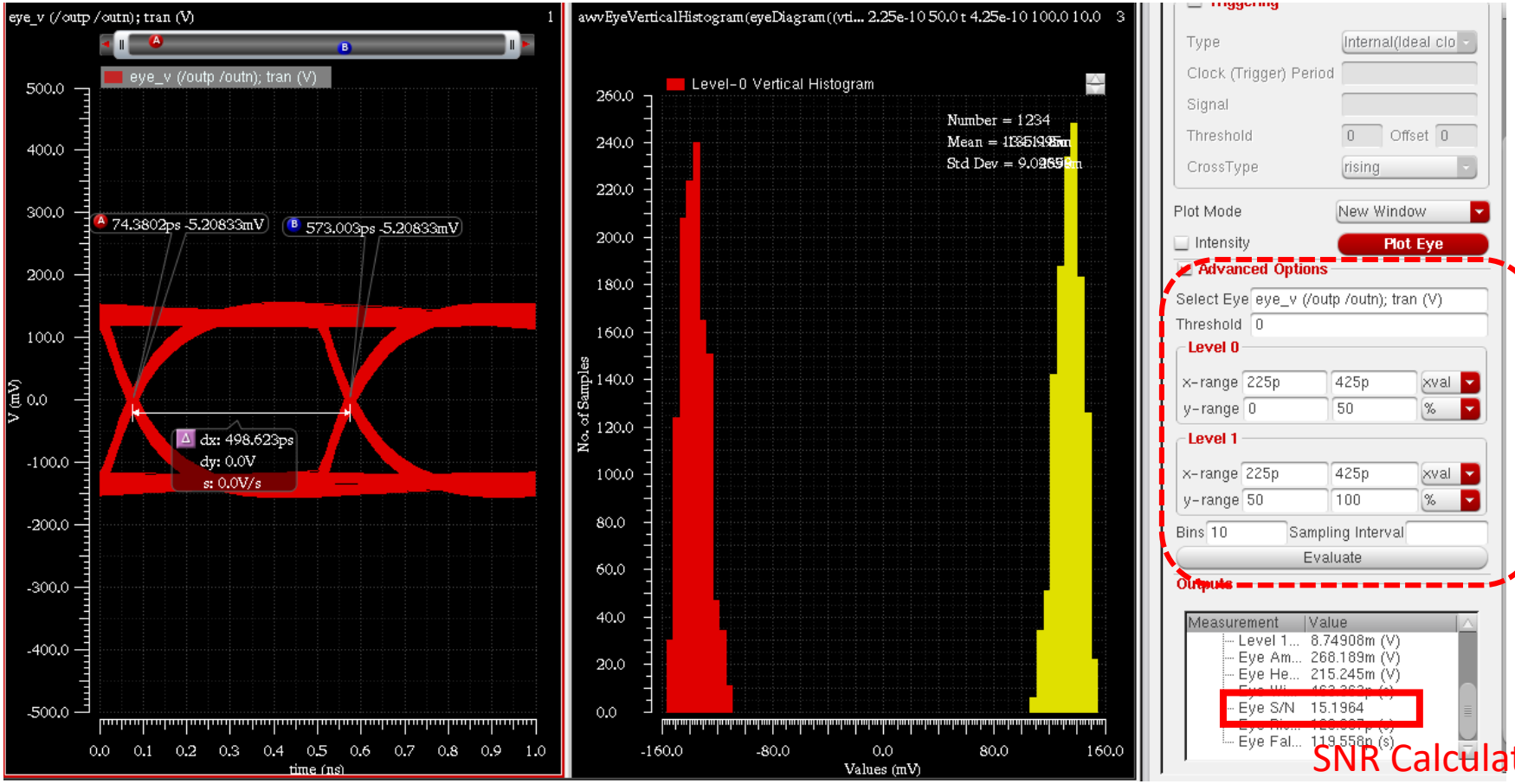


<Before EQ>



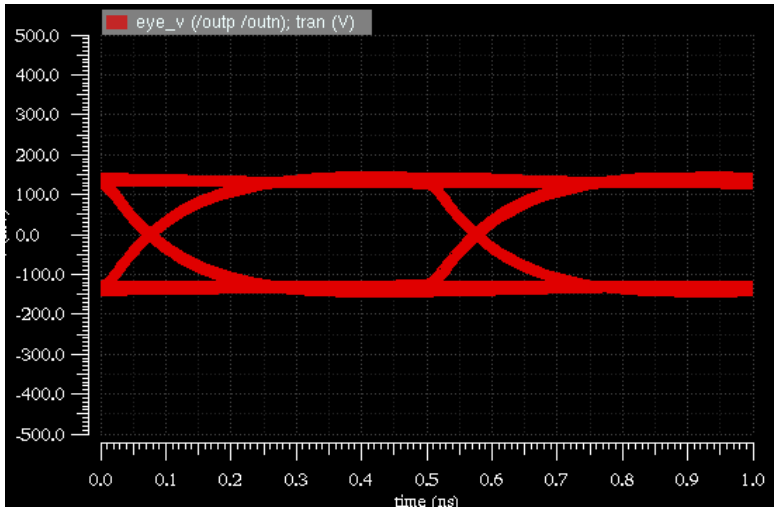
<After EQ>

SNR Calculation



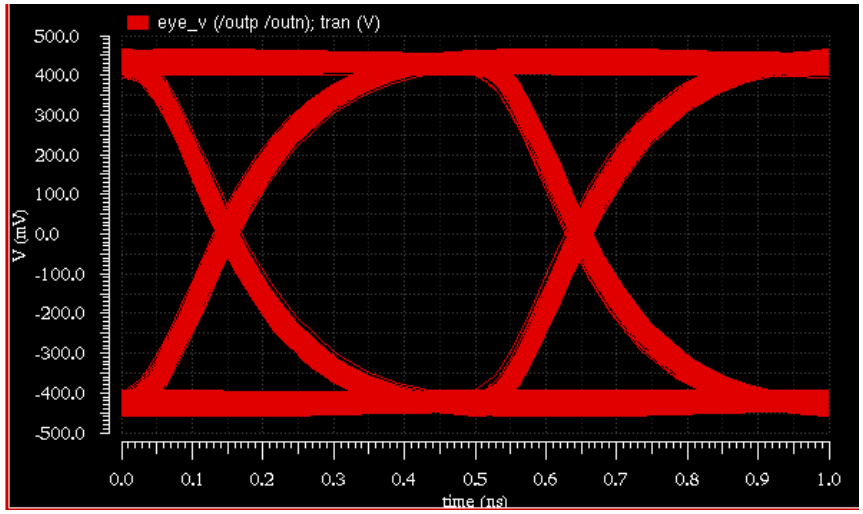
- Calculate the center of your eye diagram. (In this picture, (75p+575p)/2 = 325p
- x-range is +-10% (100ps) from the center of the eye. (In this picture, x-range = 225p ~ 425p)

SNR Calculation



< Passive CTLE >

- Eye level is degraded. (DC loss!)
- No power consumption



< Active CTLE >

- Eye level is not degraded. (by active components)
- Power consumption is needed.

Homework

- Rx CTLE

For the channel used today, design a passive and active CTLE that can recover 3 Gb/s data.

➢ Attach the passive component value, frequency response, and transient simulation results.