Rx Active CTLE

12 Gbps

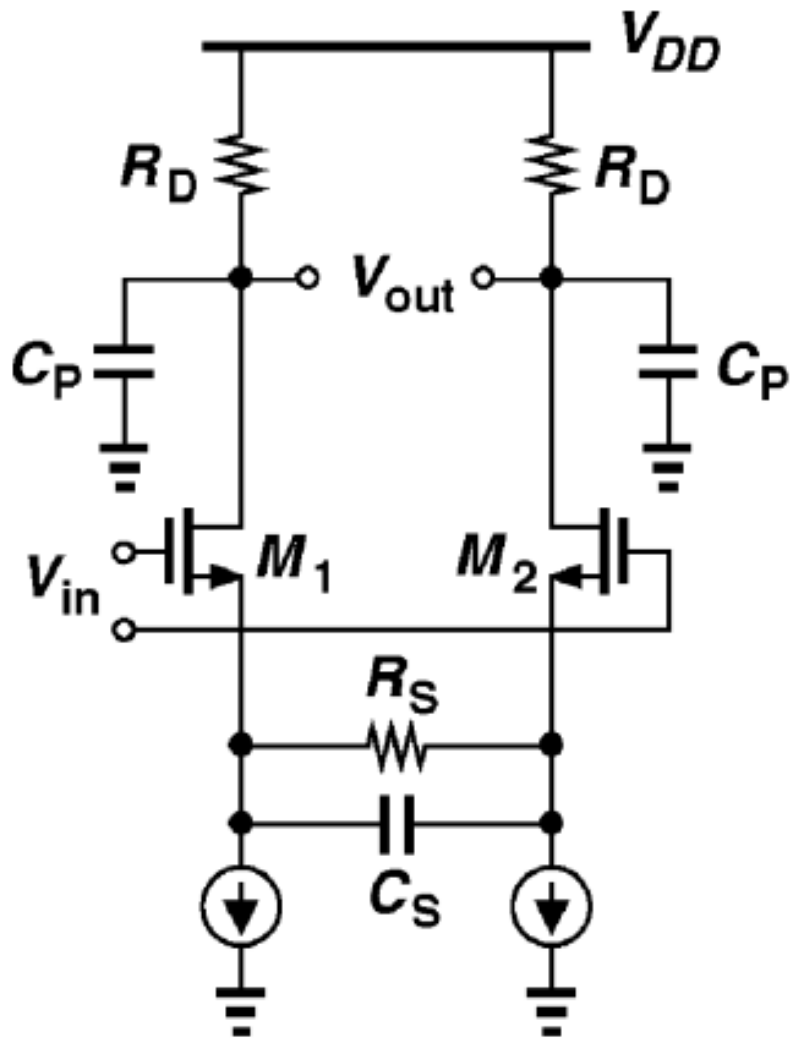
Muhammad Aldacher

Outline

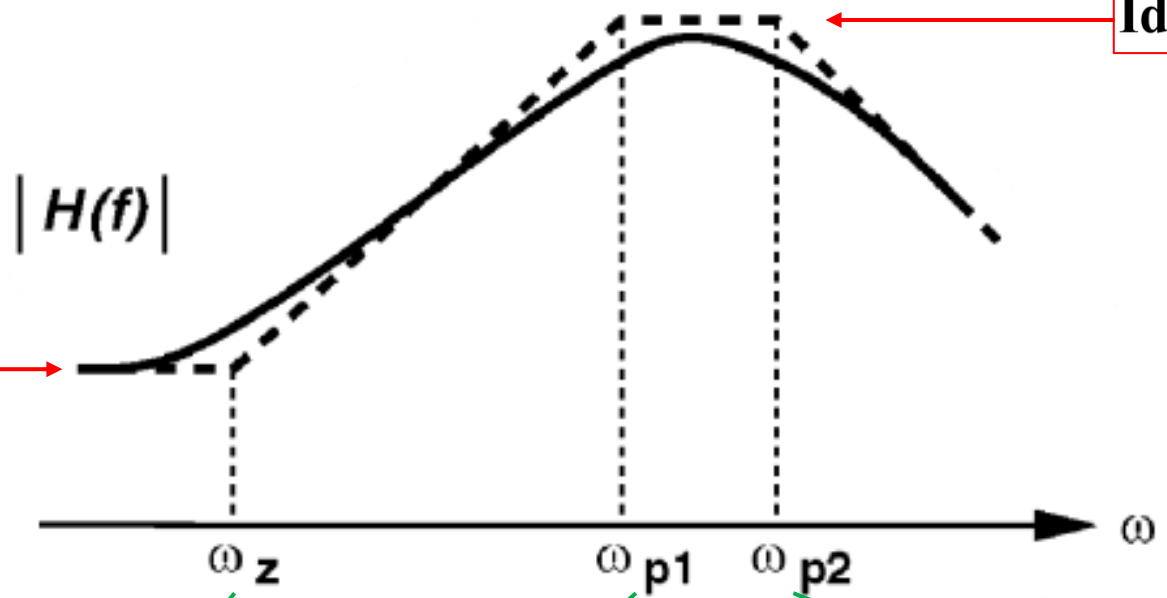
1. Design & Equations
2. Tests & Simulations
   a) Channel:
      i. Frequency response
   b) CTLE only:
      i. DC Analysis (➔ gm)
      ii. AC Analysis (➔ Gain Peaking)
   c) CTLE + Channel:
      i. AC Analysis (➔ Frequency Response)
      ii. Transient Analysis (➔ Eye Diagram)
3. Summary & Conclusion

Design Topology & Equations

Active CTLE



Active CTLE



Ideal peak gain $= g_m R_D$

DC gain $= \dfrac{g_m R_D}{1 + g_m R_S / 2}$

$\omega_z = \dfrac{1}{R_S C_S}$

$\omega_{p1} = \dfrac{1 + g_m R_S / 2}{R_S C_S}$

$\omega_{p2} = \dfrac{1}{R_D C_p}$

$$\textbf{Ideal Peaking} = \frac{\textbf{Ideal peak gain}}{\textbf{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_S / 2$$

Tests & Simulations

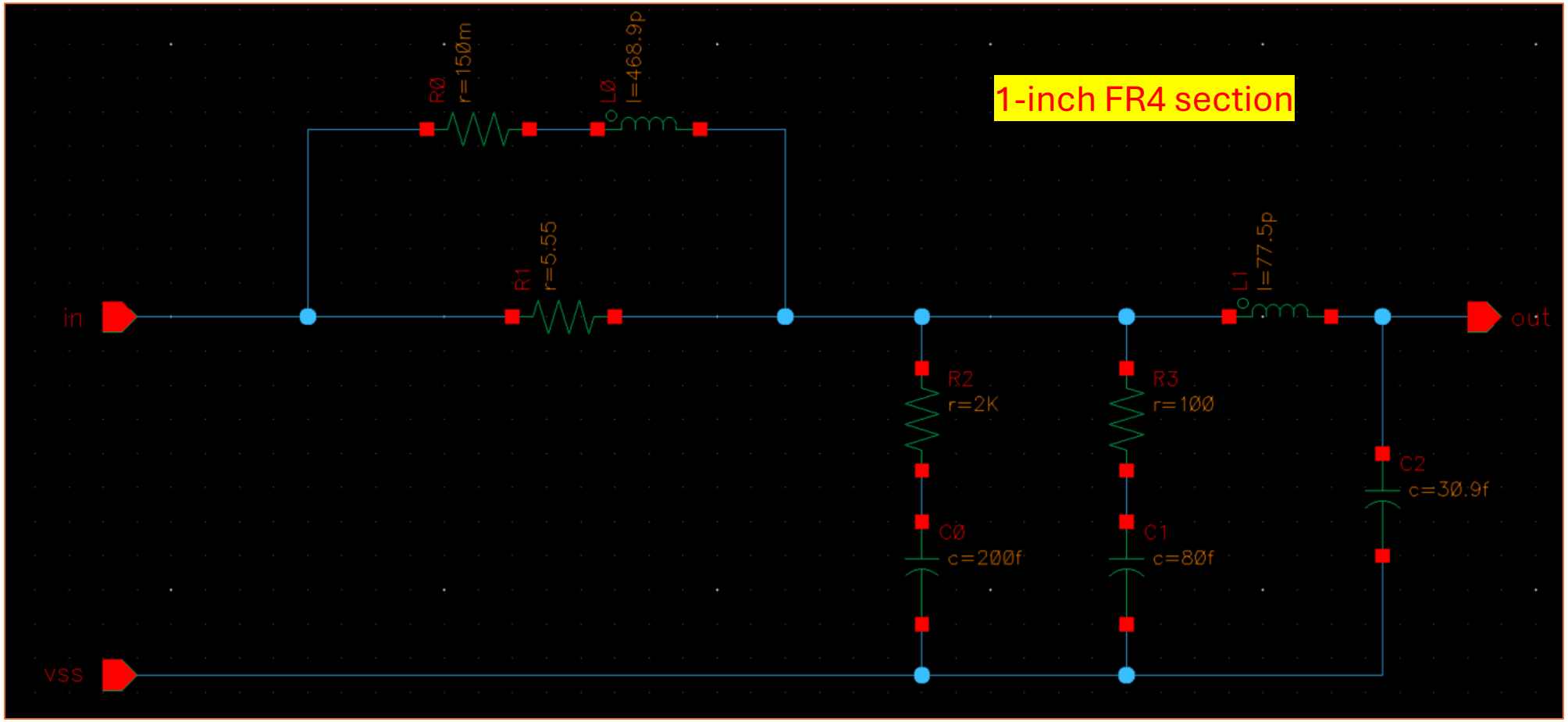
Design Parameters

Parameter	Value
Data Rate	12 Gb/s
VDD (for CTLE)	1.2 V
Input $V_{SWING\ (PK2PK)}$	0.5 V
Input V_{CM}	0.75 V
Channel	12-inch FR4
Output V_{CM}	0.6 V

a) Channel

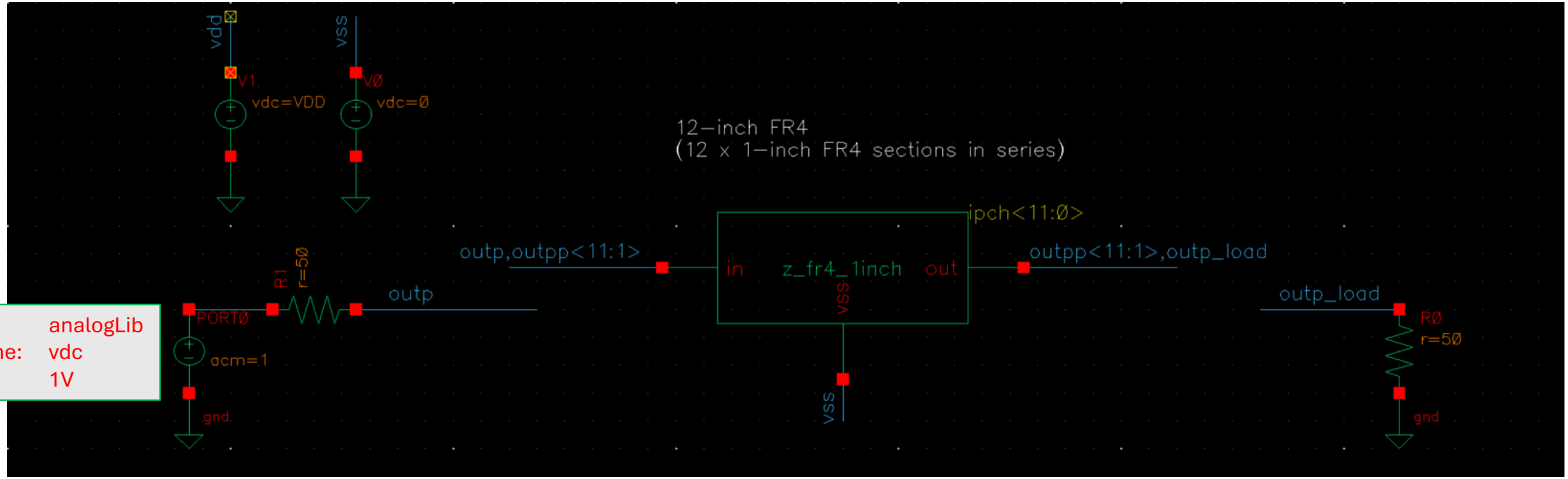
The frequency response can be found by 2 methods:
Single–ended or Differential

Channel = 12 x 1-inch FR4 section



1) Single-Ended:

Testbench



Library:	analogLib
Cell Name:	vdc
AC mag:	1V

1) Single-Ended:

Setup

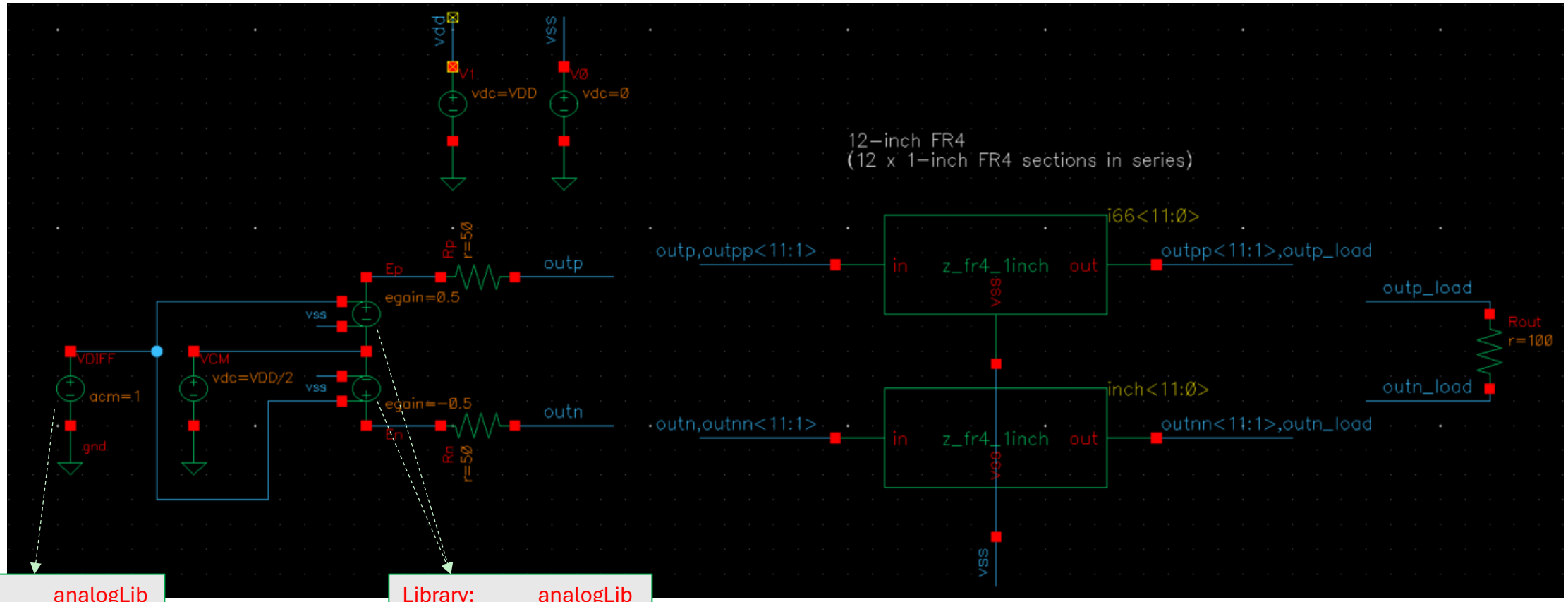
Name	Value
Filter	Filter
Tests	
AC	
Simulator	spectre
Analyses	
ac	1K 15G 300 Logarithmic Points Per Decade Start-Stop
Click to add analysis	
Design Variables	
Click to add test	
Global Variables	
VDD	1
Data_rate	12G

Measurements:

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Gain	expr	dB20(VF("/outp_load"))	point
Gain_at_Nyq	expr	value(Gain (VAR("Data_rate") / 2))	point

2) Differential:

Testbench



Library:	analogLib
Cell Name:	vdc
AC mag:	1V

Library:	analogLib
Cell Name:	vcvs
Voltage Gain:	+/− 0.5

2) Differential:

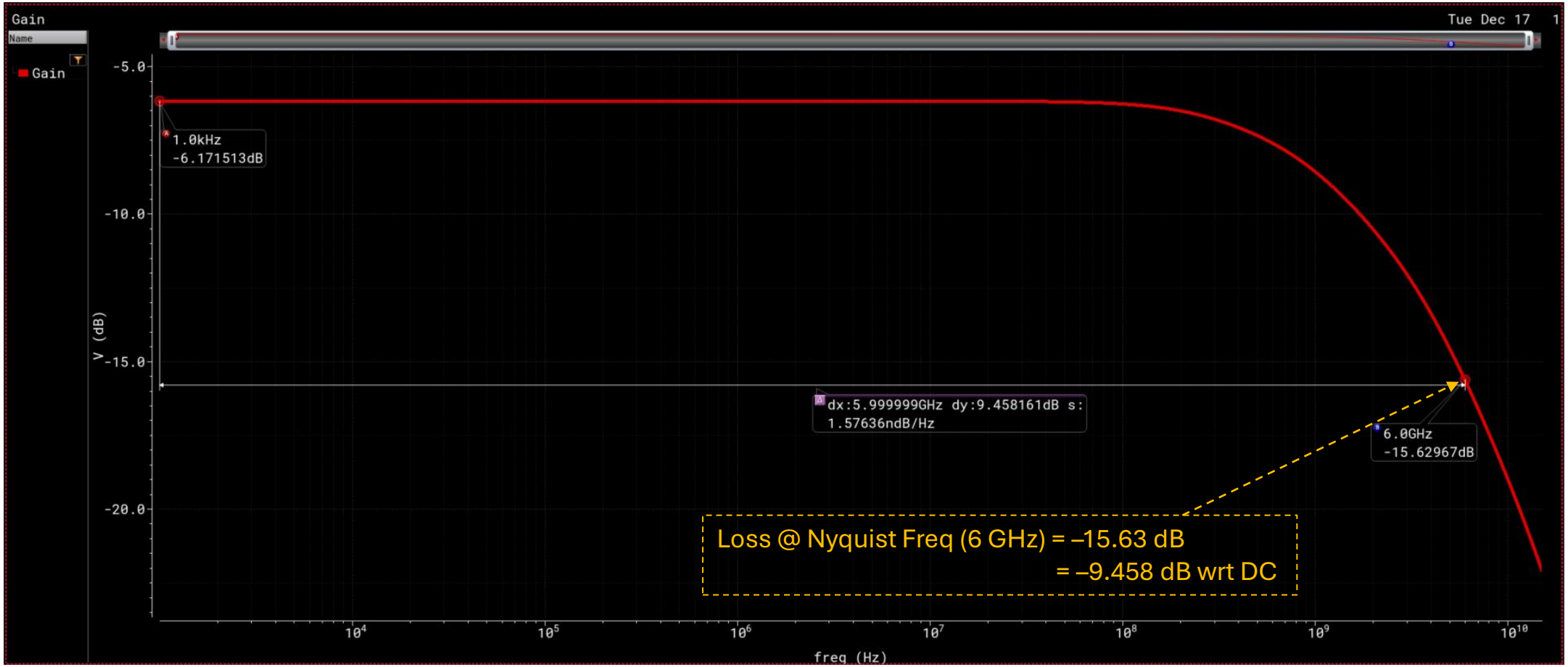
Setup

Name	Value
Filter	Filter
Tests	
AC	
Simulator	spectre
Analyses	
ac	1K 15G 300 Logarithmic Points Per Decade Start-Stop
Click to add analysis	
Design Variables	
Click to add test	
Global Variables	
VDD	1
Data_rate	12G

Measurements:

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Gain	expr	dB20((VF("/outp_load") - VF("/outn_load")))	point
Gain_at_Nyq	expr	value(Gain (VAR("Data_rate") / 2))	point
Gain_at_Nyq_wrt_dc	expr	(Gain_at_Nyq - value(Gain 0))	point

Channel's Frequency Response

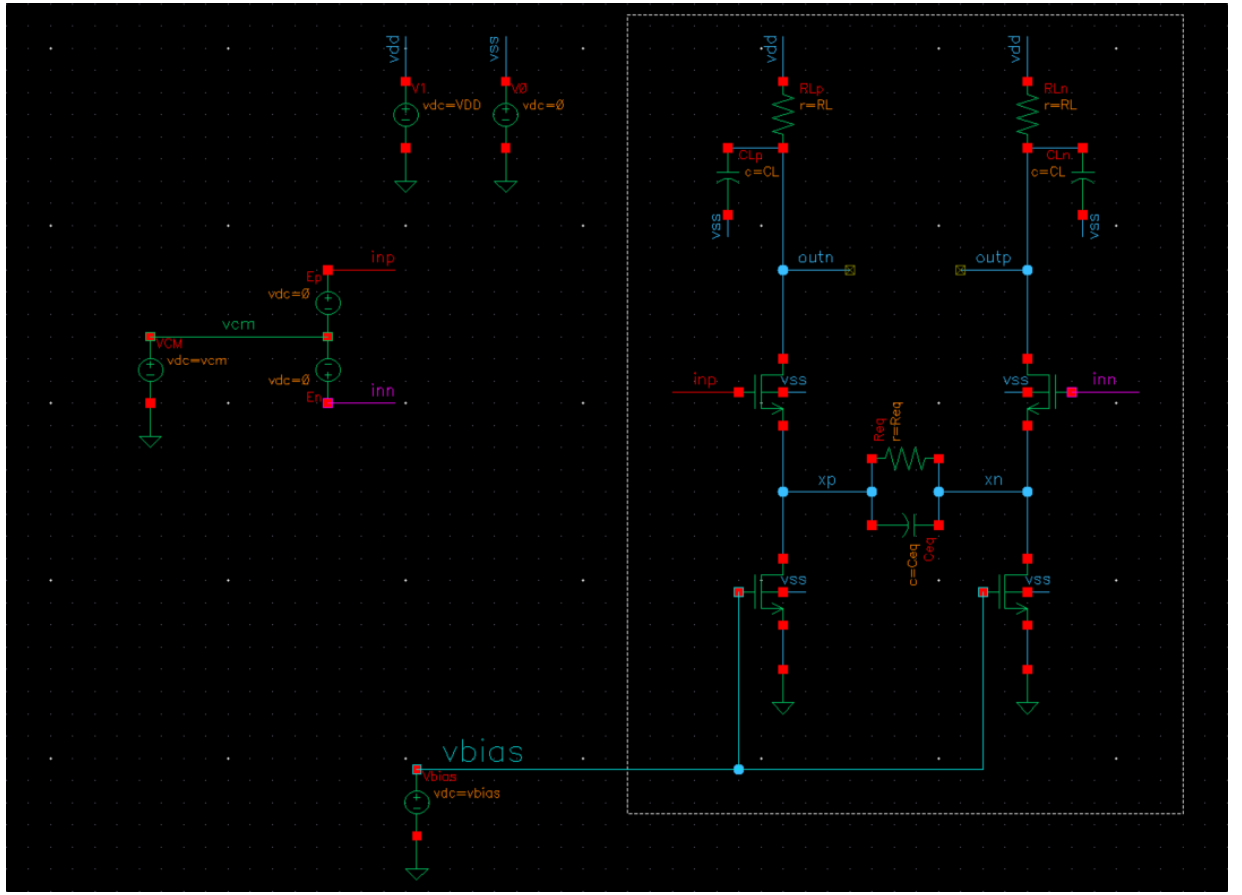


b) CTLE

1) DC Analysis:

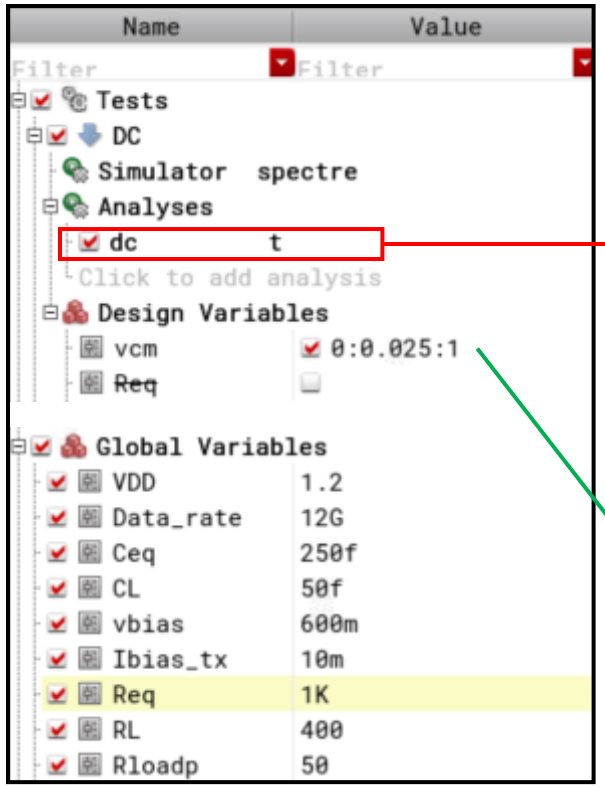
➔ We use the DC Analysis to design for the required gm, output DC level, & current consumption.

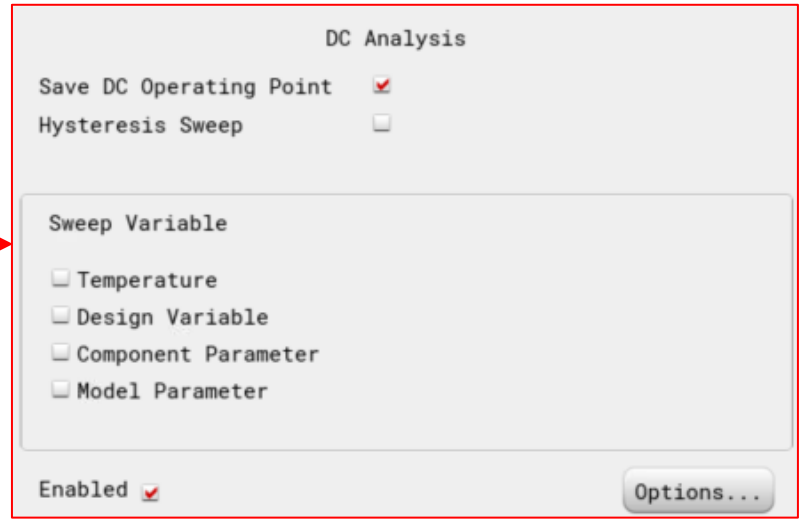
Testbench



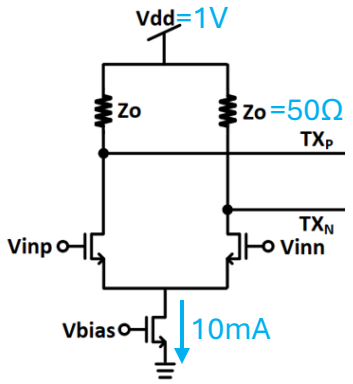
1) DC Analysis:

Setup





- The input CM voltage is swept to see how gm changes.
- The input CM voltage comes from the output CM voltage of the TX driver.
  (Or a bypass Cap can be added to make input VCM of CTLE independent of TX)



$VCM = V_{DD} - ((I_{bias}/2) * Z_o)$
$= 1V - (5mA * 50\Omega)$
$= 0.75V$

1) DC Analysis:

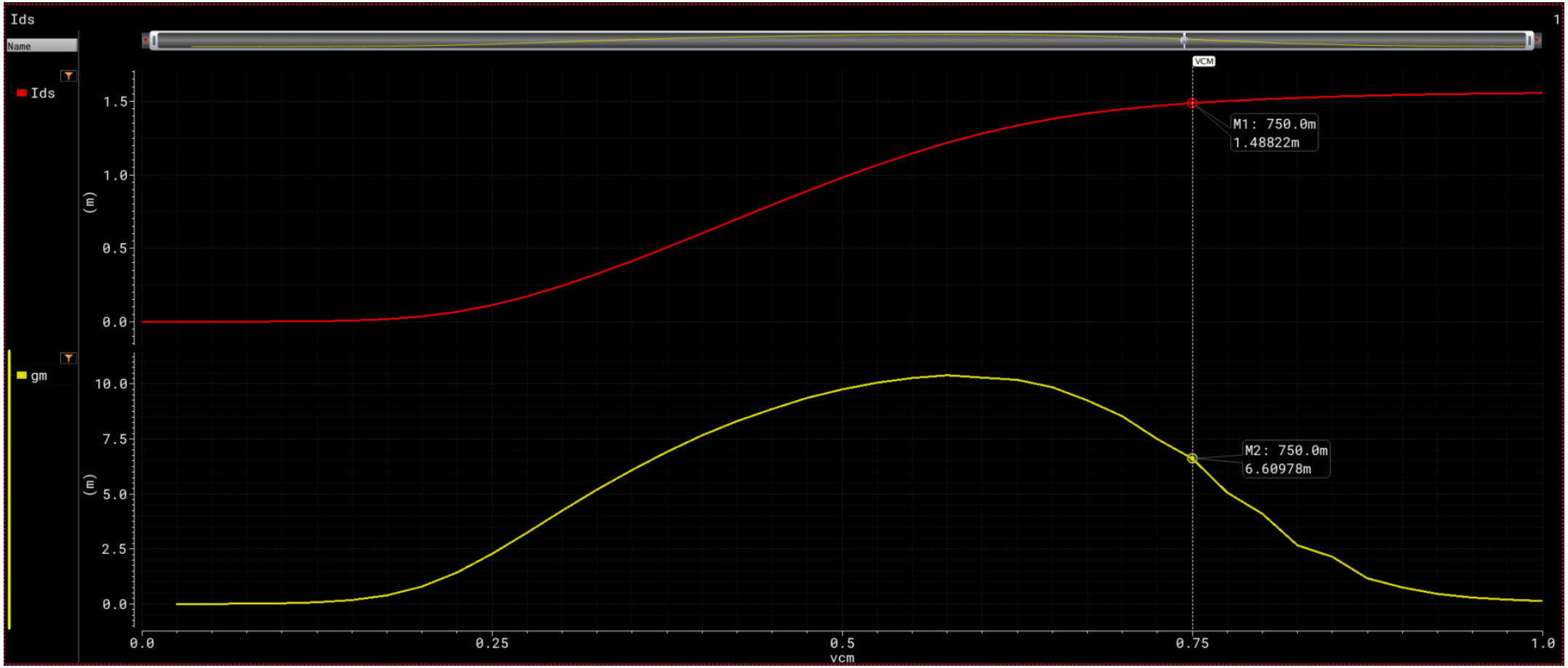
Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
VCM	expr	VDC("/vcm")	point
xp	expr	VDC("/xp")	point
xn	expr	VDC("/xn")	point
vbias	expr	VDC("/vbias")	point
outp	expr	VDC("/outp")	point
outn	expr	VDC("/outn")	point
I_branch	expr	IDC("/RLp/PLUS")	point
Vgs_in	expr	(VDC("/vcm") - VDC("/xp"))	point
Ids	expr	I_branch	sweeps
dIds	expr	deriv(I_branch)	sweeps
dVgs	expr	deriv(Vgs_in)	sweeps
gm	expr	(dIds / dVgs)	sweeps
gm_vcm	expr	value(gm 0.75)	sweeps
Out_vcm	expr	value(outp 0.75)	sweeps
Ids_vcm	expr	value(Ids 0.75)	sweeps

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{\left(\frac{dI_{DS}}{dV_{CM}}\right)}{\left(\frac{dV_{GS}}{dV_{CM}}\right)}$$

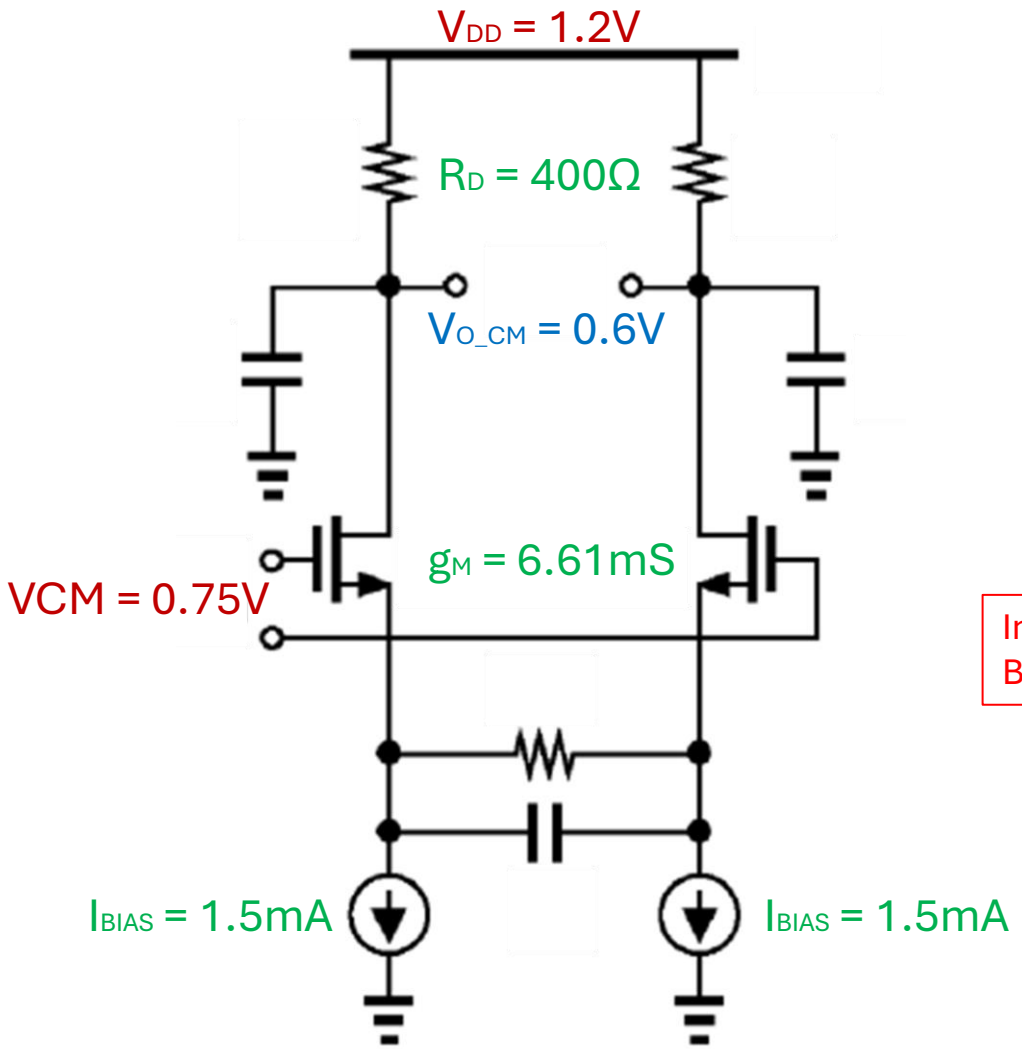
1) DC Analysis:

Results



1) DC Analysis:

Results

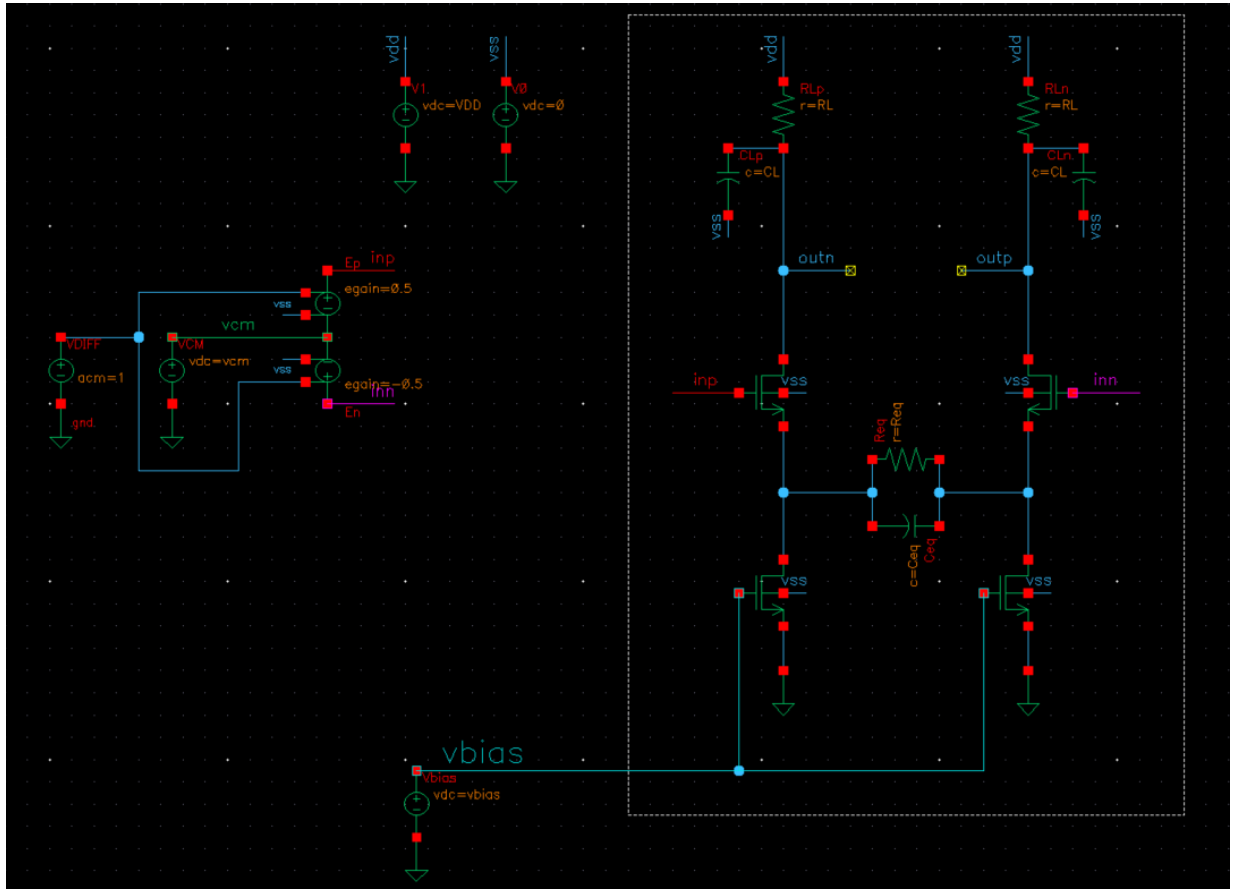


Input NMOS devices: $L = 2 * L_{MIN}$, m=30x
Bias NMOS devices: $L = 4 * L_{MIN}$, m=16x

2) AC Analysis:

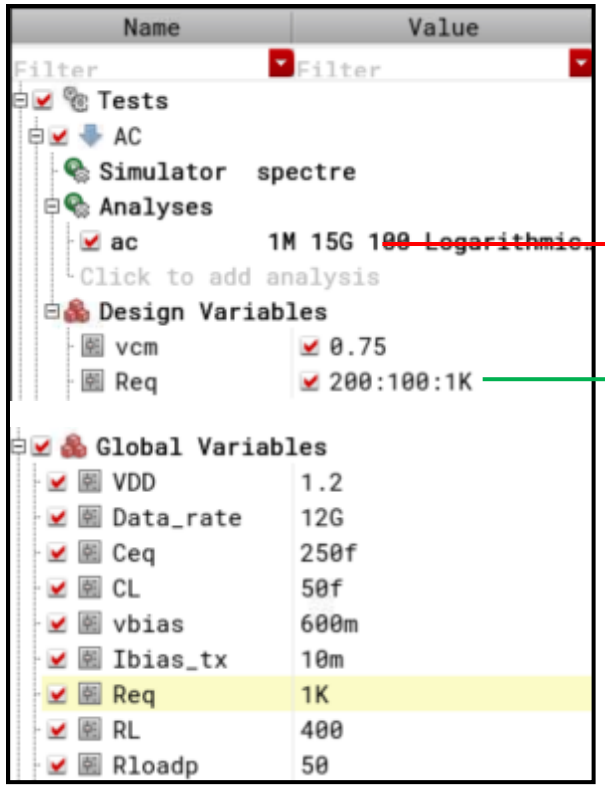
➔ We use the AC Analysis to design for the required gain peaking, zero & pole frequencies.

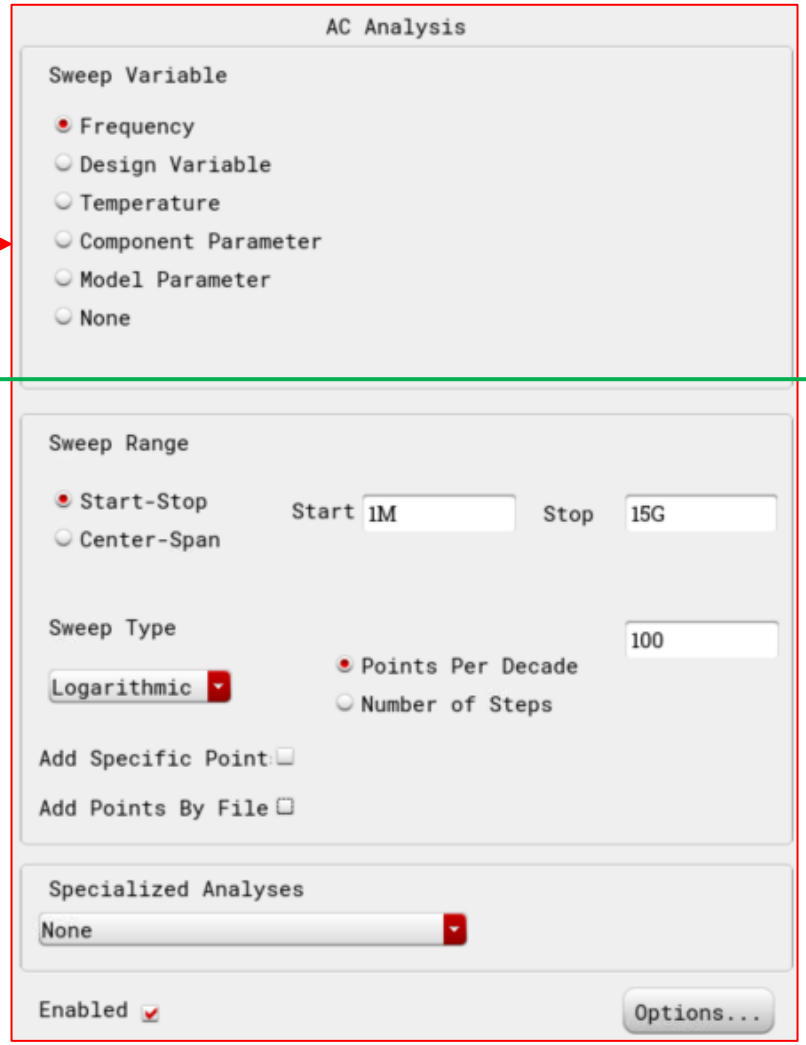
Testbench



2) AC Analysis:

Setup





- The degeneration R (or C) can be swept to change the amount of equalization or gain peaking.

2) AC Analysis:

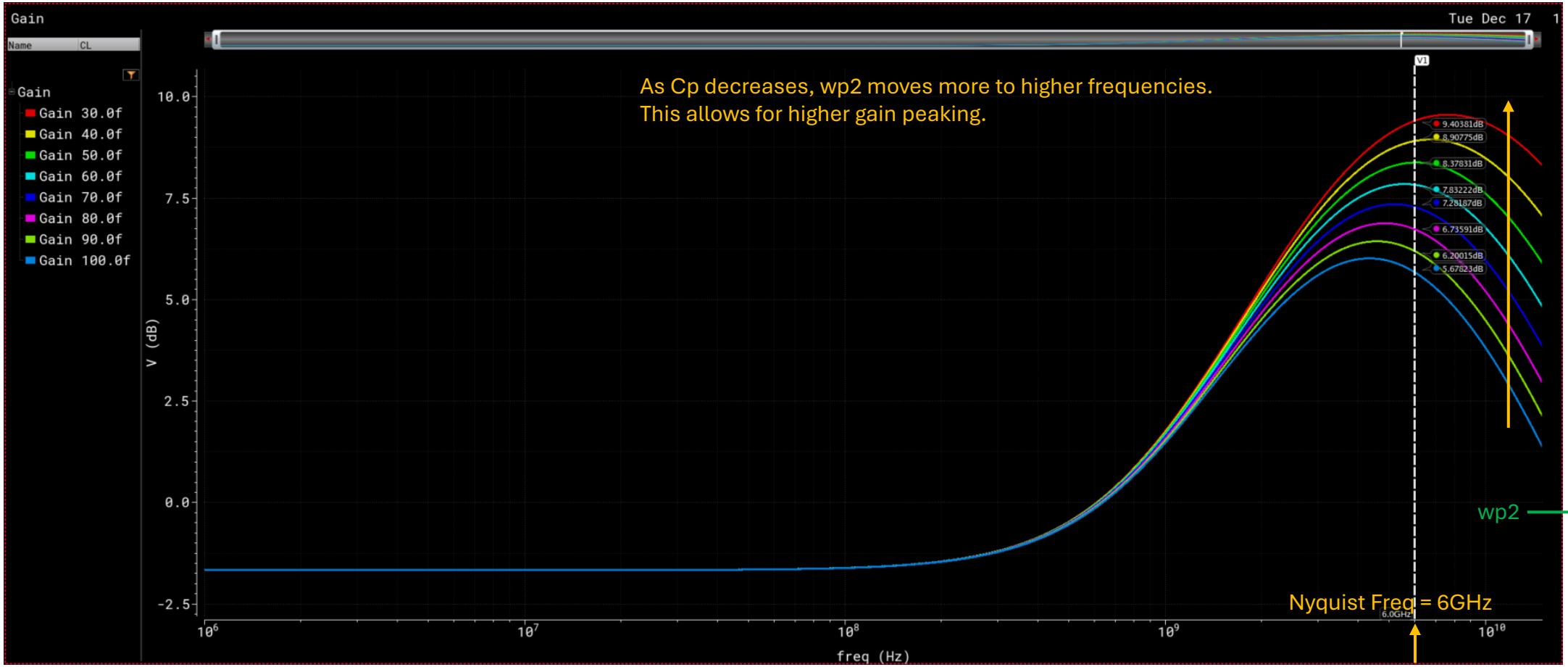
Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Gain	expr	dB20((VF("/outp") - VF("/outn")))	point
Gain_at_DC	expr	value(Gain 0)	point
Gain_at_Nyq	expr	value(Gain (VAR("Data_rate") / 2))	point
Peaking	expr	(Gain_at_Nyq - Gain_at_DC)	point

2) AC Analysis:

Results - Sweeps

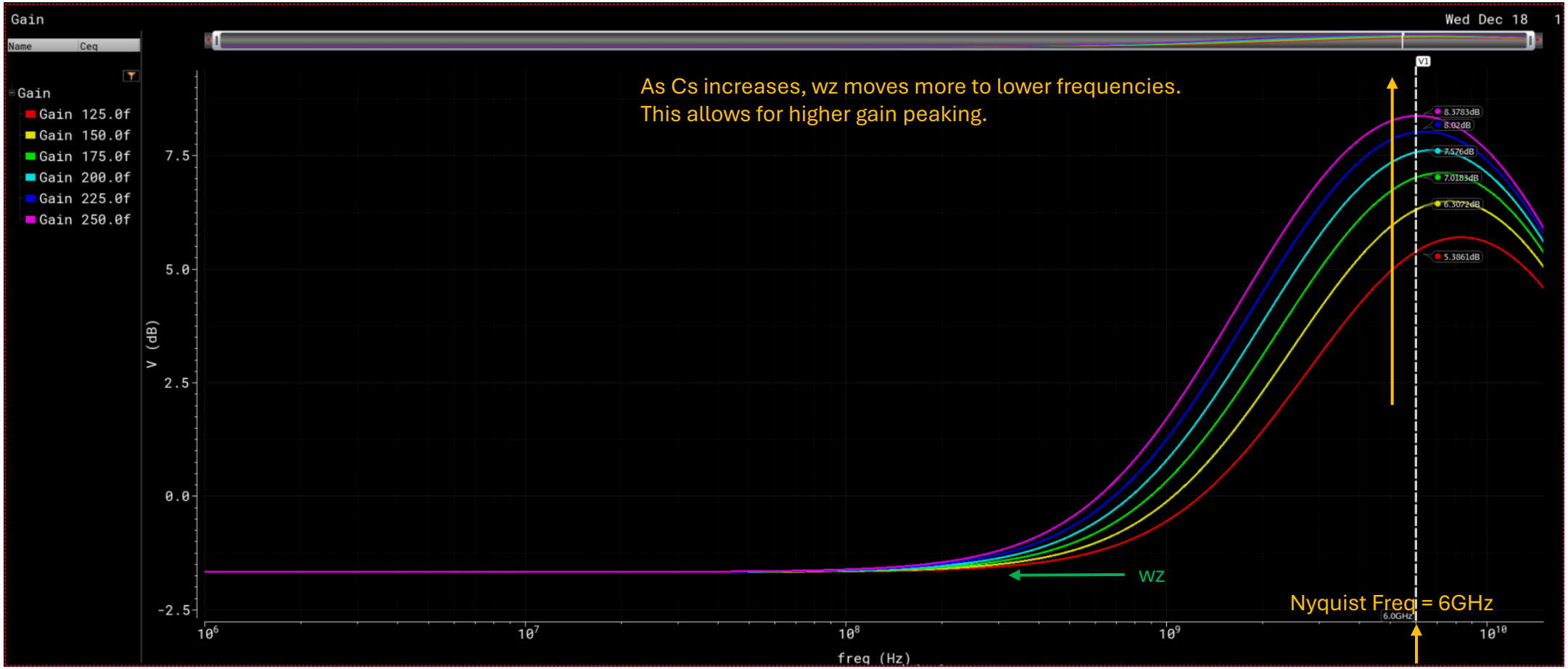
a) Sweeping Cp (Output loading Cap)



2) AC Analysis:

Results - Sweeps

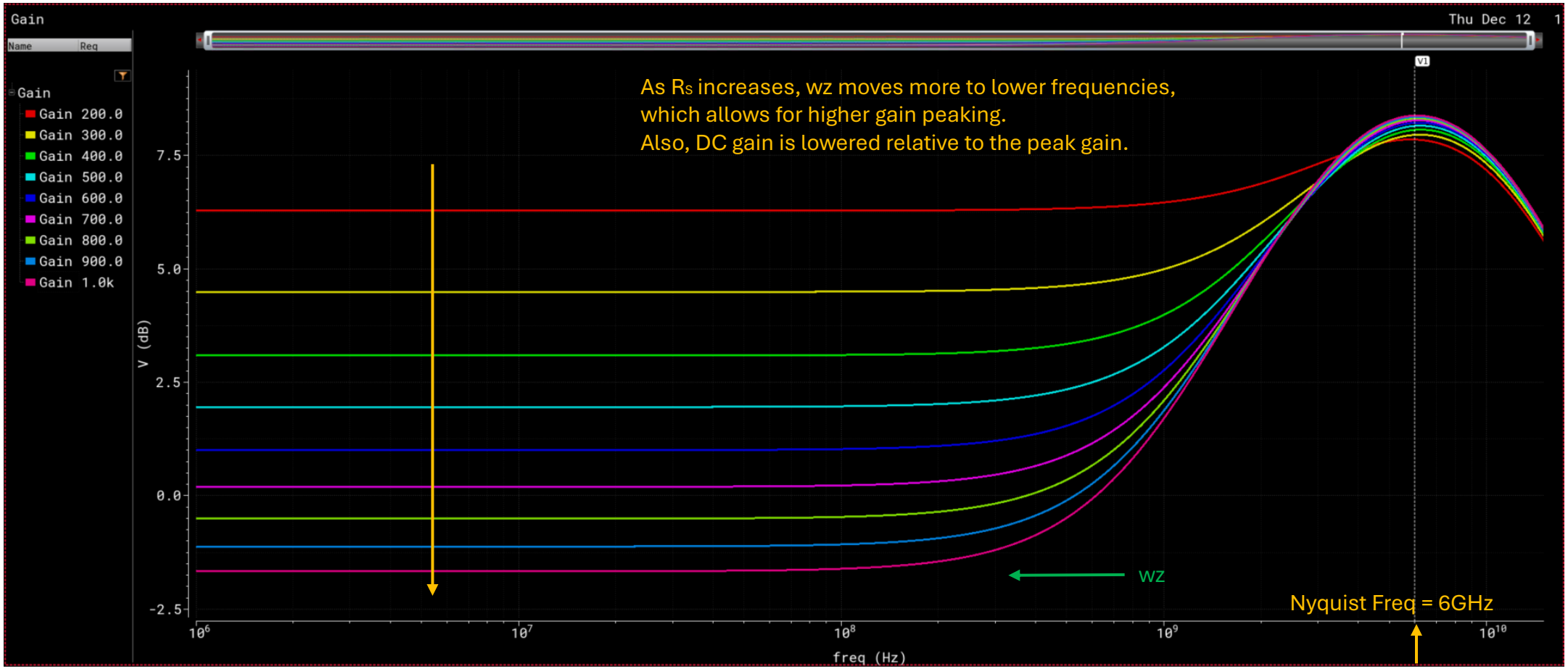
b) Sweeping Cs (Equalization Cap)



2) AC Analysis:

Results - Sweeps

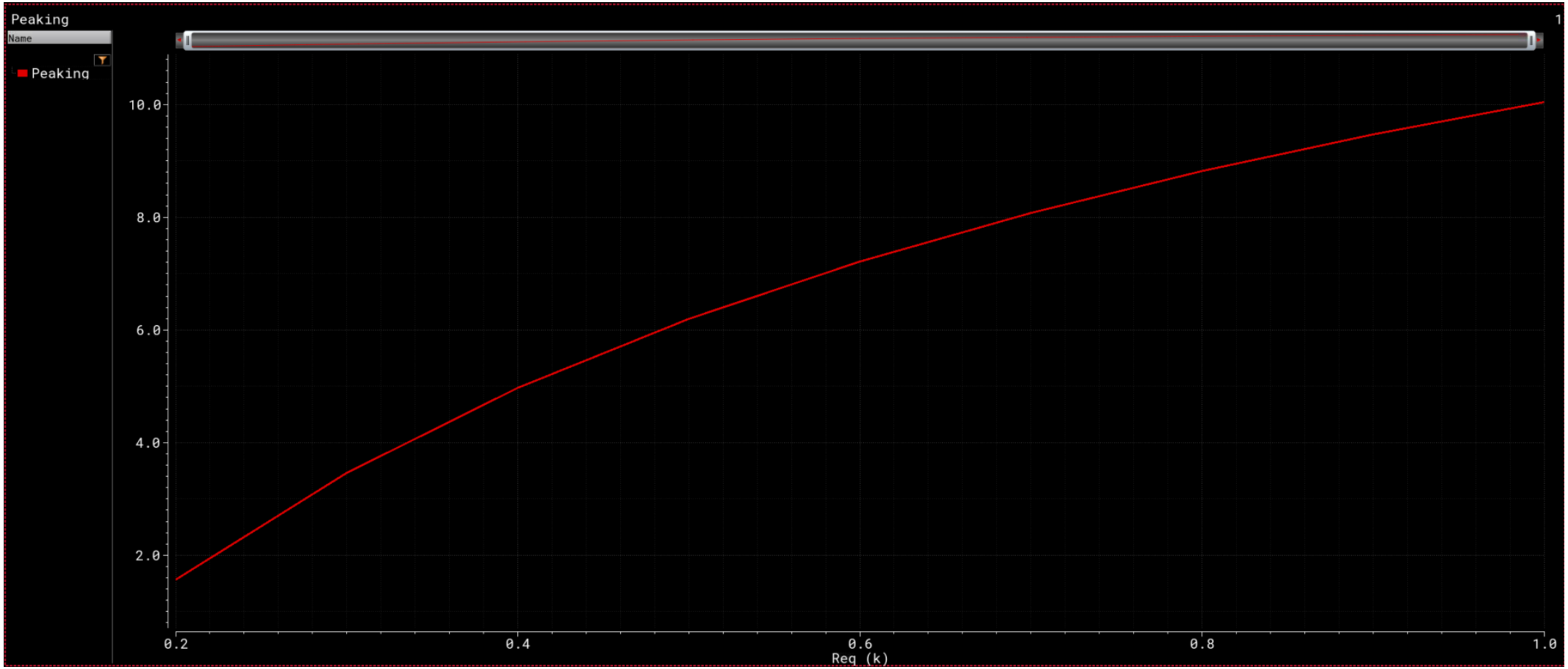
c) Sweeping R_S (Equalization Resistance)



2) AC Analysis:

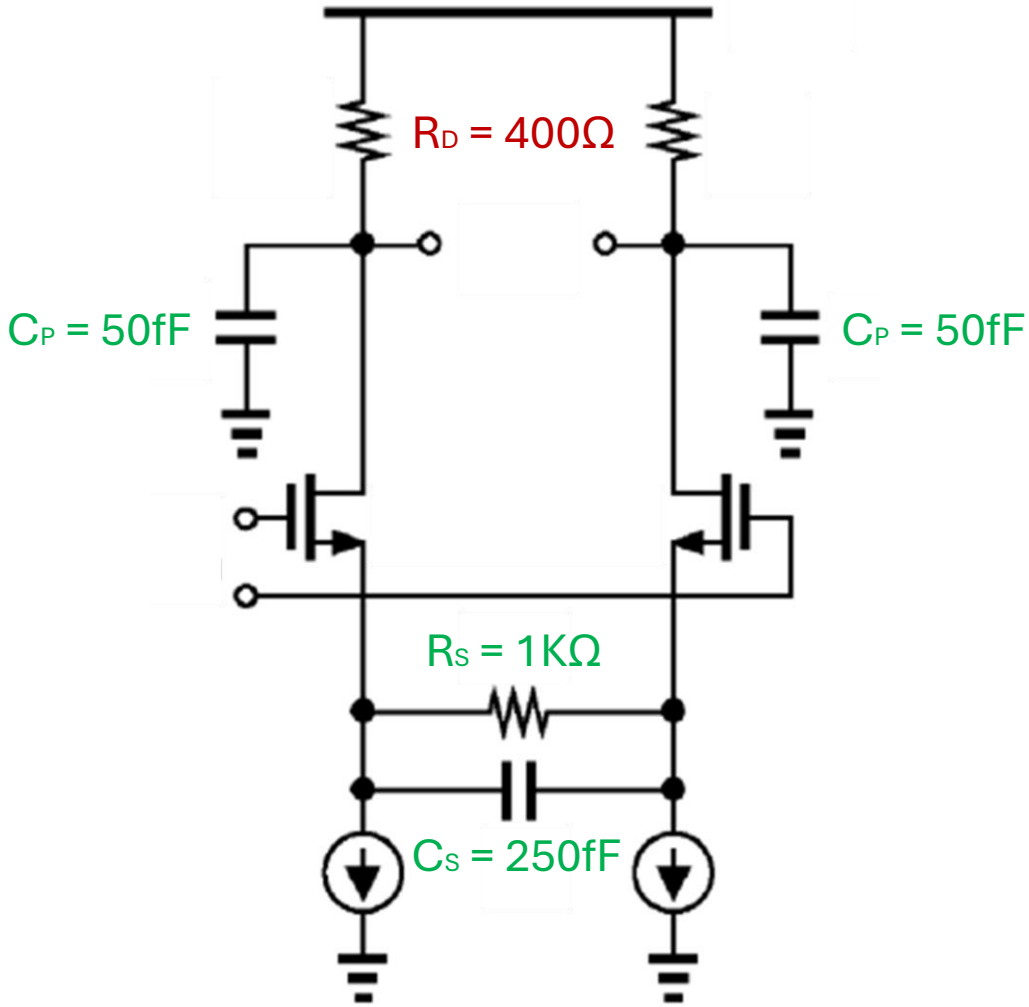
Results - Sweeps

c) Sweeping R_S (Equalization Resistance)



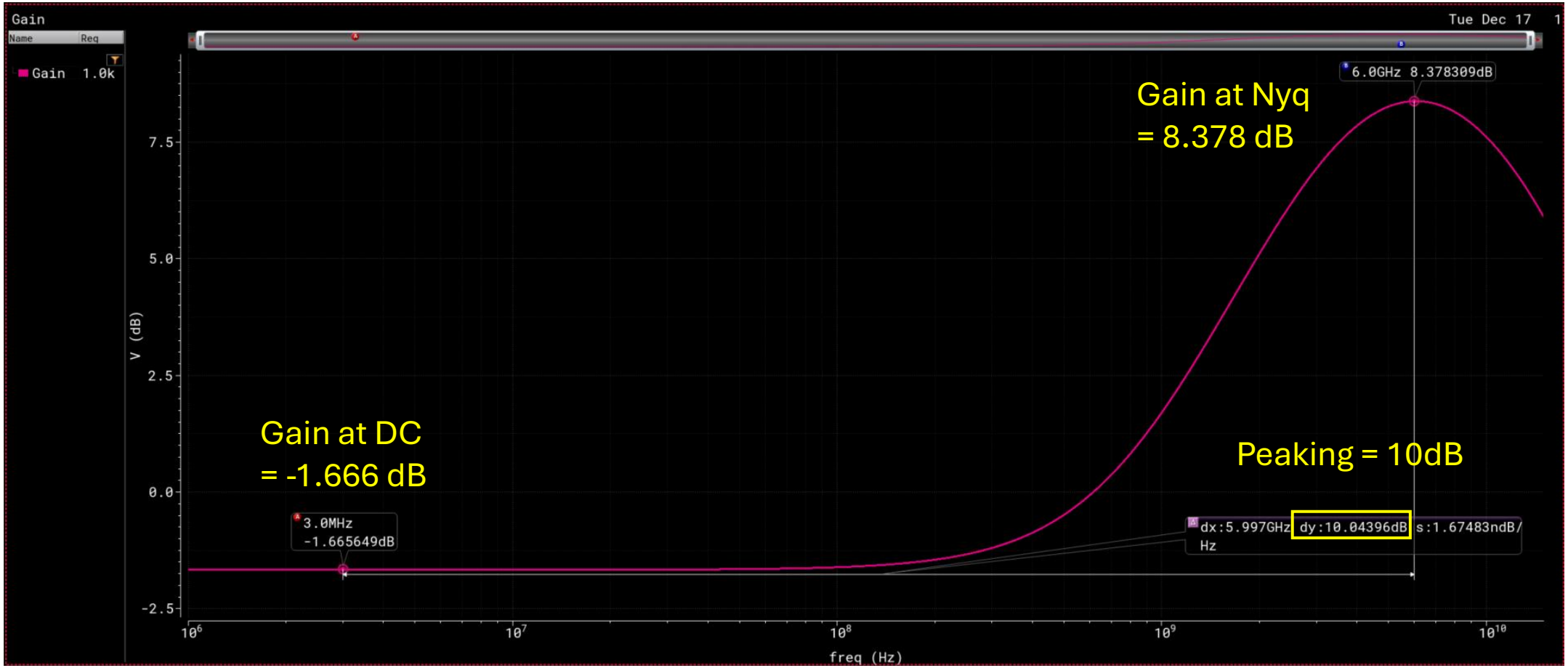
2) AC Analysis:

Results



2) AC Analysis:

Results

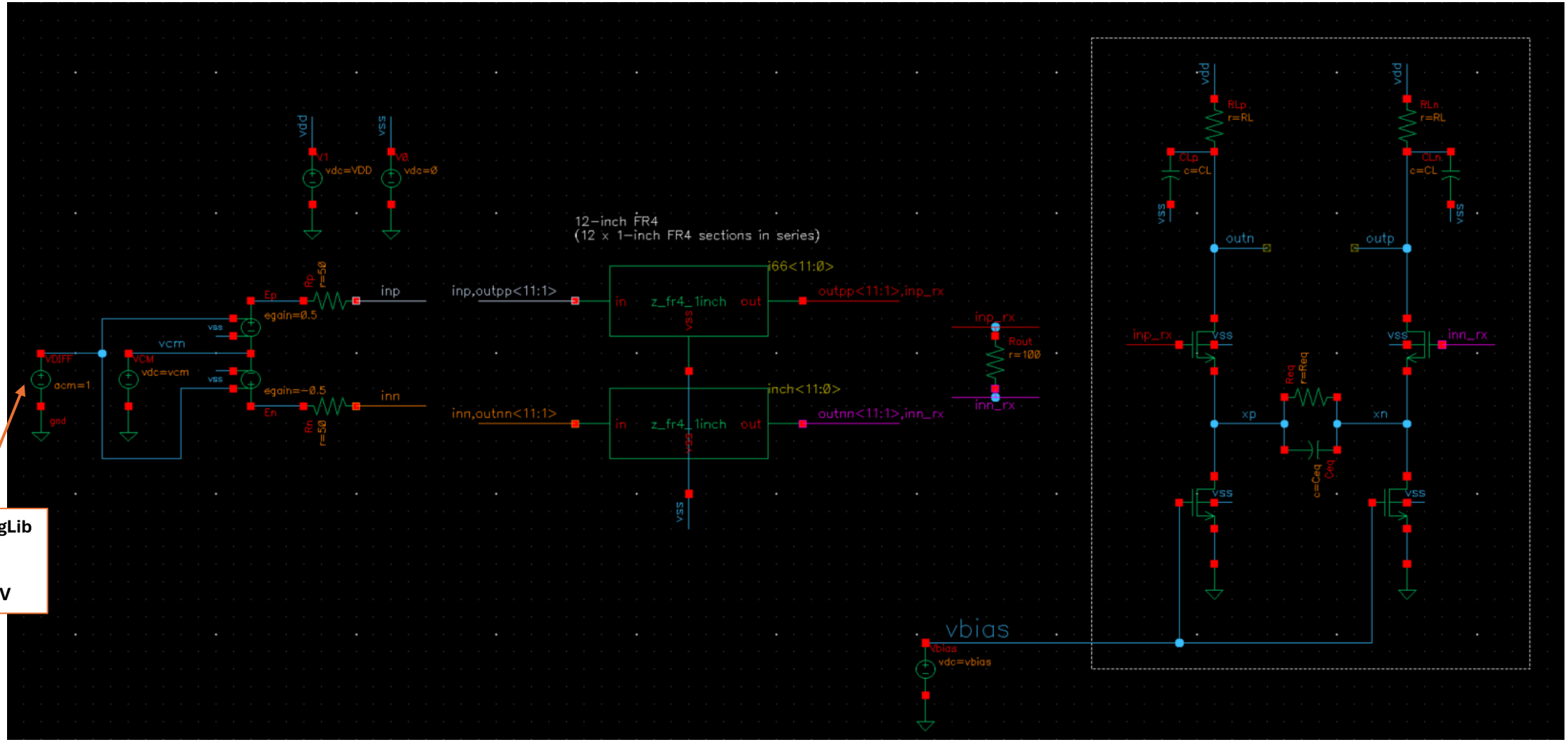


c) CTLE + Channel

1) AC Analysis:

Testbench

➔ For Frequency Response

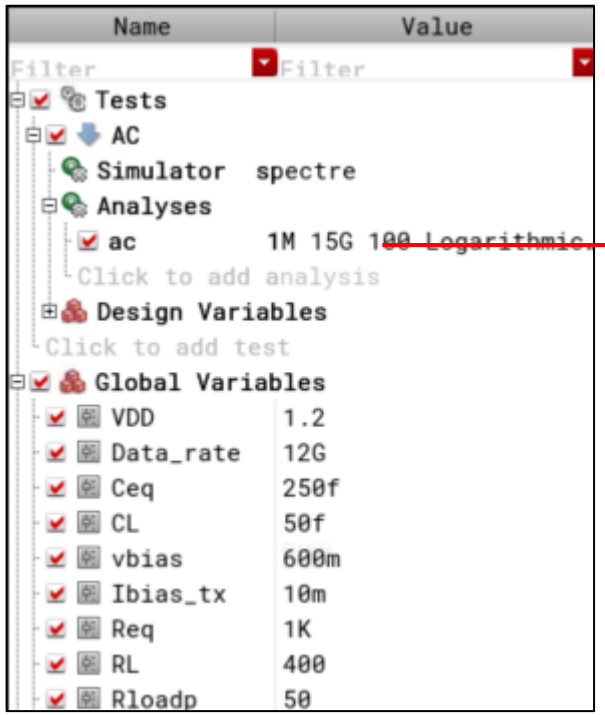


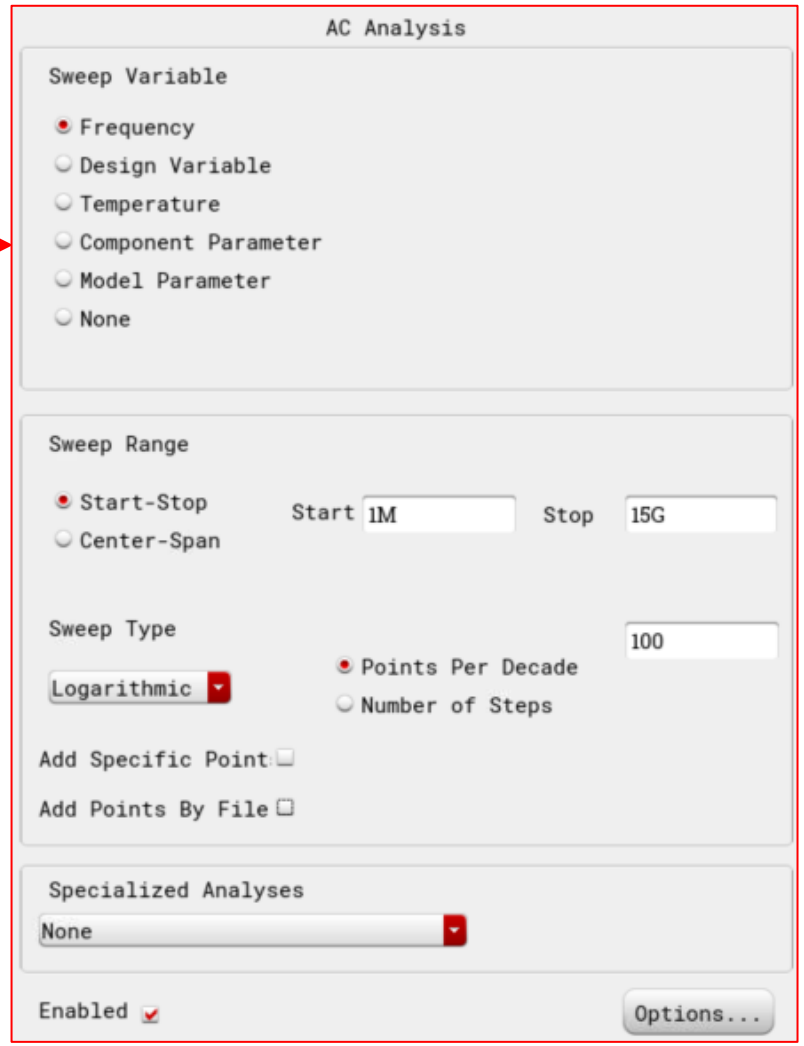
LIB: **analogLib**
CELL: **vdc**

AC Mag: **1 V**

1) AC Analysis:

Setup





1) AC Analysis:

Measurements

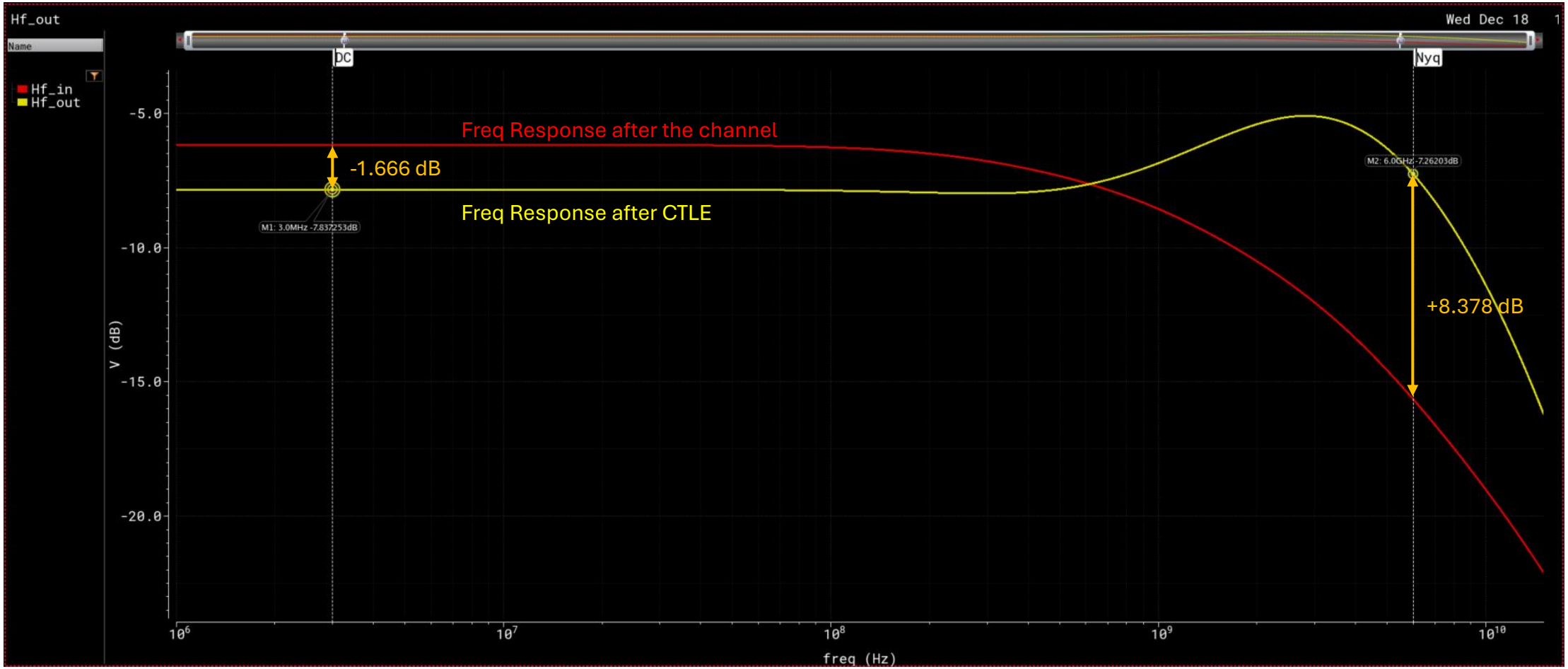
Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Hf_in	expr	dB20((VF("/inp_rx") - VF("/inn_rx")))	point
Hf_out	expr	dB20((VF("/outp") - VF("/outn")))	point
Hf_at_DC	expr	value(Hf_out 0)	point
Hf_at_Nyq	expr	value(Hf_out (VAR("Data_rate") / 2))	point
Peaking	expr	(Hf_at_Nyq - Hf_at_DC)	point

HF_in = Freq Response after the channel
HF_out = Freq Response after CTLE

Peaking = Gain Peaking @ Nyquist after CTLE

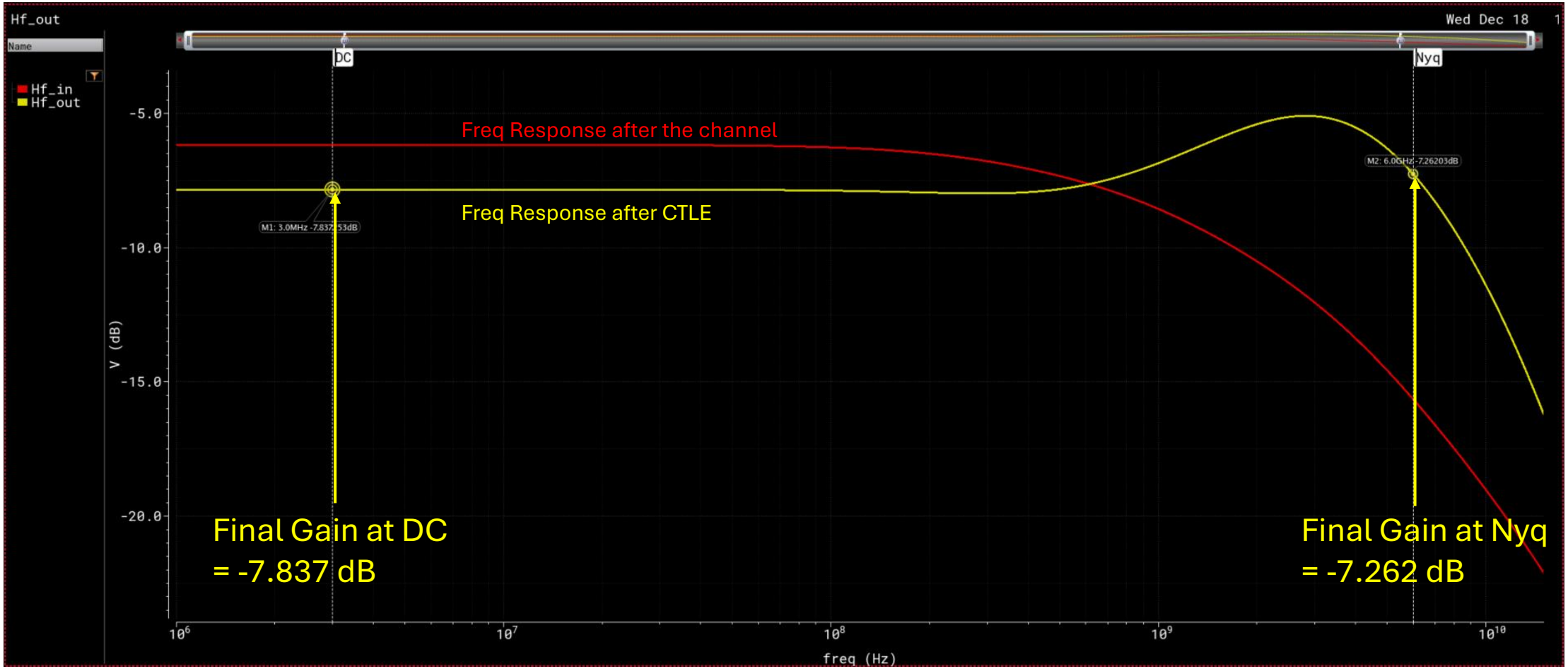
1) AC Analysis:

Results



1) AC Analysis:

Results

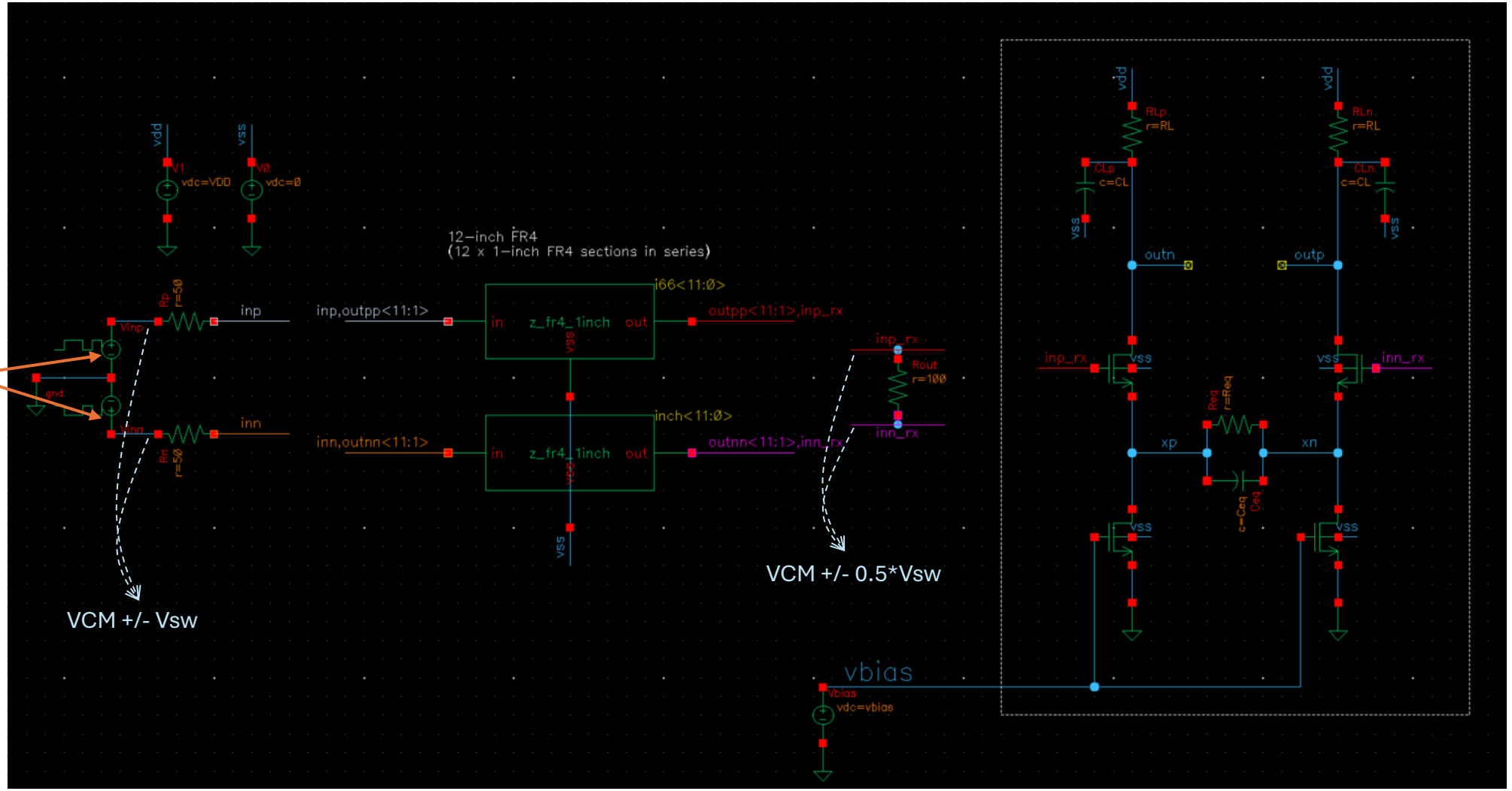


2) Transient Analysis: Testbench

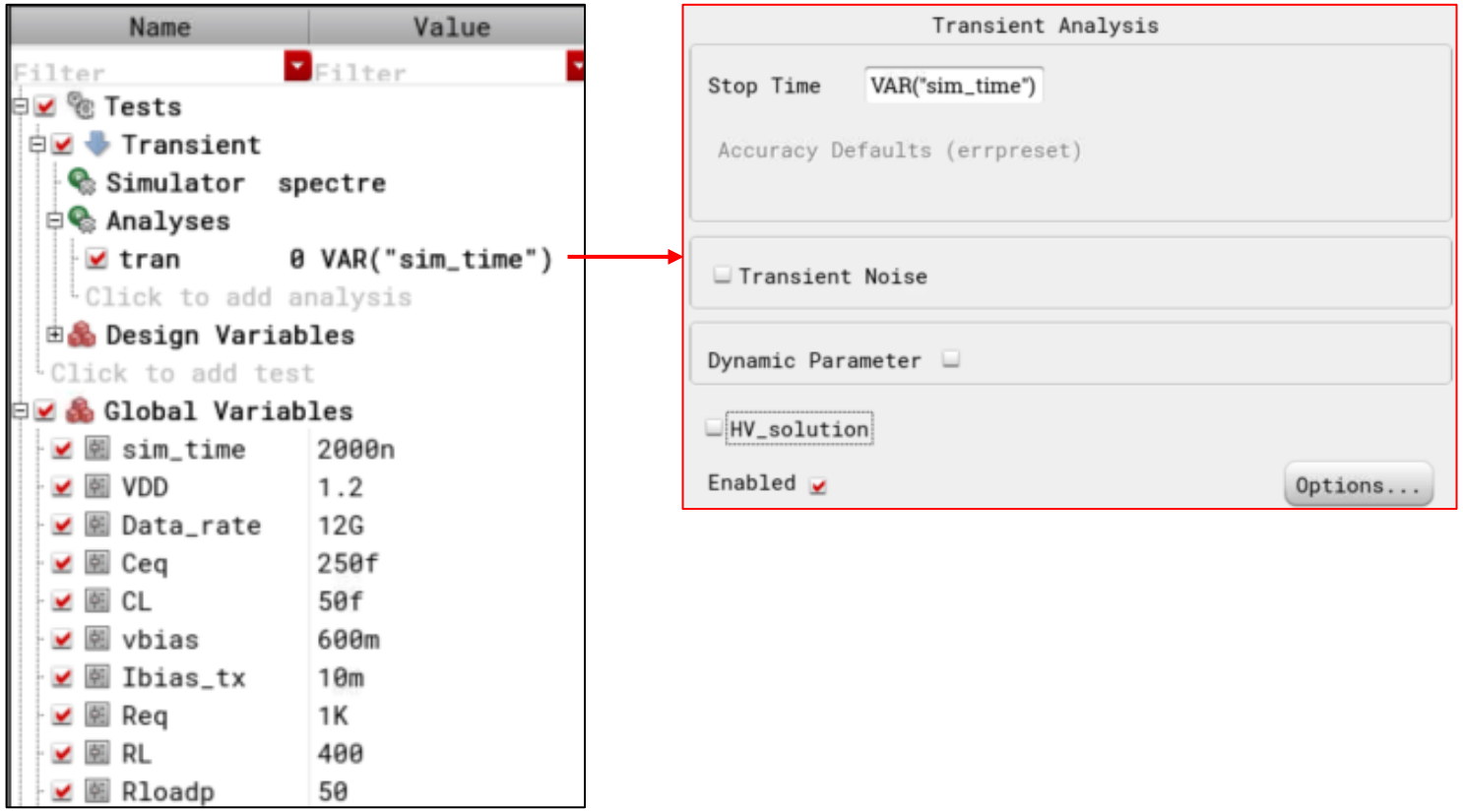
➔ For Eye Diagrams

LIB: **analogLib**
CELL: **vprbs**

Zero value: **vcm +/- 0.5**
One value: **vcm -/+ 0.5**
Bit period: **83.33ps (1/12G)**
Rise/Fall times: **10 ps**
Edge type: **linear**
Trigger: **Internal**
LFSR Mode: **PN32**



2) Transient Analysis: Setup



2) Transient Analysis:

Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
	signal	/vcm	point
	signal	/inp	point
	signal	/inn	point
	signal	/inp_rx	point
	signal	/inn_rx	point
	signal	/outp	point
	signal	/outn	point
*** PK2PK ***	expr		point
Vchin_pk2pk	expr	(VT("/inp") - VT("/inn"))	point
Vchout_pk2pk	expr	(VT("/inp_rx") - VT("/inn_rx"))	point
Vctleout_pk2pk	expr	(VT("/outp") - VT("/outn"))	point
*** EYE ***	expr		point
EYE_ch_out	expr	eyeDiagram(Vchout_pk2pk 1e-08 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
EYE_ctle_out	expr	eyeDiagram(Vctleout_pk2pk 1e-08 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point

Eye Diagram at CTLE input

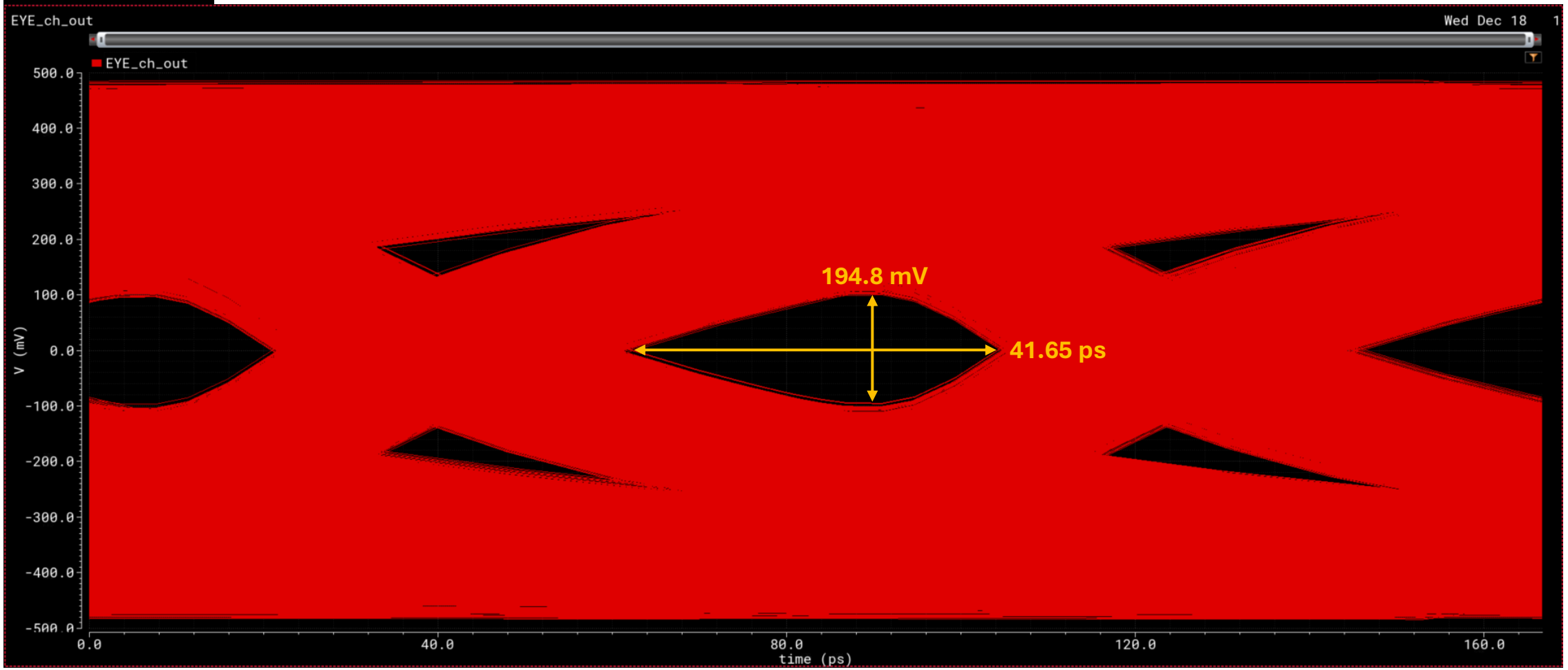
Eye Diagram at CTLE output

2) Transient Analysis:

Eye Diagram

Before CTLE

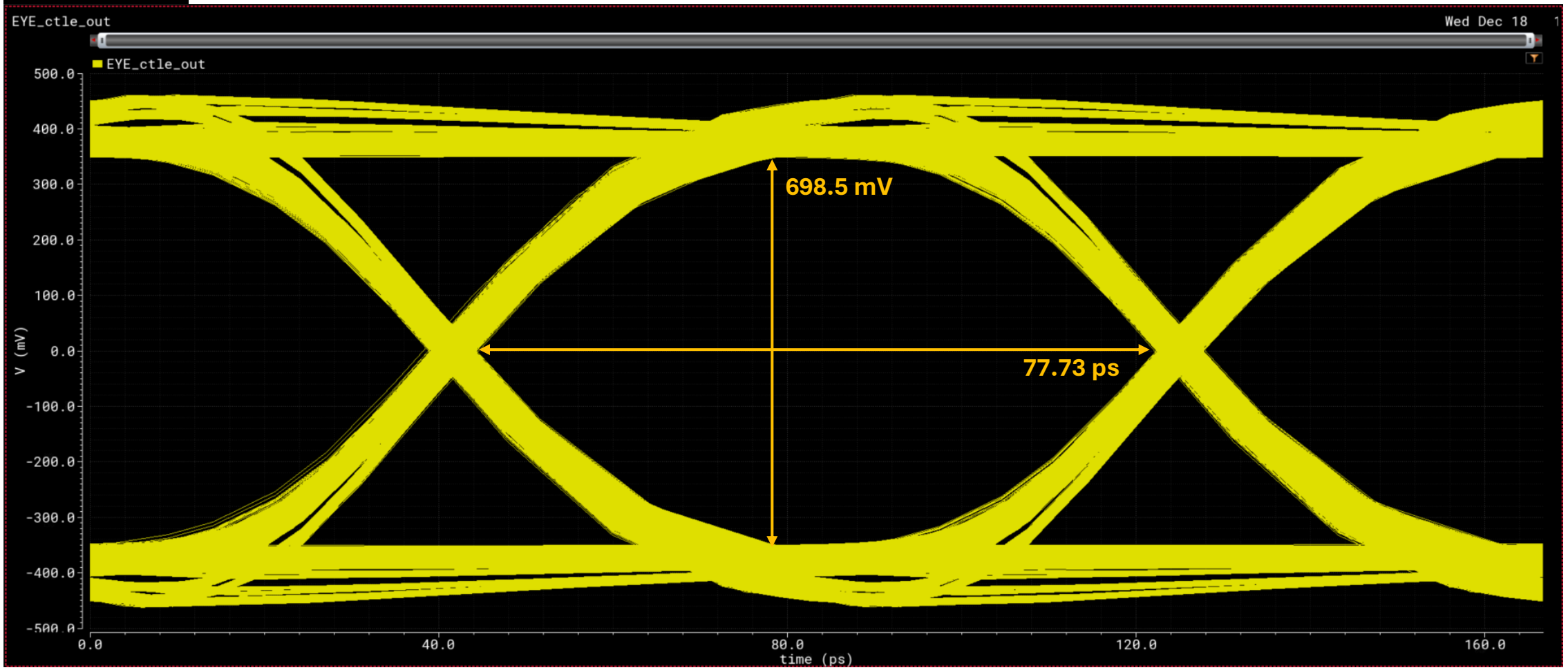
Eye SNR = 2.51dB



2) Transient Analysis:
Eye Diagram

After CTLE

Eye SNR = 14.08dB



2) Transient Analysis:

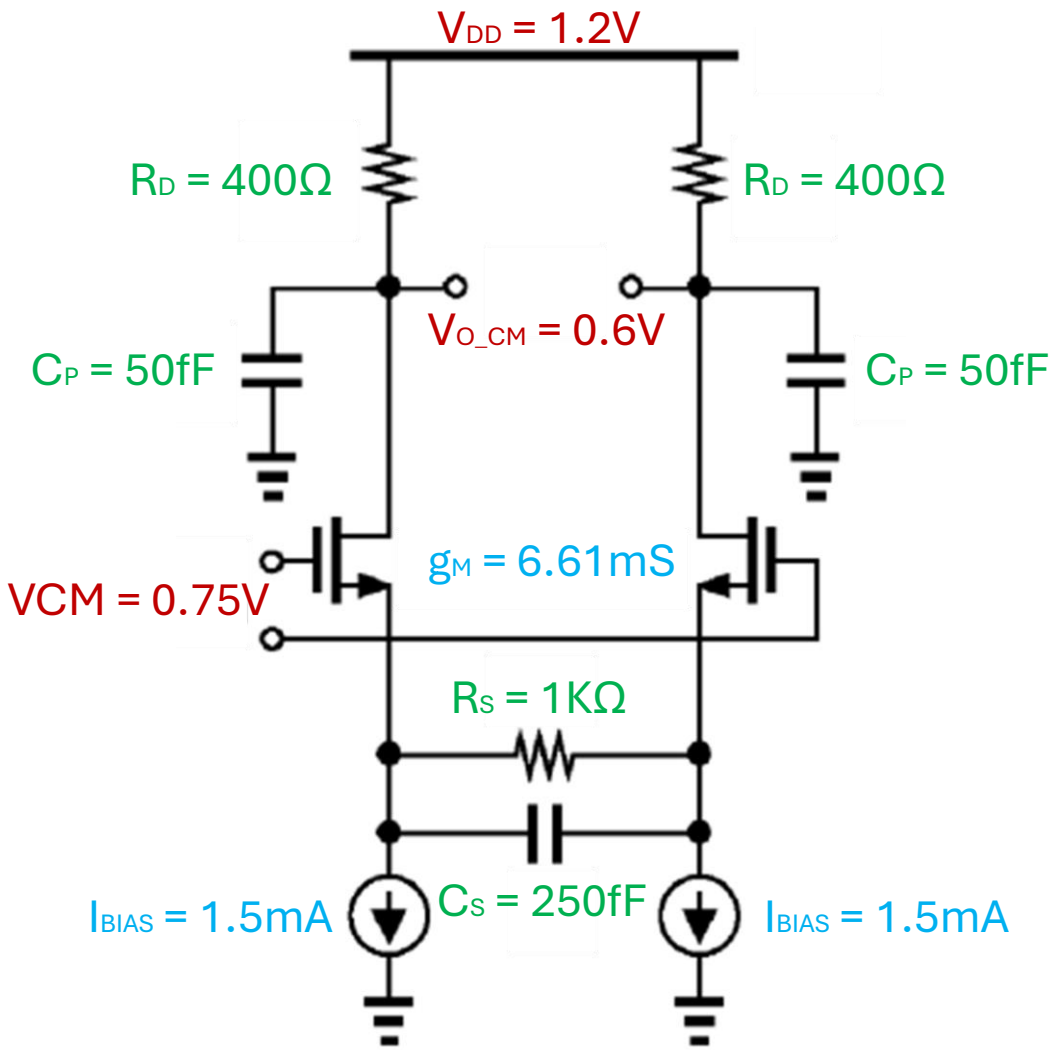
Eye Diagram

Summary

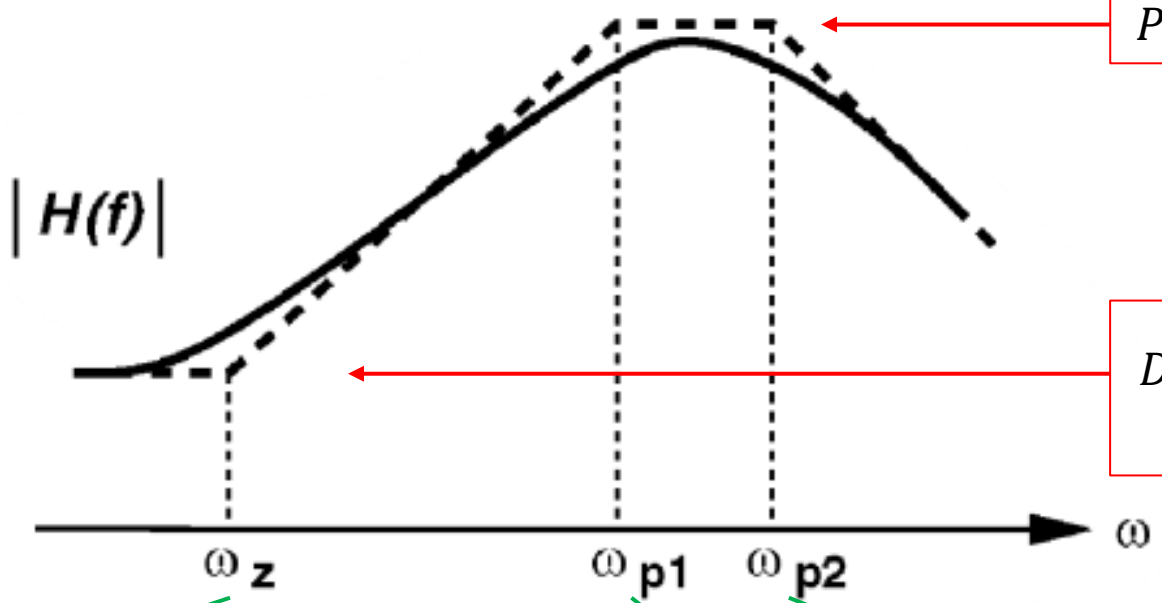
Design Parameters

Parameter	Value
Data Rate	12 Gb/s
VDD (for CTLE)	1.2 V
Input $V_{SWING\ (PK2PK)}$	0.5 V
Input V_{CM}	0.75 V
Channel	12-inch FR4
Output V_{CM}	0.6 V

Design Parameters



Poles/Zero/Gains (calculated based on previous values)



$$Peak\ Gain = 20\log(g_m.R_D) = 8.445\ dB$$

$$DC\ Gain = 20\log\left(\frac{g_m.R_D}{1+g_m.\frac{R_S}{2}}\right) = -4.23\ dB$$

$$f_Z = \frac{1}{2\pi.R_S.C_S} = 636.62\ MHz$$

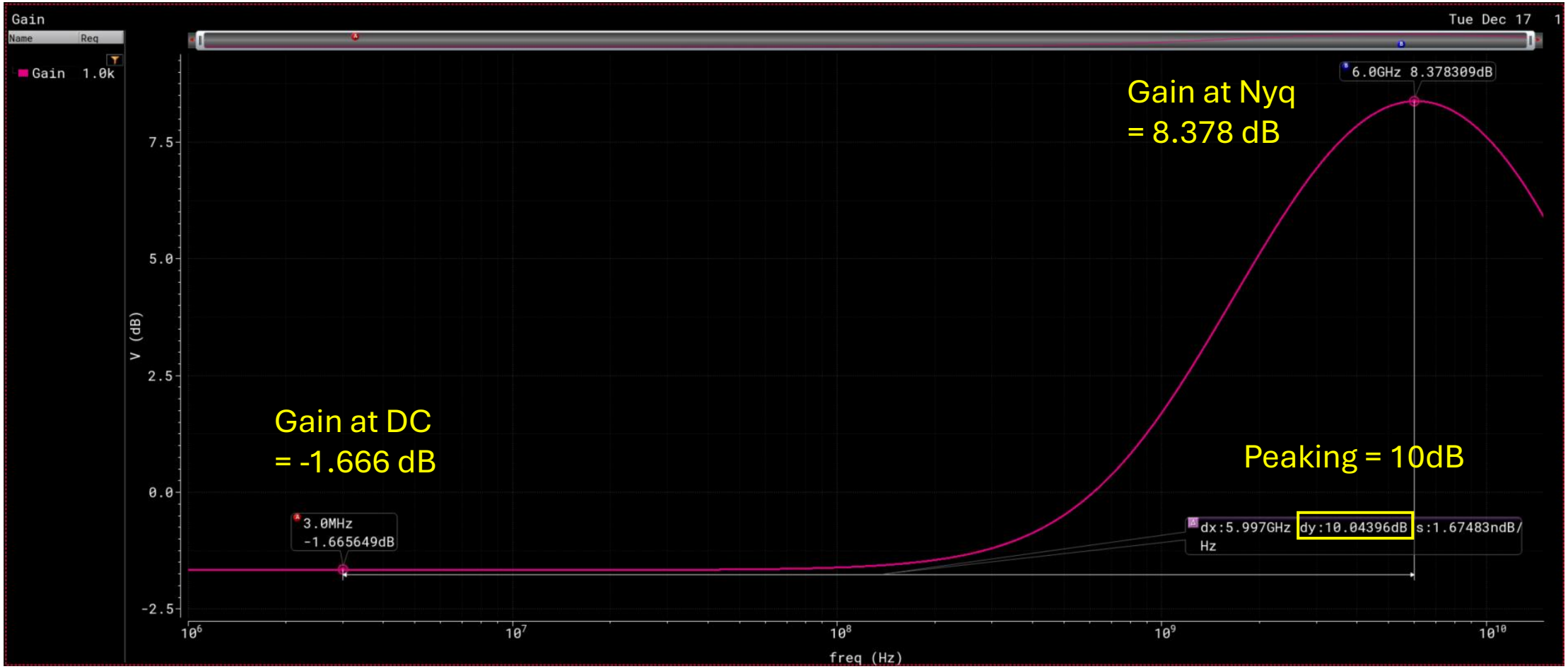
$$f_{P1} = \frac{1+g_m.\frac{R_S}{2}}{2\pi.R_S.C_S} = 2.74\ GHz$$

$$f_{P2} = \frac{1}{2\pi.R_D.C_P} = 8\ GHz$$

$$Peaking = 20\log\left(1+g_m.\frac{R_S}{2}\right) = 12.68\ dB$$

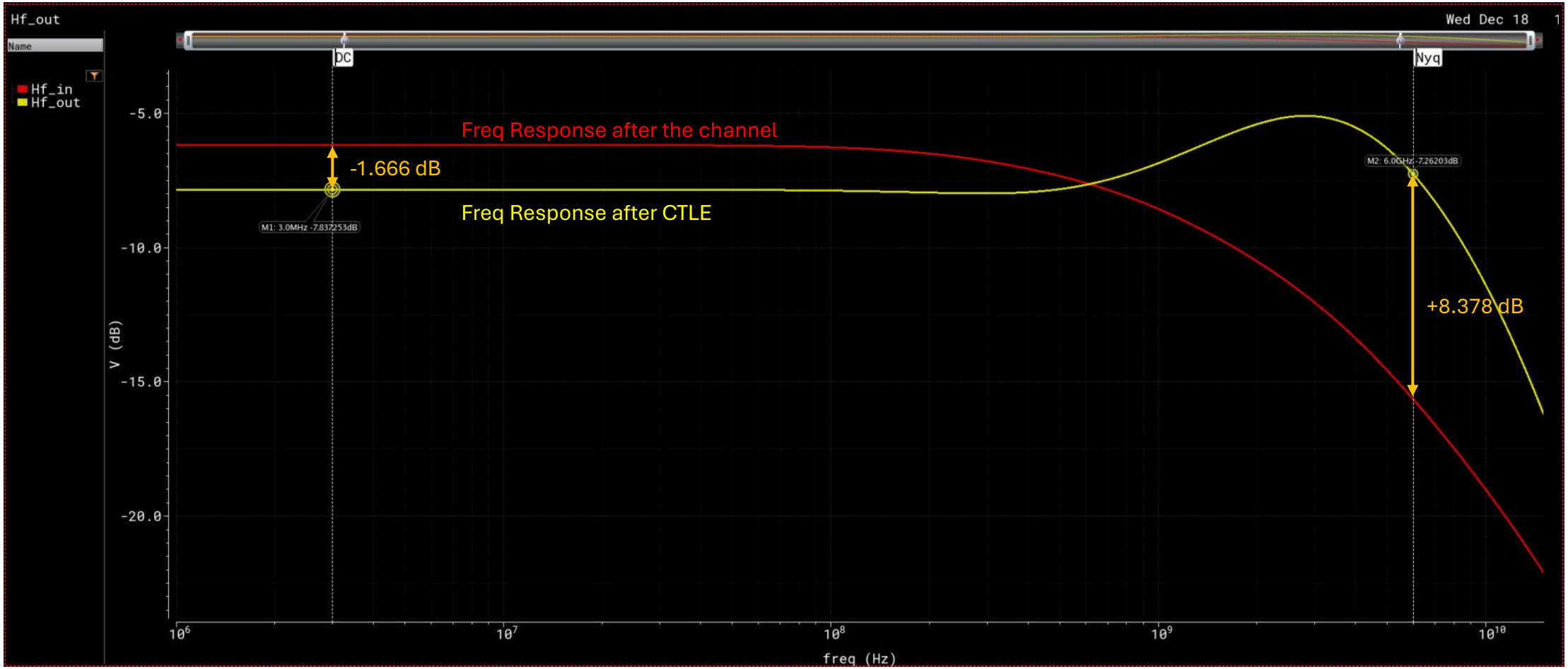
Final Results

➔ Frequency Response of CTLE: (Simulated Values)



Final Results

➔ Frequency Response of Channel + CTLE:



Final Results

➔ Eye Diagrams:

Final Results

➔ Eye Diagram Comparison:

	Before CTLE (After Channel)	After CTLE
Eye Height (Max)	**194.8 mV**	**698.5 mV**
Eye Width (Max)	**41.65 ps**	**77.73 ps**
Eye SNR	**2.51 dB**	**14.08 dB**

Conclusion

- This project shows the design procedure & the testbench setup details used for the design of an Active RX CTLE Equalizer for a 12 Gb/s NRZ input & a channel of 12-inch FR4.