

Rx Active CTLE

12 Gbps

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Outline

1. Design & Equations

2. Tests & Simulations

a) Channel:

- i. Frequency response

b) CTLE only:

- i. DC Analysis (→ gm)
- ii. AC Analysis (→ Gain Peaking)

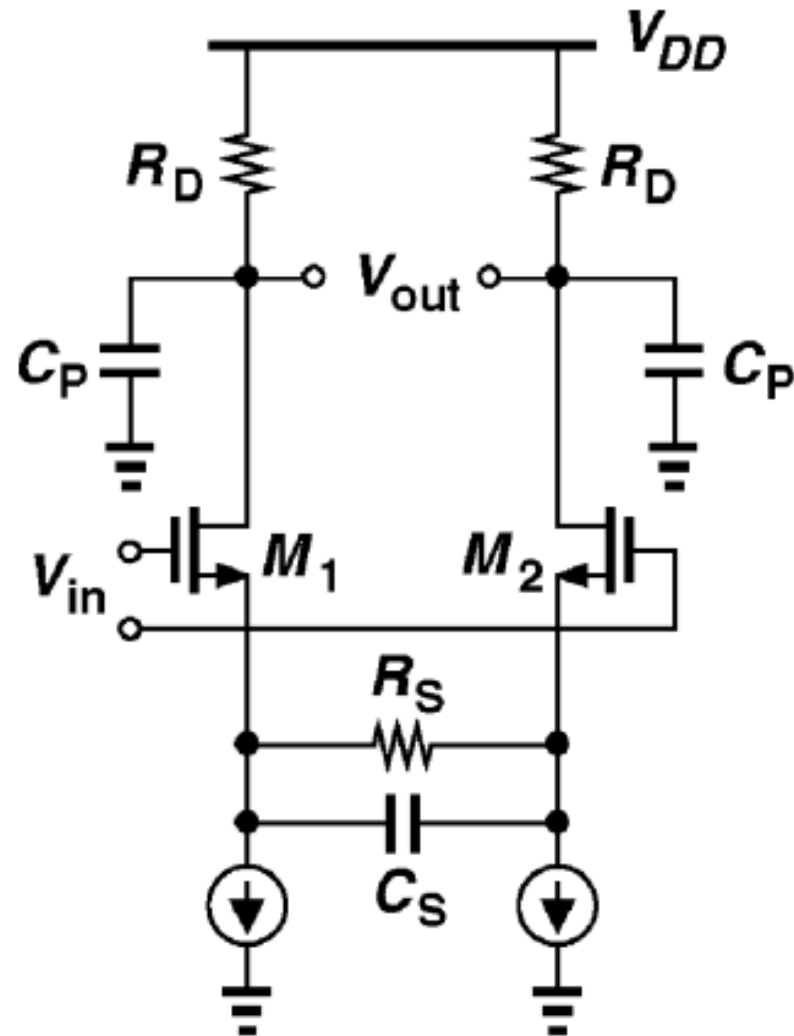
c) CTLE + Channel:

- i. AC Analysis (→ Frequency Response)
- ii. Transient Analysis (→ Eye Diagram)

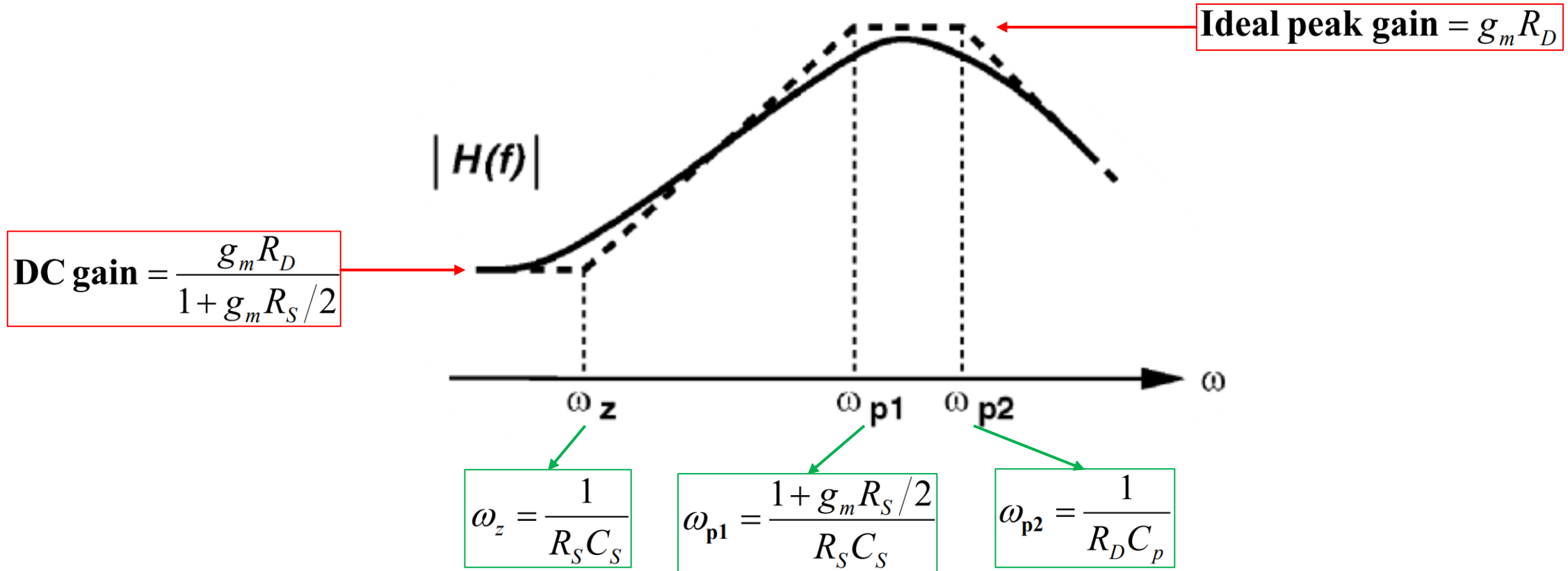
3. Summary & Conclusion

Design Topology & Equations

Active CTLE



Active CTLE



$$\text{Ideal Peaking} = \frac{\text{Ideal peak gain}}{\text{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_S / 2$$

Tests & Simulations

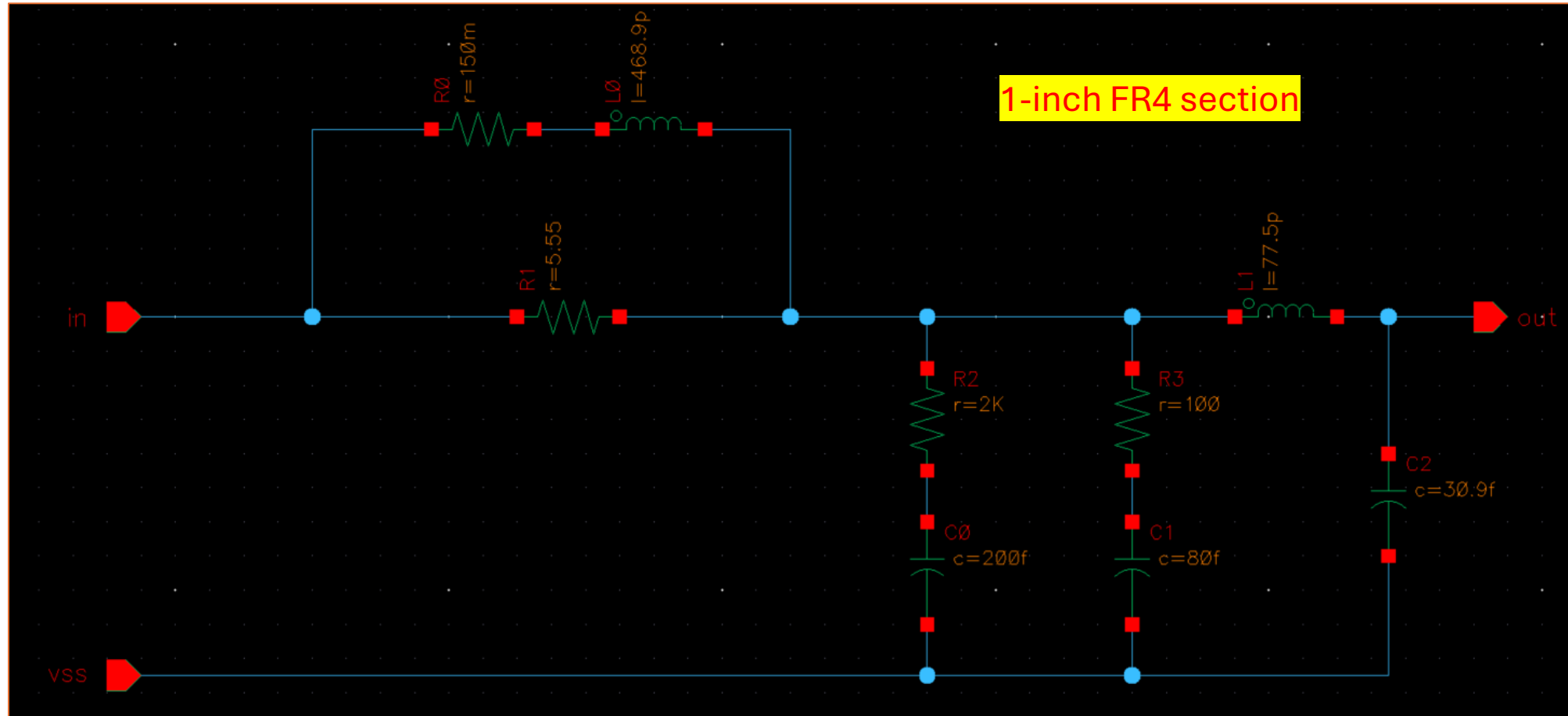
Design Parameters

Parameter	Value
Data Rate	12 Gb/s
VDD (for CTLE)	1.2 V
Input $V_{\text{SWING (PK2PK)}}$	0.5 V
Input V_{CM}	0.75 V
Channel	12-inch FR4
Output V_{CM}	0.6 V

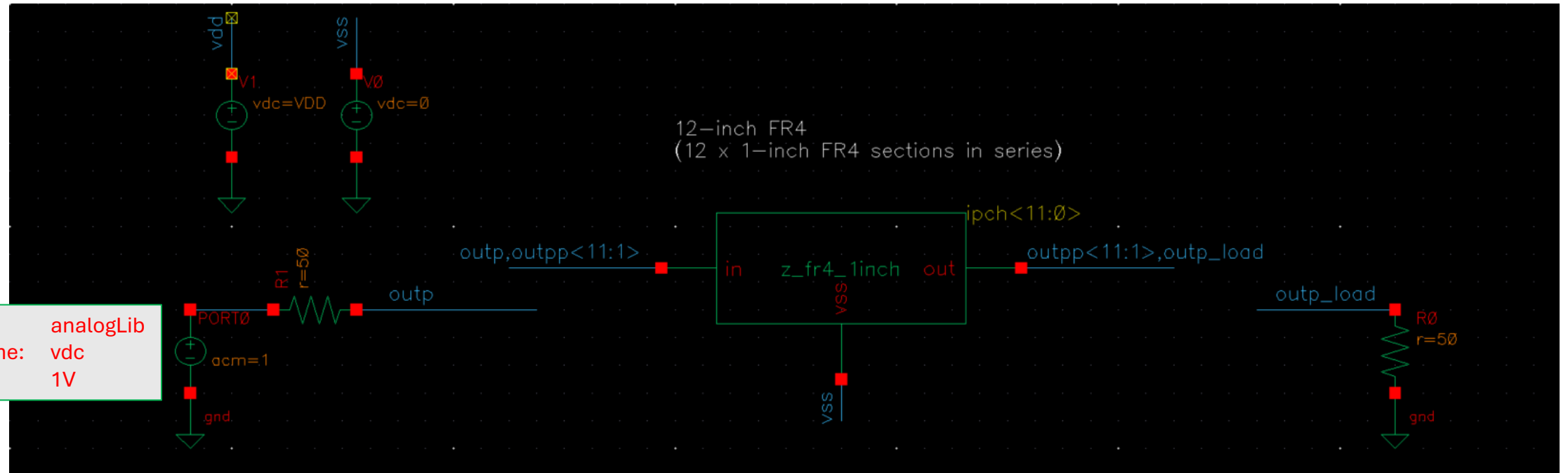
a) Channel

The frequency response can be found by 2 methods:
Single-ended or Differential

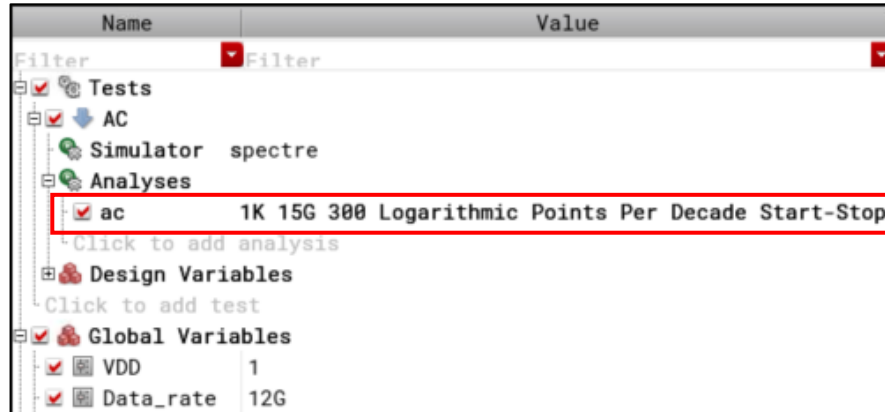
Channel = 12 x 1-inch FR4 section



1) Single-Ended: Testbench



1) Single-Ended: Setup



AC Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop Start 1K Stop 15G

☐ Center-Span

Sweep Type

☒ Points Per Decade 300

☐ Number of Steps

Add Specific Point ☐

Add Points By File ☐

Specialized Analyses

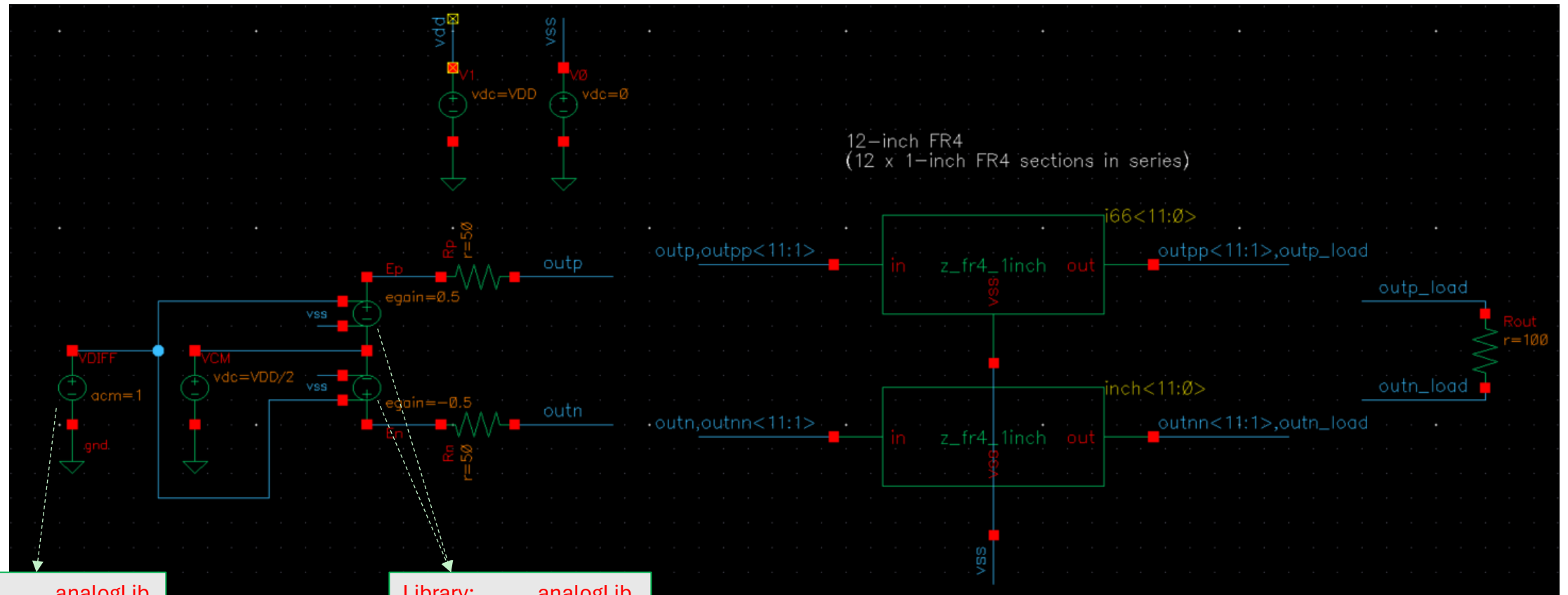
None

Enabled ☒ Options...

Measurements:

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Gain	expr	dB20(VF("/outp_load"))	point
Gain_at_Nyq	expr	value(Gain (VAR("Data_rate") / 2))	point

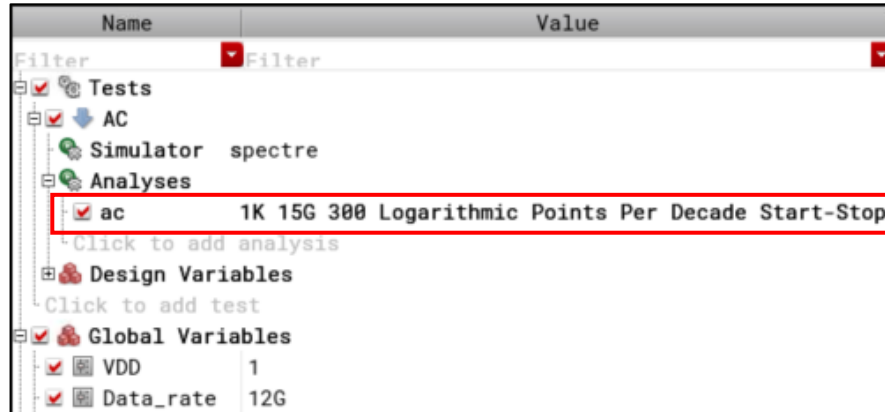
2) Differential: Testbench



Library: analogLib
Cell Name: vdc
AC mag: 1V

Library: analogLib
Cell Name: vcvs
Voltage Gain: +/- 0.5

2) Differential: Setup



AC Analysis

Sweep Variable

☒ Frequency
☐ Design Variable
☐ Temperature
☐ Component Parameter
☐ Model Parameter
☐ None

Sweep Range

☒ Start-Stop Start 1K Stop 15G
☐ Center-Span

Sweep Type

☒ Points Per Decade 300
☐ Number of Steps

Logarithmic

Add Specific Point ☐

Add Points By File ☐

Specialized Analyses

None

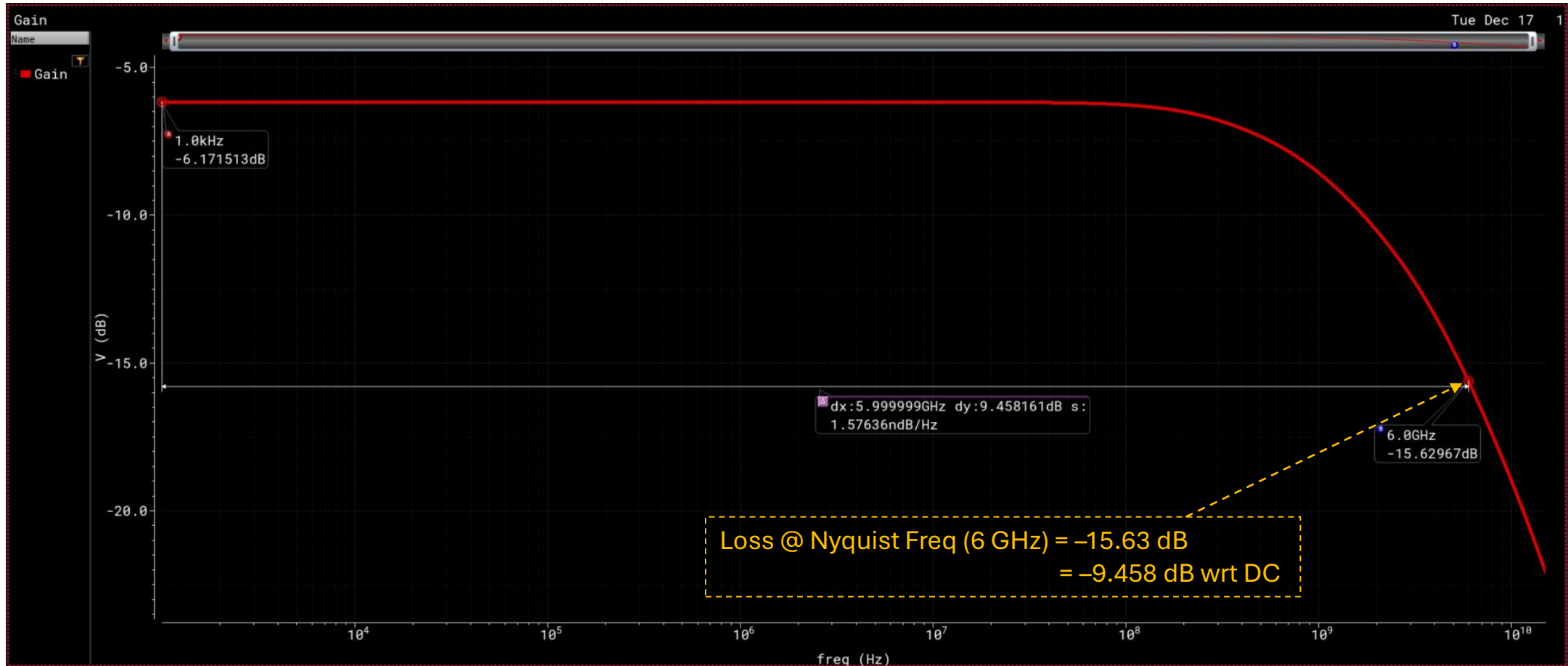
Enabled ☒

Options...

Measurements:

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Gain	expr	dB20((VF("/outp_load") - VF("/outn_load")))	point
Gain_at_Nyq	expr	value(Gain (VAR("Data_rate") / 2))	point
Gain_at_Nyq_wrt_dc	expr	(Gain_at_Nyq - value(Gain 0))	point

Channel's Frequency Response

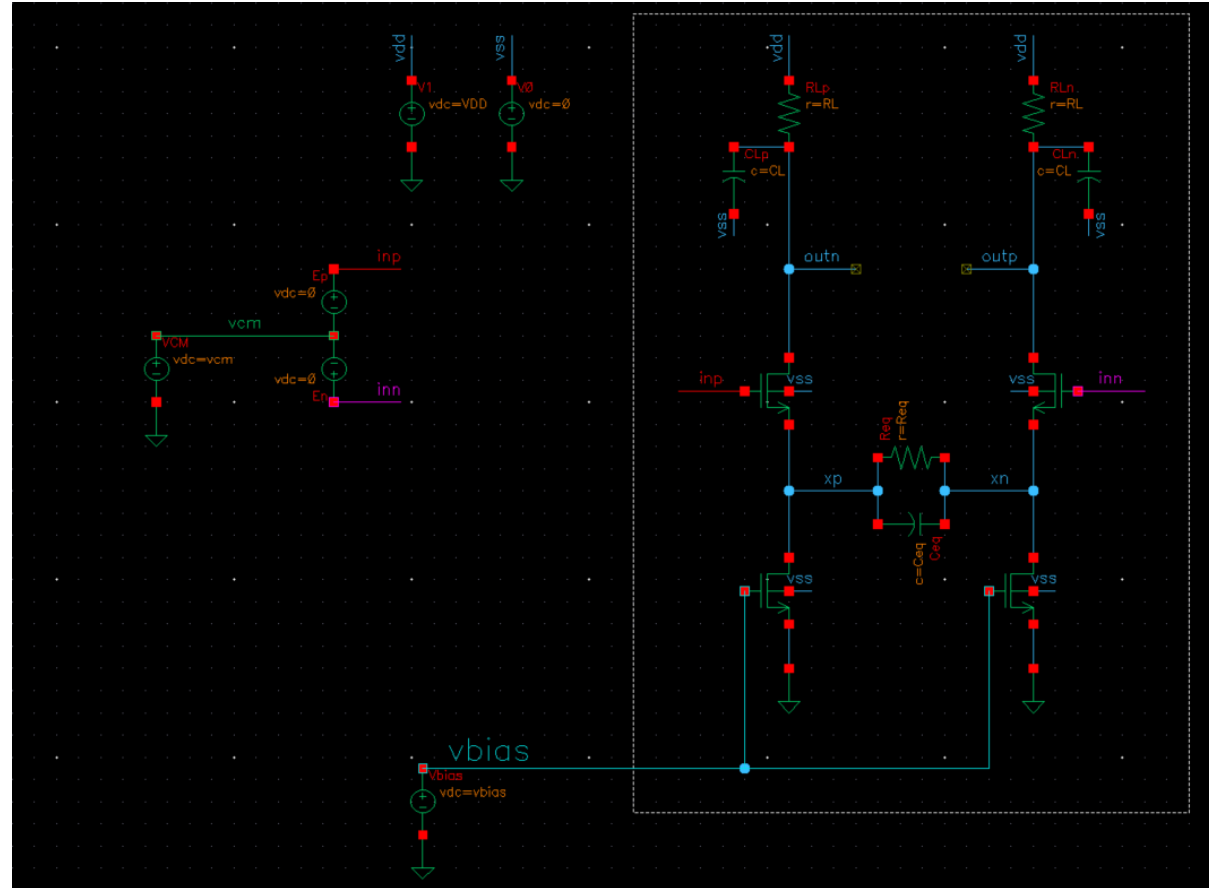


b) CTLE

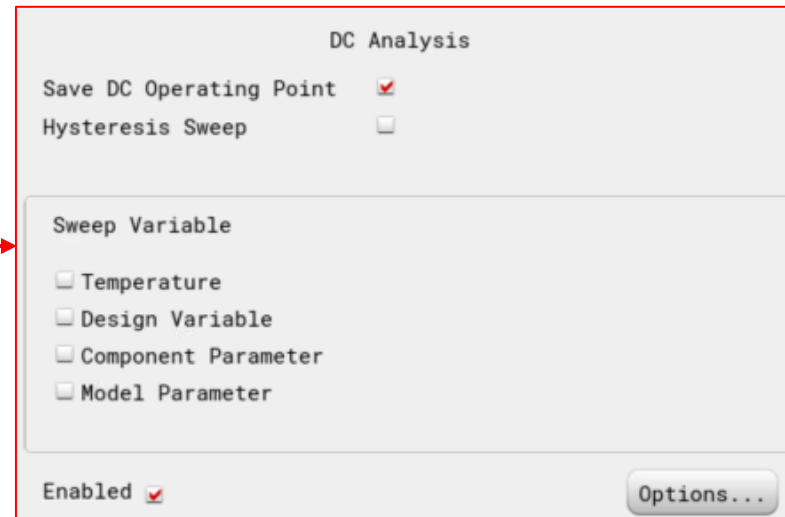
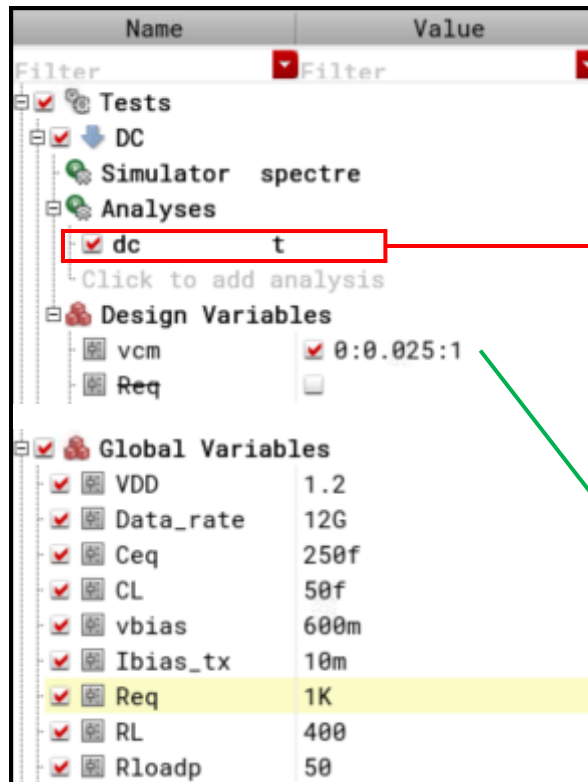
1) DC Analysis:

Testbench

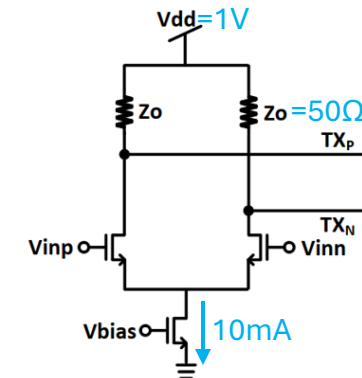
→ We use the DC Analysis to design for the required gm, output DC level, & current consumption.



1) DC Analysis: Setup



- The input CM voltage is swept to see how gm changes.
- The input CM voltage comes from the output CM voltage of the TX driver.
(Or a bypass Cap can be added to make input VCM of CTLE independent of TX)



$$\begin{aligned} V_{CM} &= V_{DD} - ((I_{bias}/2) * Z_o) \\ &= 1V - (5mA * 50\Omega) \\ &= 0.75V \end{aligned}$$

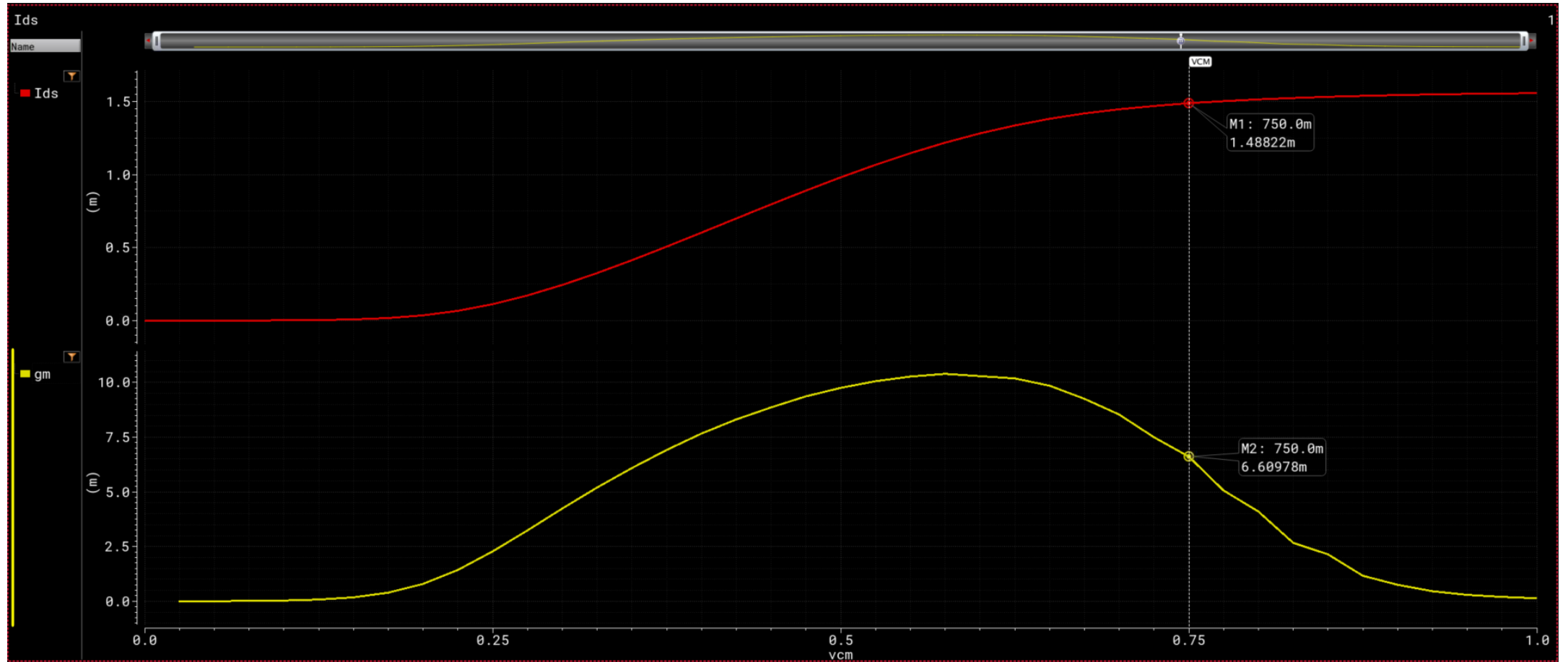
1) DC Analysis:

Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
VCM	expr	VDC("/vcm")	point
xp	expr	VDC("/xp")	point
xn	expr	VDC("/xn")	point
vbias	expr	VDC("/vbias")	point
outp	expr	VDC("/outp")	point
outn	expr	VDC("/outn")	point
I_branch	expr	IDC("/RLp/PLUS")	point
Vgs_in	expr	(VDC("/vcm") - VDC("/xp"))	point
Ids	expr	I_branch	sweeps
dIds	expr	deriv(I_branch)	sweeps
dVgs	expr	deriv(Vgs_in)	sweeps
gm	expr	(dIds / dVgs)	sweeps
gm_vcm	expr	value(gm 0.75)	sweeps
Out_vcm	expr	value(outp 0.75)	sweeps
Ids_vcm	expr	value(Ids 0.75)	sweeps

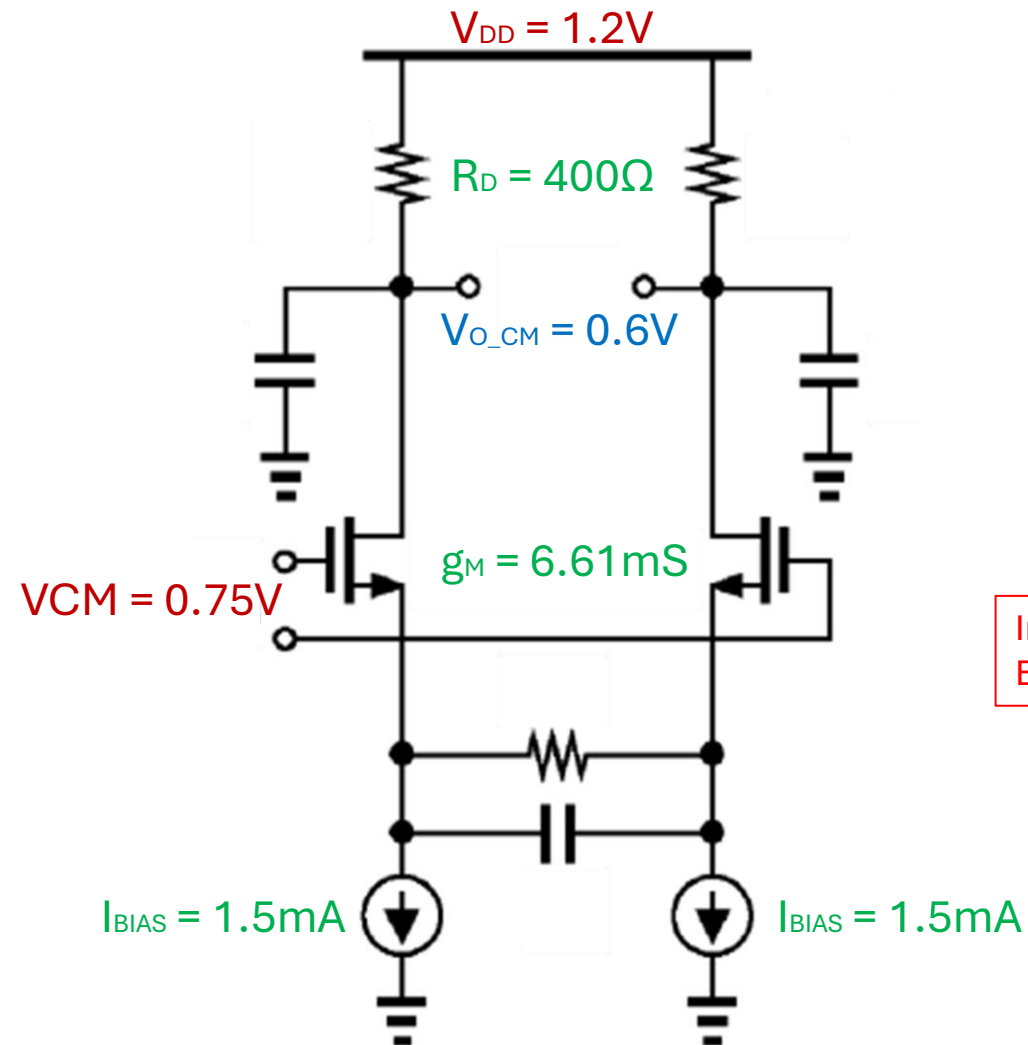
$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{\left(\frac{dI_{DS}}{dV_{CM}}\right)}{\left(\frac{dV_{GS}}{dV_{CM}}\right)}$$

1) DC Analysis: Results



1) DC Analysis:

Results

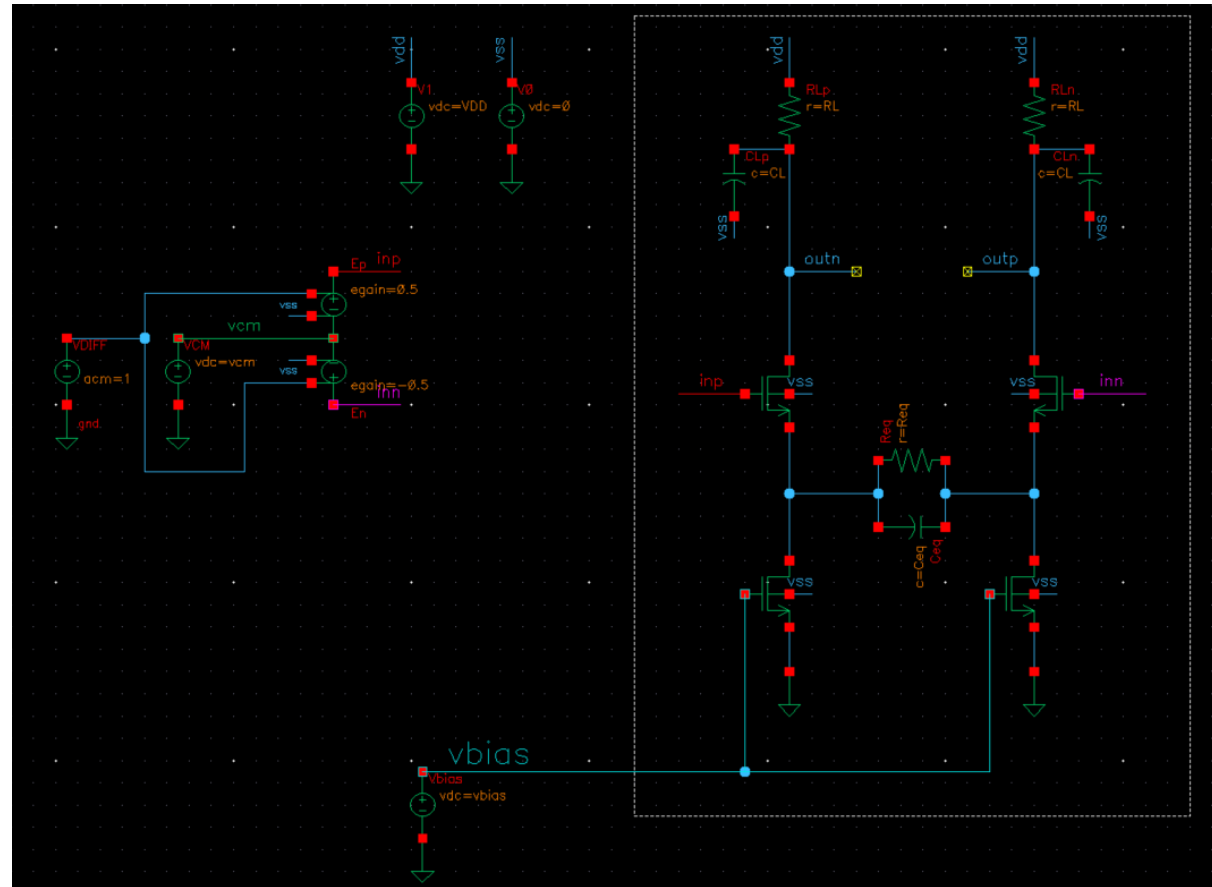


Input NMOS devices: $L = 2 * L_{MIN}$, $m=30x$
Bias NMOS devices: $L = 4 * L_{MIN}$, $m=16x$

2) AC Analysis:

Testbench

→ We use the AC Analysis to design for the required gain peaking, zero & pole frequencies.



2) AC Analysis: Setup

The image shows the LTSPICE simulation setup for an AC Analysis. On the left, the project tree displays the following structure:

- Tests
 - AC
 - Simulator: spectre
 - Analyses
 - ac: 1M 15G 100 Logarithmic
 - Design Variables
 - vcm: 0.75
 - Req: 200:100:1K
- Global Variables
 - VDD: 1.2
 - Data_rate: 12G
 - Ceq: 250f
 - CL: 50f
 - vbias: 600m
 - Ibias_tx: 10m
 - Req: 1K
 - RL: 400
 - Rloadp: 50

On the right, the 'AC Analysis' configuration dialog is shown with the following settings:





- Sweep Variable: ☒ Frequency
- Sweep Range: ☒ Start-Stop (Start: 1M, Stop: 15G)
- Sweep Type: Logarithmic (Points Per Decade: 100)
- Specialized Analyses: None
- Enabled: ☒

Red and green arrows indicate the mapping from the project tree to the dialog settings: a red arrow points from 'ac' to 'Sweep Variable', and a green arrow points from 'Req' to 'Sweep Range'.

- The degeneration R (or C) can be swept to change the amount of equalization or gain peaking.

2) AC Analysis:

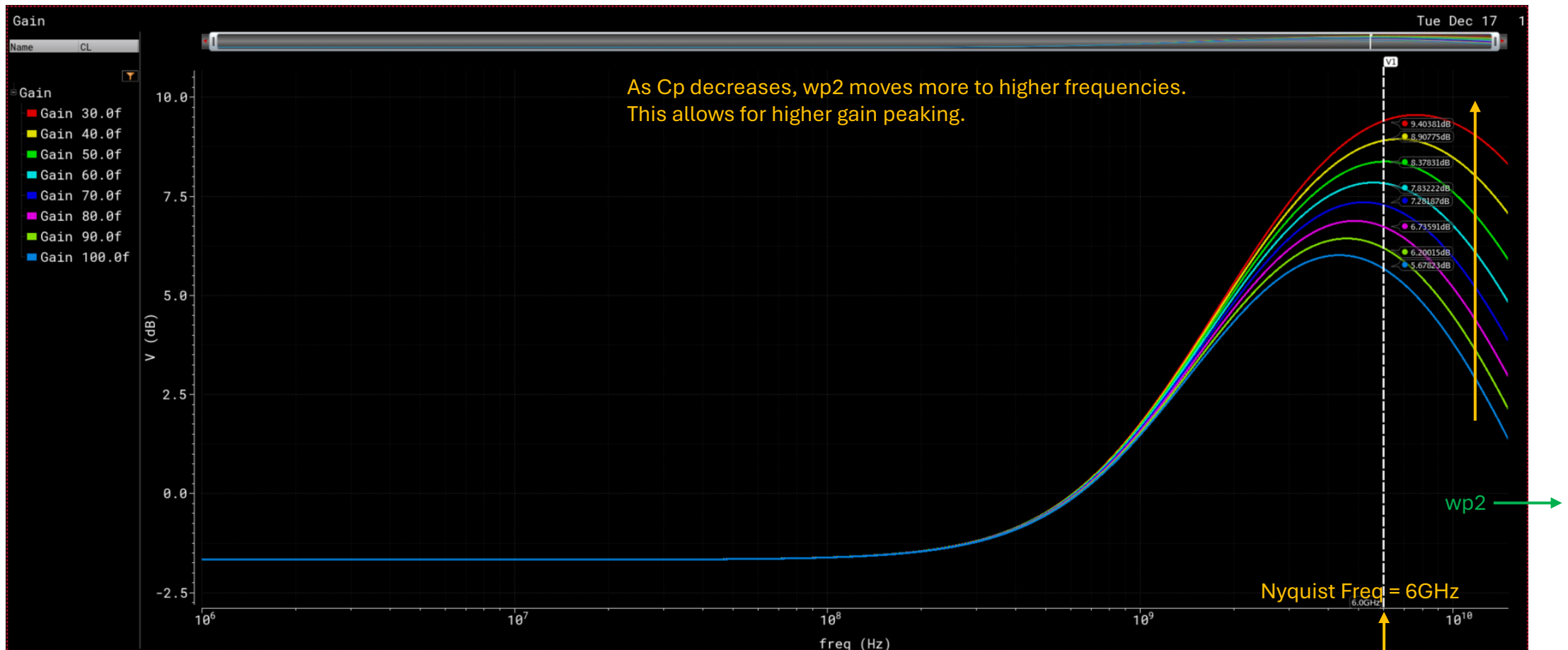
Measurements

Name	Type	Details	EvalType
Filter 	Filter 	Filter 	Filter 
Gain	expr	dB20((VF("/outp") - VF("/outn")))	point
Gain_at_DC	expr	value(Gain 0)	point
Gain_at_Nyq	expr	value(Gain (VAR("Data_rate") / 2))	point
Peaking	expr	(Gain_at_Nyq - Gain_at_DC)	point

2) AC Analysis:

Results - Sweeps

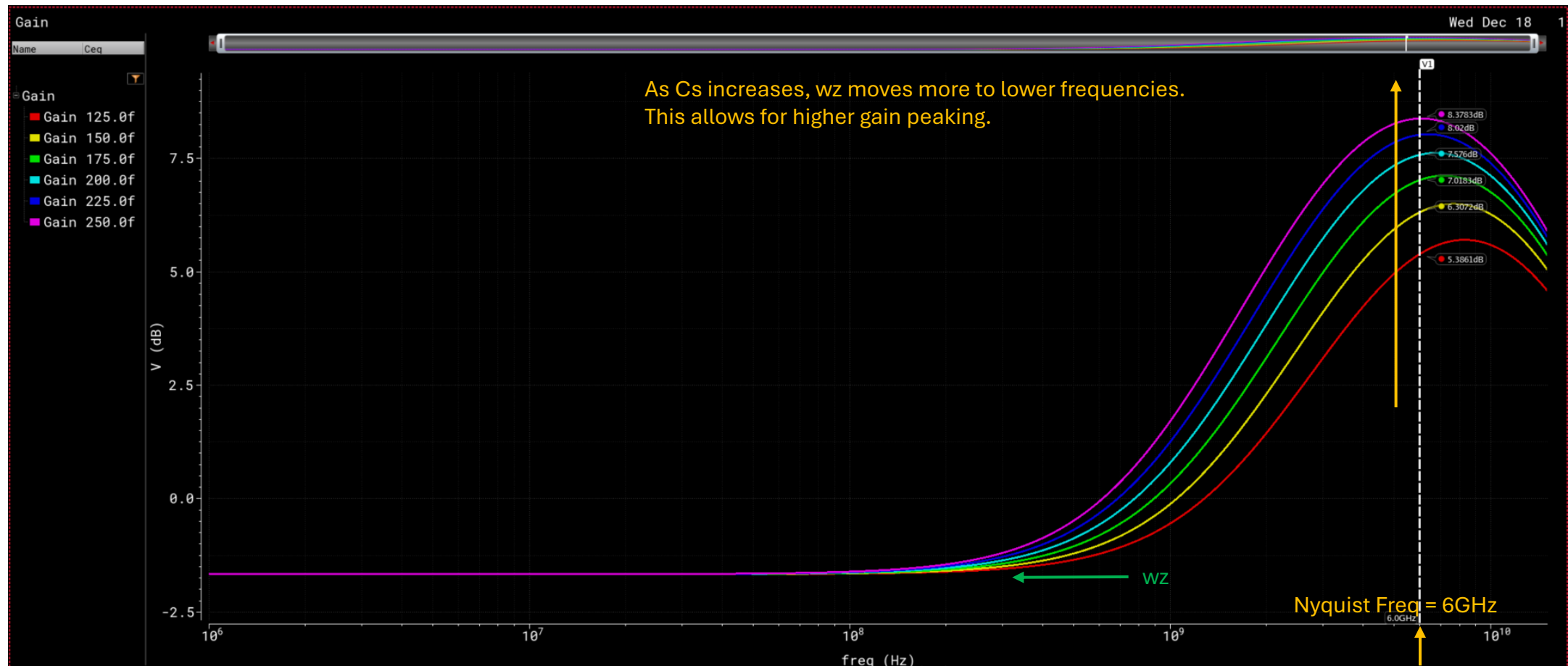
a) Sweeping C_p (Output loading Cap)



2) AC Analysis:

Results - Sweeps

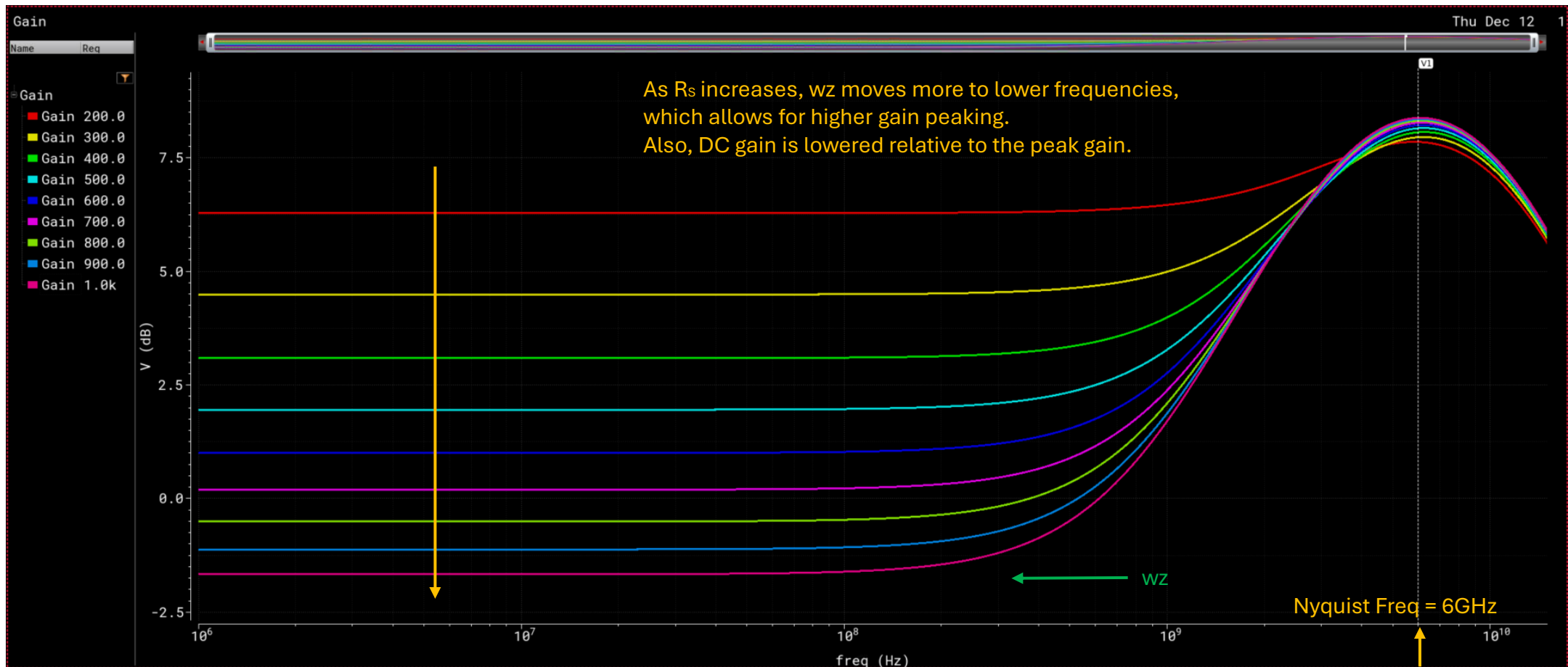
b) Sweeping C_s (Equalization Cap)



2) AC Analysis:

Results - Sweeps

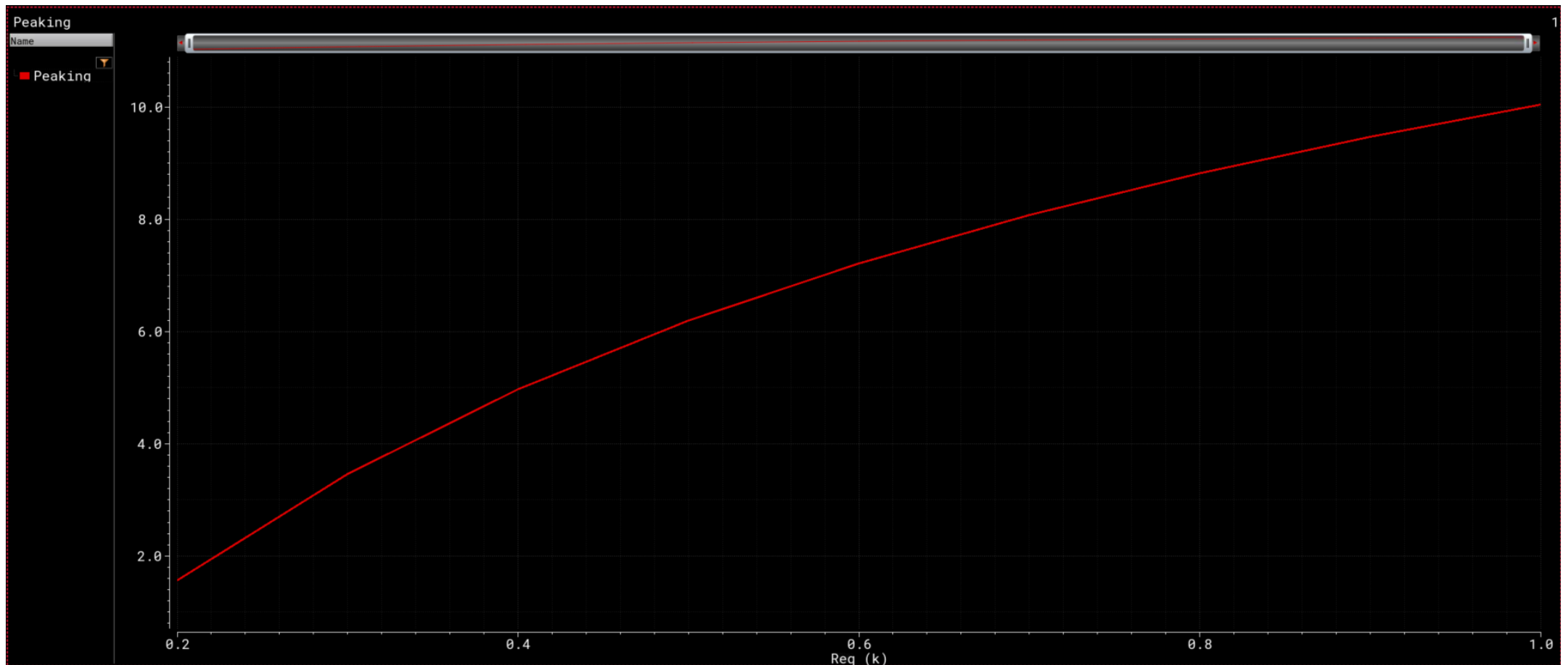
c) Sweeping R_s (Equalization Resistance)



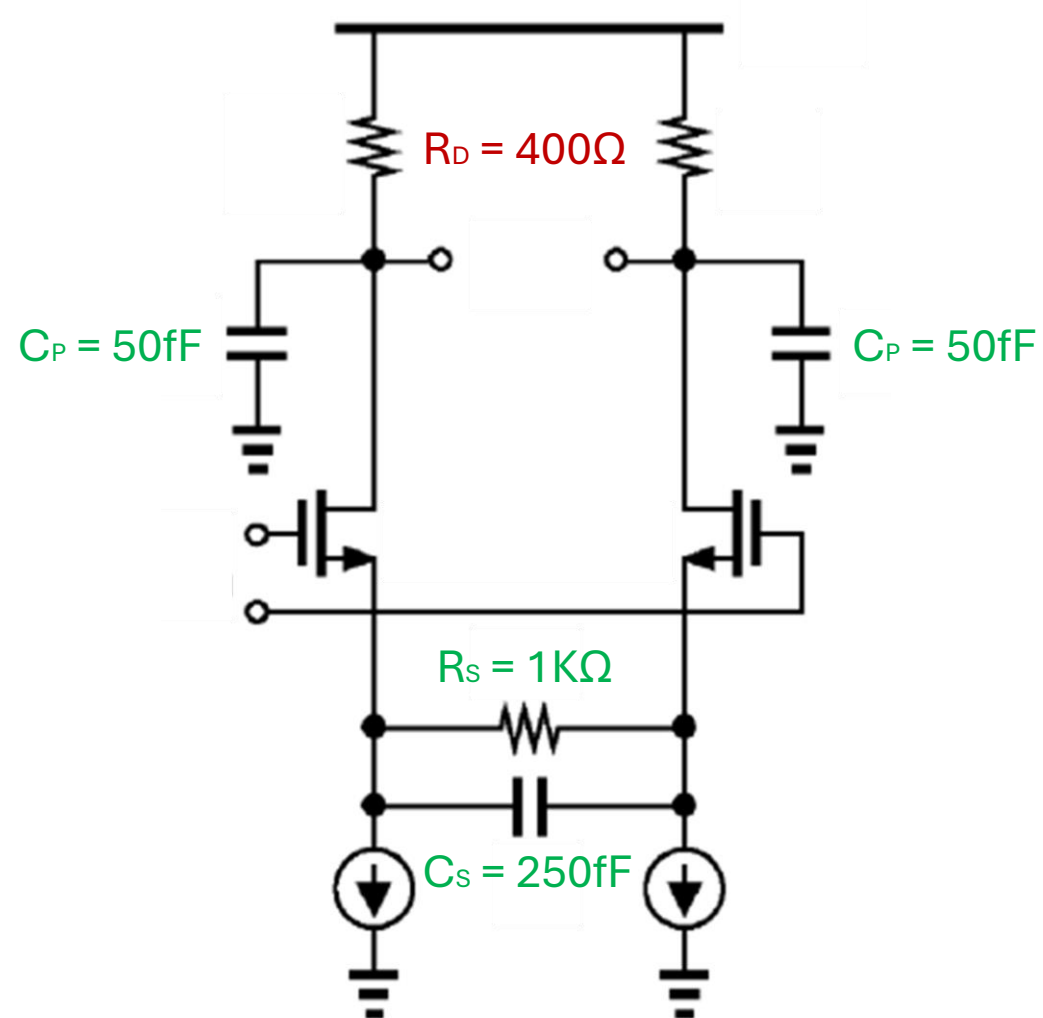
2) AC Analysis:

Results - Sweeps

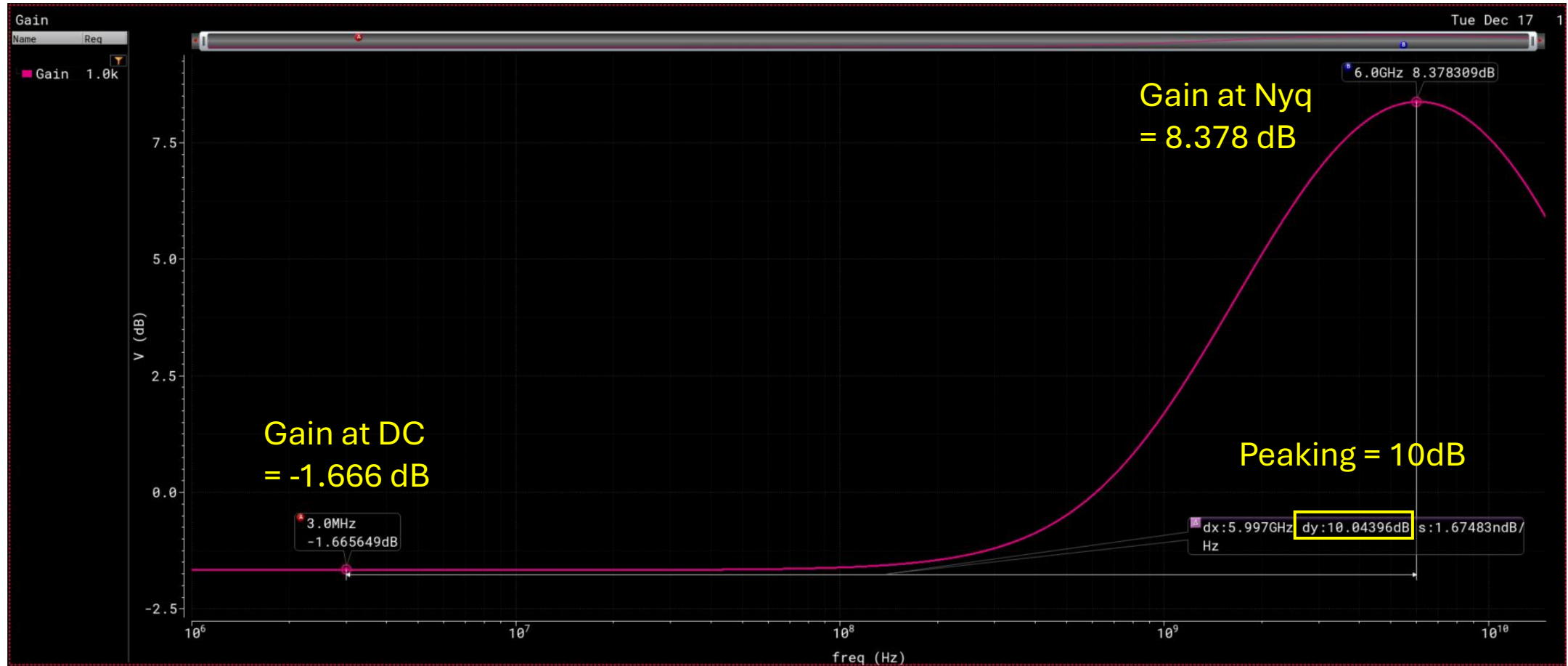
c) Sweeping R_s (Equalization Resistance)



2) AC Analysis: Results



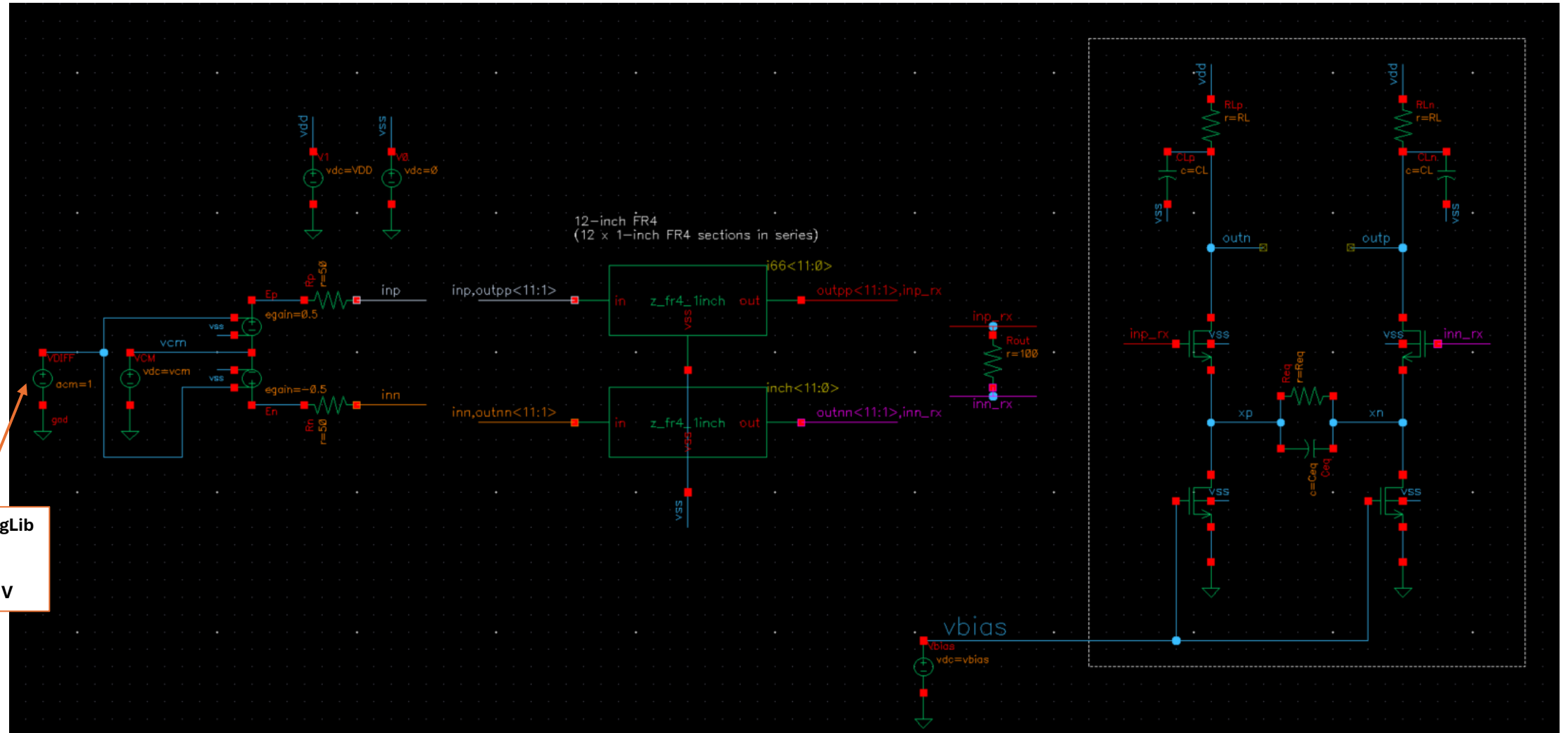
2) AC Analysis: Results



c) CTLE + Channel

1) AC Analysis: Testbench

➔ For Frequency Response



1) AC Analysis: Setup

The image shows the setup for an AC Analysis in a simulation software. The left pane displays a project tree with the following structure:

- Tests
 - AC
 - Simulator: spectre
 - Analyses
 - ac: 1M 15G 100 Logarithmic
 - Design Variables
- Global Variables
 - VDD: 1.2
 - Data_rate: 12G
 - Ceq: 250f
 - CL: 50f
 - vbias: 600m
 - Ibias_tx: 10m
 - Req: 1K
 - RL: 400
 - Rloadp: 50

A red arrow points from the 'ac' analysis entry in the project tree to the 'AC Analysis' dialog box on the right.

The 'AC Analysis' dialog box contains the following settings:

- Sweep Variable:** Frequency (selected), Design Variable, Temperature, Component Parameter, Model Parameter, None.
- Sweep Range:** Start-Stop (selected), Start: 1M, Stop: 15G, Center-Span.
- Sweep Type:** Logarithmic (selected), Points Per Decade: 100, Number of Steps.
- Specialized Analyses:** None.
- Enabled:** Checked.
- Options...** button.

1) AC Analysis:

Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
Hf_in	expr	dB20((VF("/inp_rx") - VF("/inn_rx")))	point
Hf_out	expr	dB20((VF("/outp") - VF("/outn")))	point
Hf_at_DC	expr	value(Hf_out 0)	point
Hf_at_Nyq	expr	value(Hf_out (VAR("Data_rate") / 2))	point
Peaking	expr	(Hf_at_Nyq - Hf_at_DC)	point

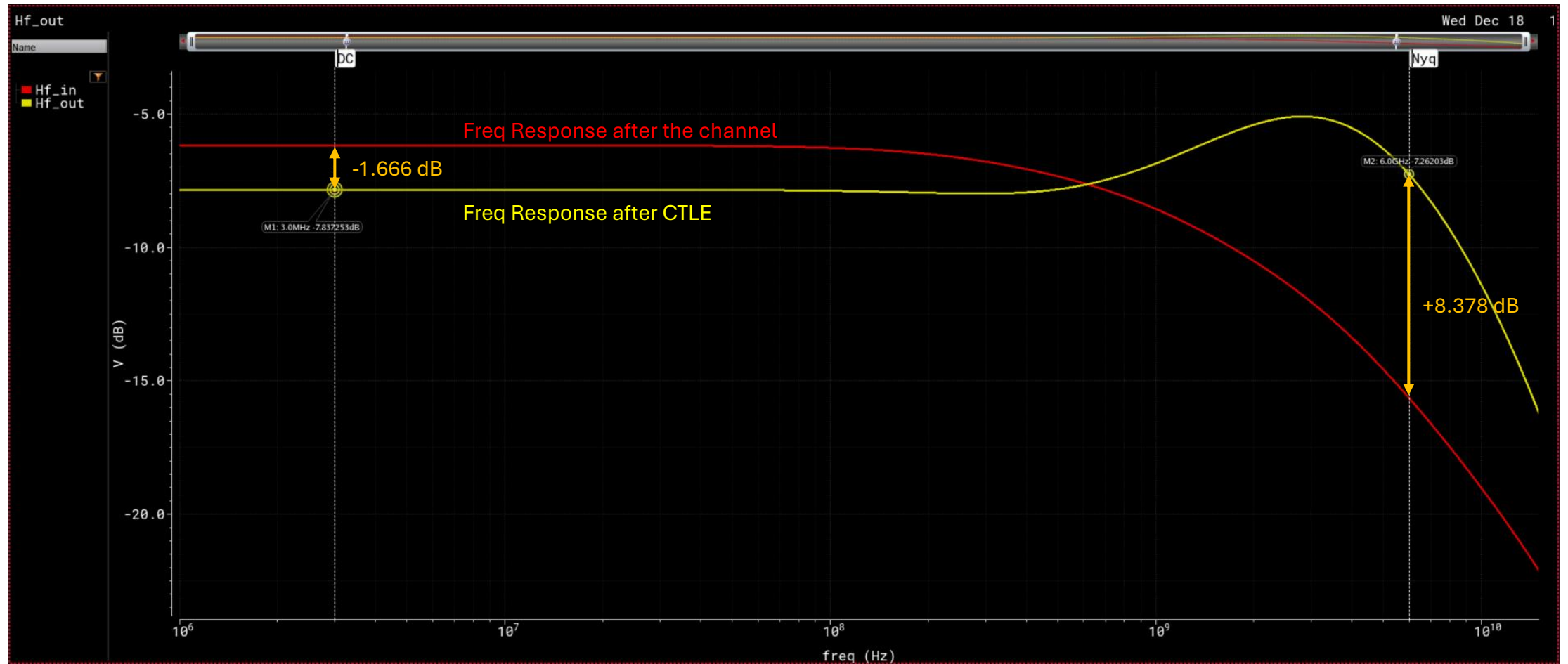
Hf_in = Freq Response after the channel

Hf_out = Freq Response after CTLE

Peaking = Gain Peaking @ Nyquist after CTLE

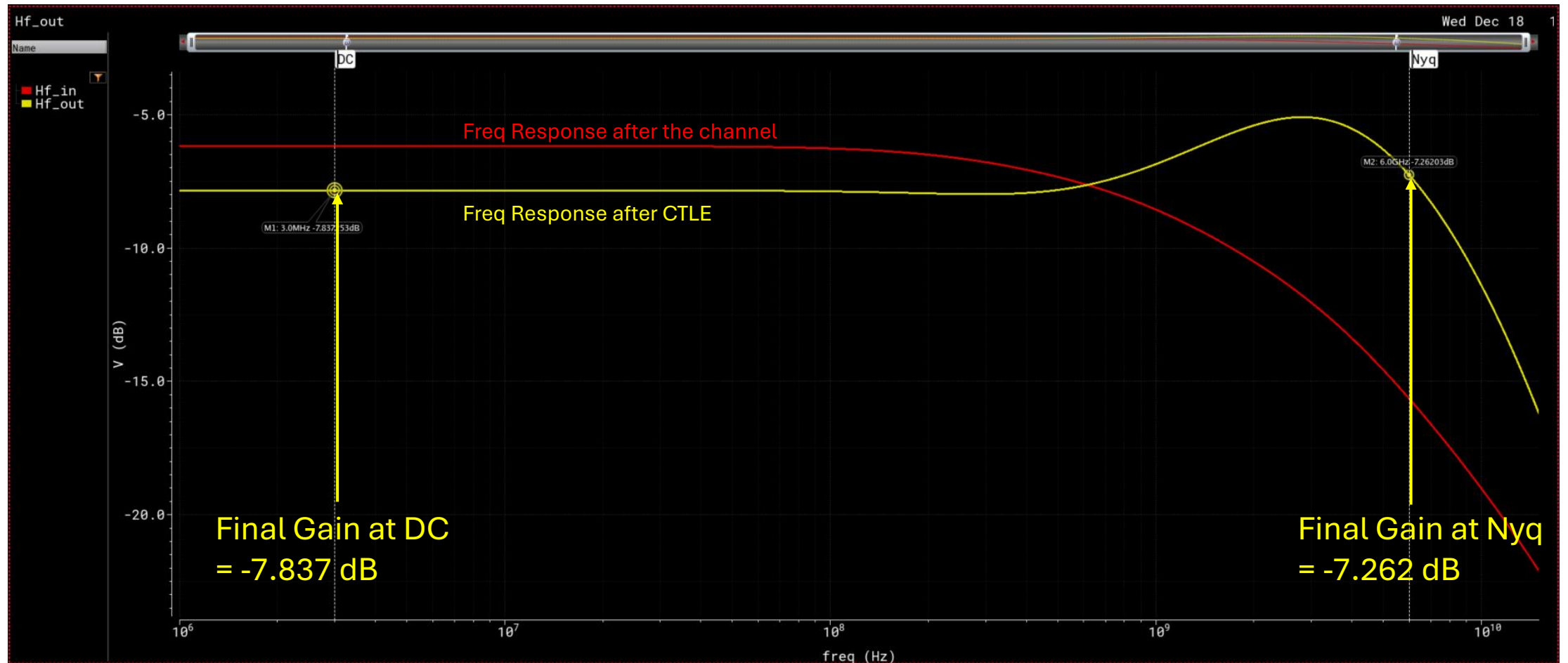
1) AC Analysis:

Results



1) AC Analysis:

Results



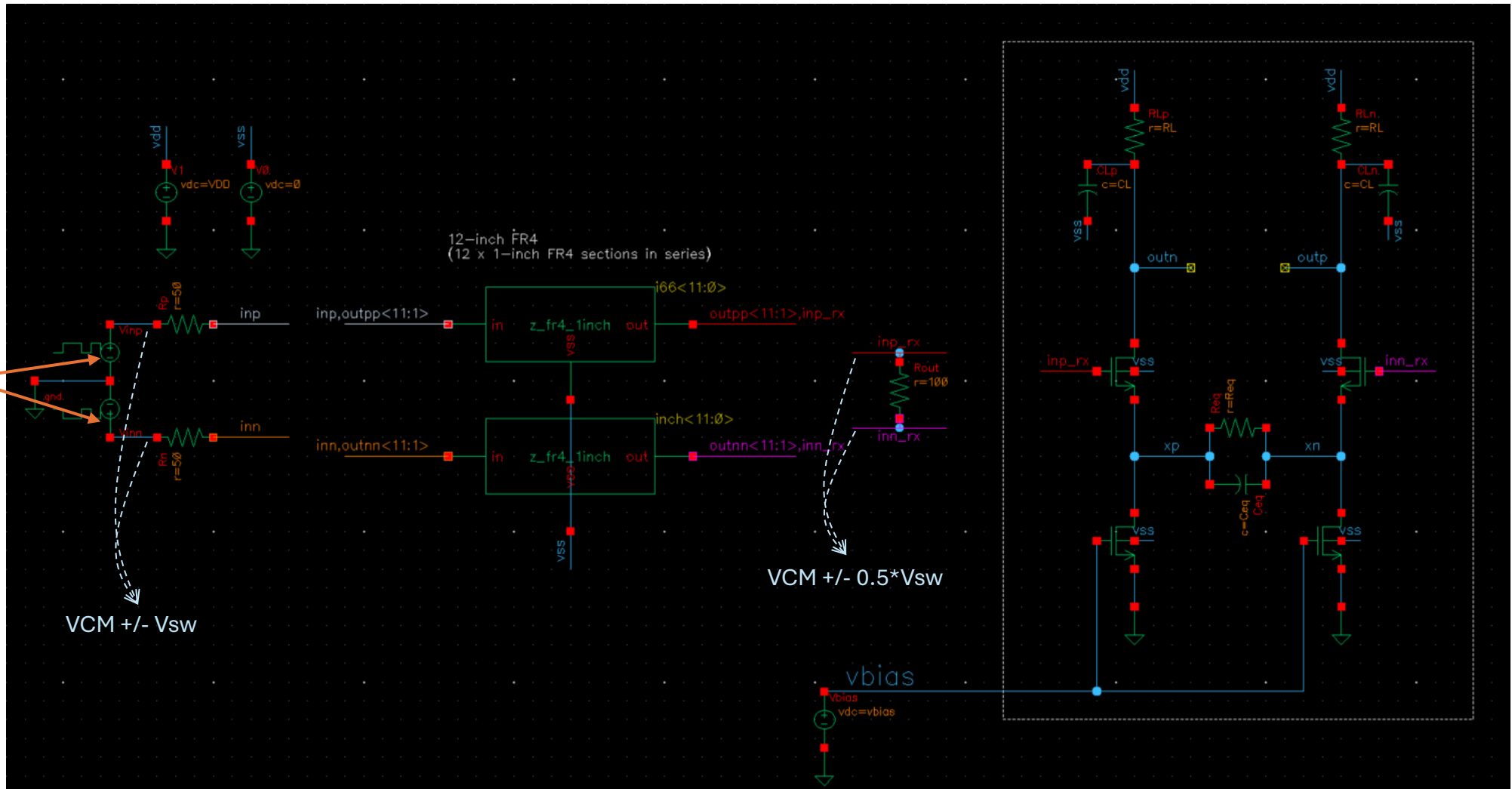
2) Transient Analysis: Testbench

➔ For Eye Diagrams

LIB: analogLib
CELL: vprbs

Zero value: $v_{cm} \pm 0.5$
One value: $v_{cm} \mp 0.5$
Bit period: **83.33ps**
(1/12G)

Rise/Fall times: **10 ps**
Edge type: **linear**
Trigger: **Internal**
LFSR Mode: **PN32**



2) Transient Analysis: Setup

The image shows a simulation setup interface. On the left is a project tree with a 'Name' and 'Value' column. On the right is a 'Transient Analysis' configuration panel. A red arrow points from the 'tran' analysis entry in the tree to the configuration panel.

Project Tree:

Name	Value
Filter	Filter
Tests	
Transient	
Simulator	spectre
Analyses	
tran	0 VAR("sim_time")
Design Variables	
Global Variables	
sim_time	2000n
VDD	1.2
Data_rate	12G
Ceq	250f
CL	50f
vbias	600m
Ibias_tx	10m
Req	1K
RL	400
Rloadp	50

Transient Analysis Configuration:

- Stop Time: VAR("sim_time")
- Accuracy Defaults: (errpreset)
- Transient Noise: ☐
- Dynamic Parameter: ☐
- HV_solution: ☐
- Enabled: ☒
- Options...

2) Transient Analysis: Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
	signal	/vcm	point
	signal	/inp	point
	signal	/inn	point
	signal	/inp_rx	point
	signal	/inn_rx	point
	signal	/outp	point
	signal	/outn	point
*** PK2PK ***	expr		point
Vchin_pk2pk	expr	(VT("/inp") - VT("/inn"))	point
Vchout_pk2pk	expr	(VT("/inp_rx") - VT("/inn_rx"))	point
Vctleout_pk2pk	expr	(VT("/outp") - VT("/outn"))	point
*** EYE ***	expr		point
EYE_ch_out	expr	eyeDiagram(Vchout_pk2pk 1e-08 VAR("sim_time") (2 * (1 / VAR("Data_rate")))) ?autoCenter t)	point
EYE_ctle_out	expr	eyeDiagram(Vctleout_pk2pk 1e-08 VAR("sim_time") (2 * (1 / VAR("Data_rate")))) ?autoCenter t)	point

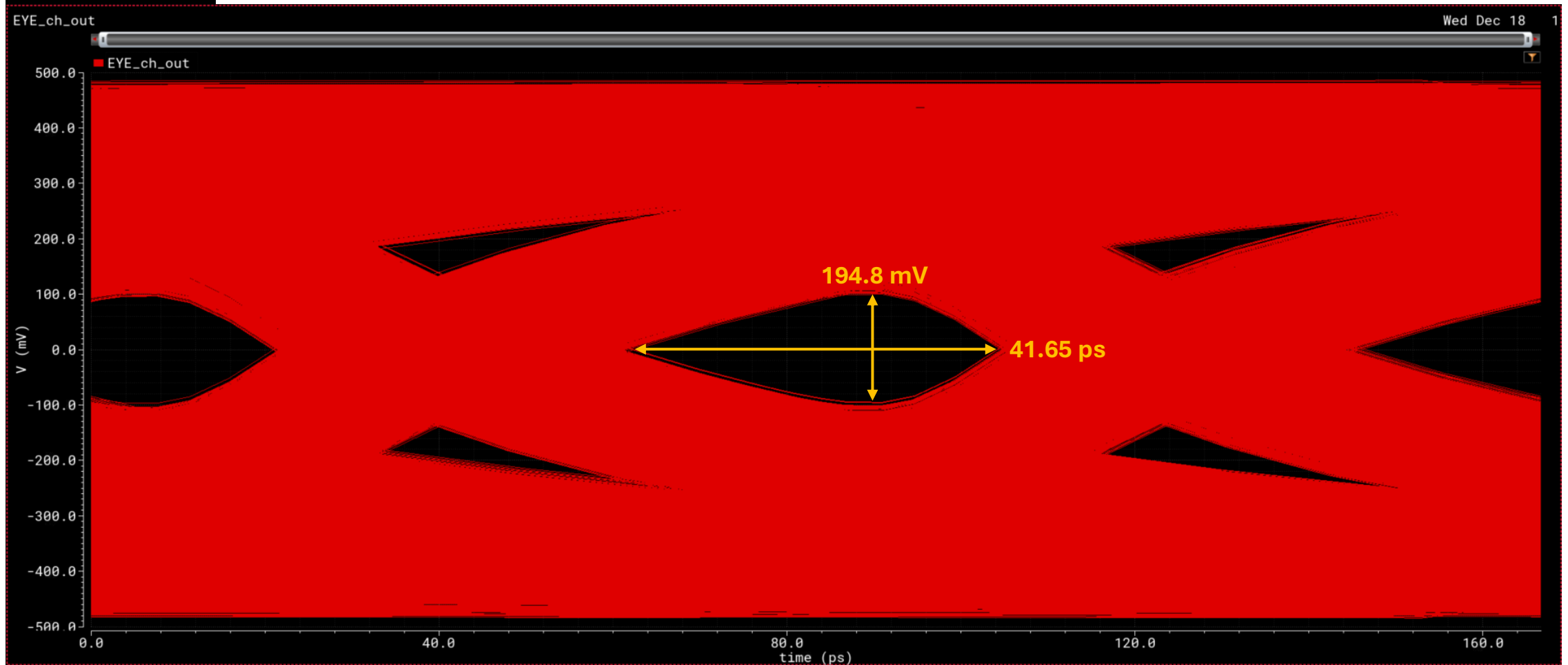
→ Eye Diagram at CTLE input

→ Eye Diagram at CTLE output

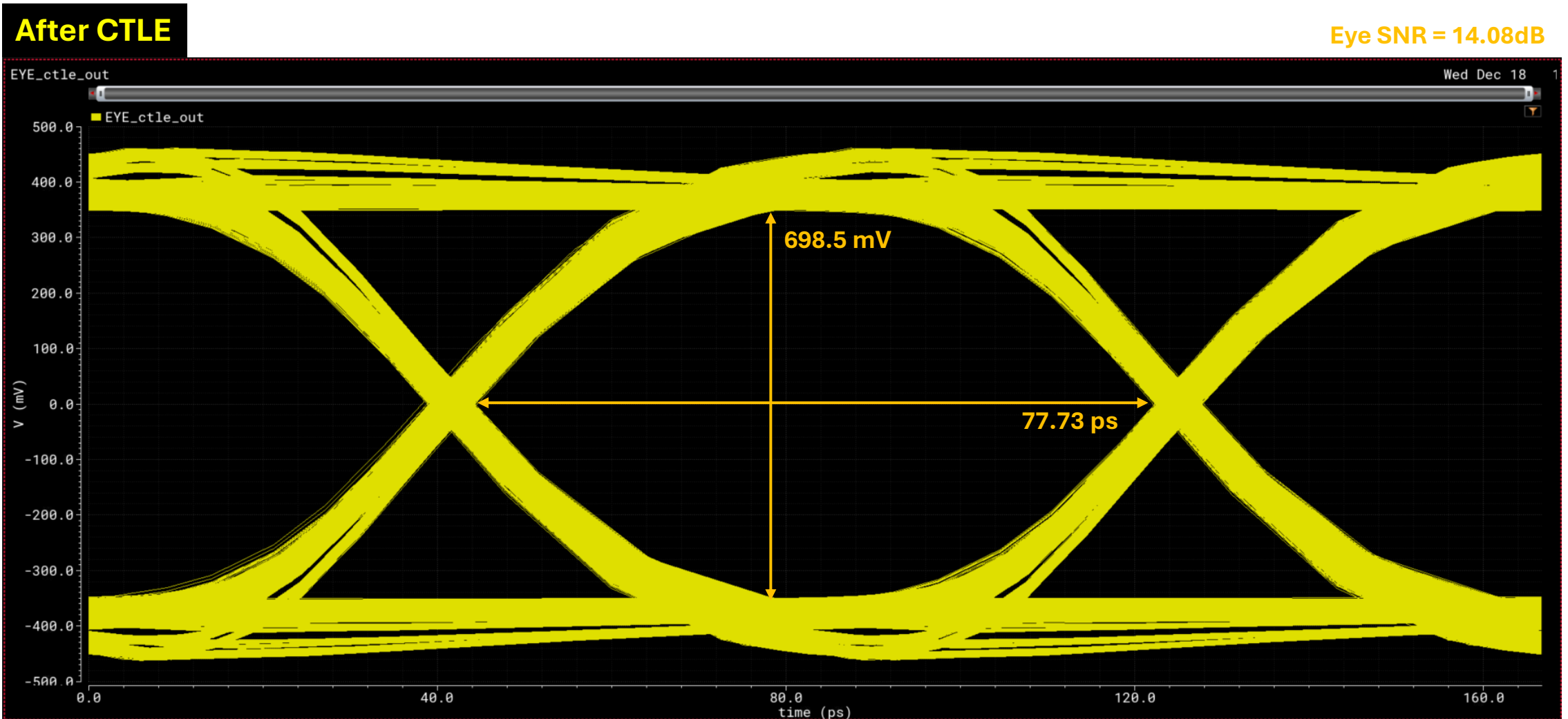
2) Transient Analysis: Eye Diagram

Before CTLE

Eye SNR = 2.51dB



2) Transient Analysis: Eye Diagram



2) Transient Analysis: Eye Diagram

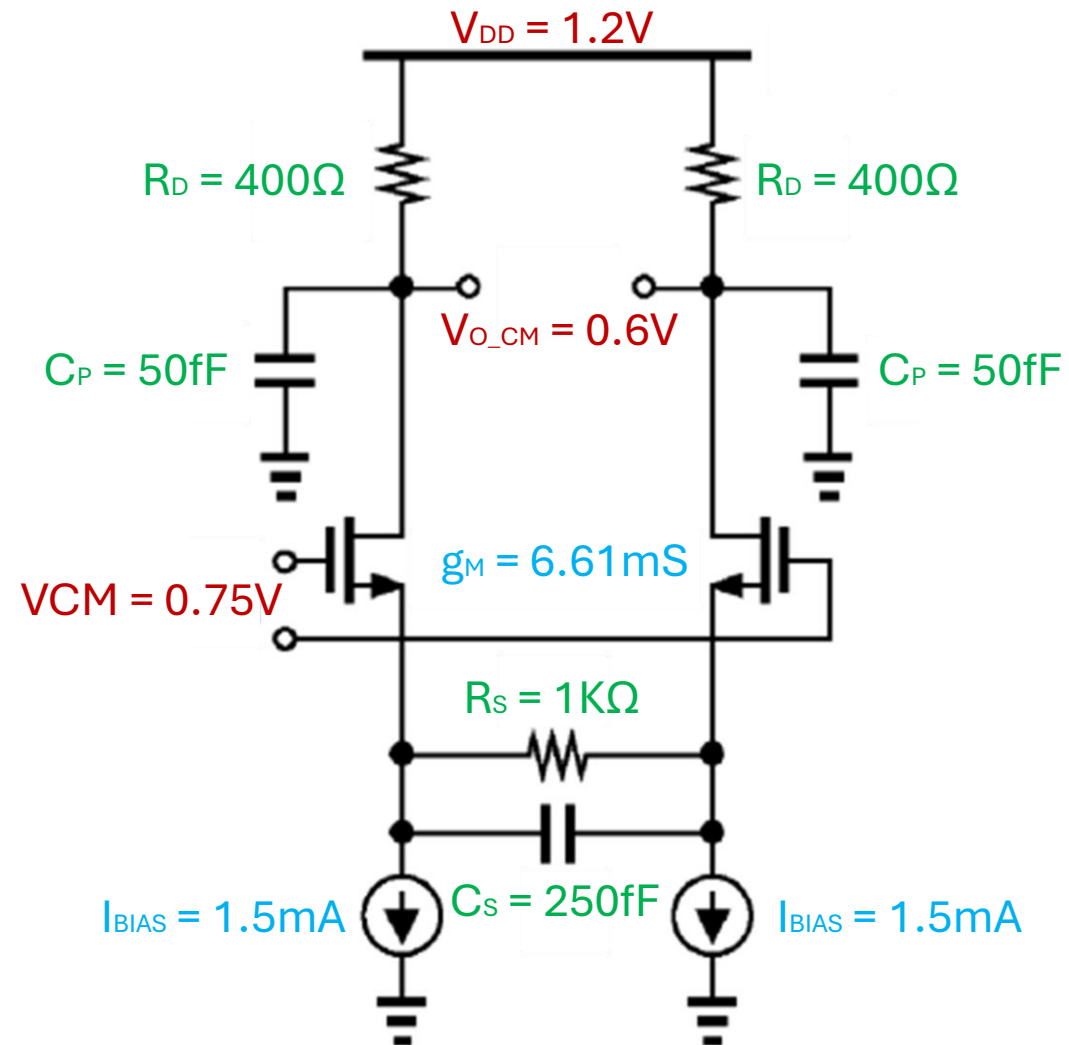


Summary

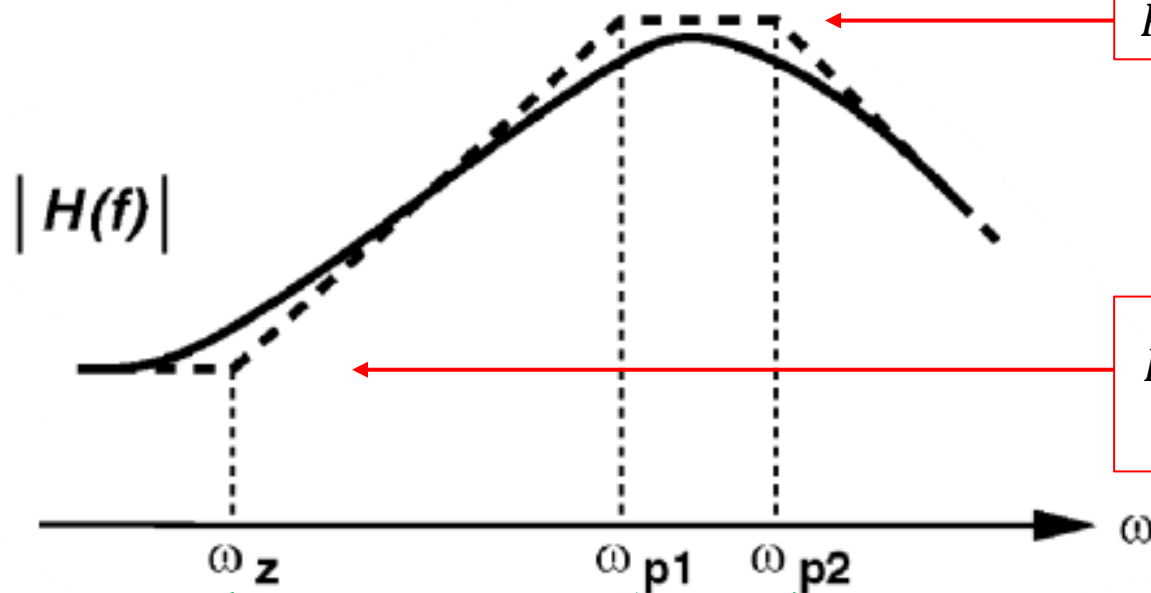
Design Parameters

Parameter	Value
Data Rate	12 Gb/s
VDD (for CTLE)	1.2 V
Input V_{SWING} (PK2PK)	0.5 V
Input V_{CM}	0.75 V
Channel	12-inch FR4
Output V_{CM}	0.6 V

Design Parameters



Poles/Zero/Gains (calculated based on previous values)



$$\text{Peak Gain} = 20 \log(g_m \cdot R_D) = 8.445 \text{ dB}$$

$$\text{DC Gain} = 20 \log \left(\frac{g_m \cdot R_D}{1 + g_m \cdot \frac{R_S}{2}} \right) = -4.23 \text{ dB}$$

$$f_Z = \frac{1}{2\pi \cdot R_S \cdot C_S} = 636.62 \text{ MHz}$$

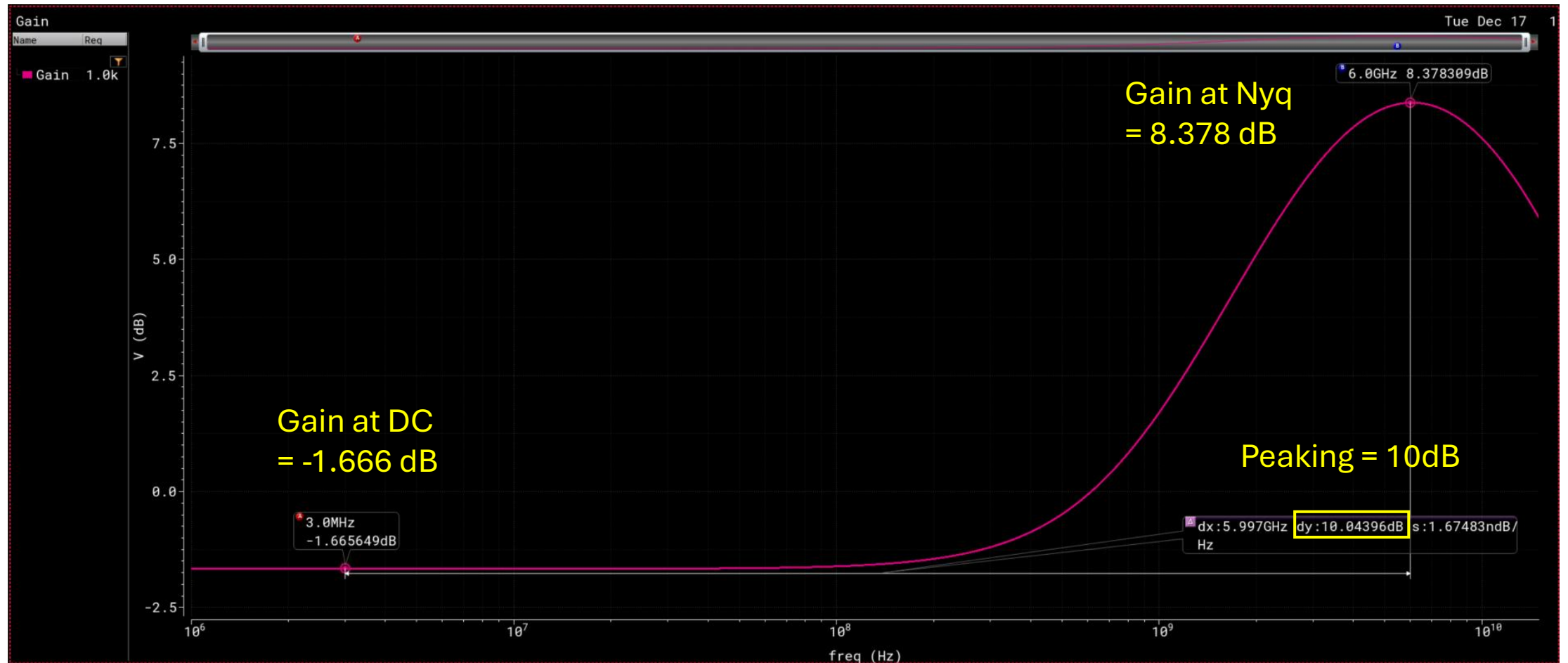
$$f_{P1} = \frac{1 + g_m \cdot \frac{R_S}{2}}{2\pi \cdot R_S \cdot C_S} = 2.74 \text{ GHz}$$

$$f_{P2} = \frac{1}{2\pi \cdot R_D \cdot C_P} = 8 \text{ GHz}$$

$$\text{Peaking} = 20 \log \left(1 + g_m \cdot \frac{R_S}{2} \right) = 12.68 \text{ dB}$$

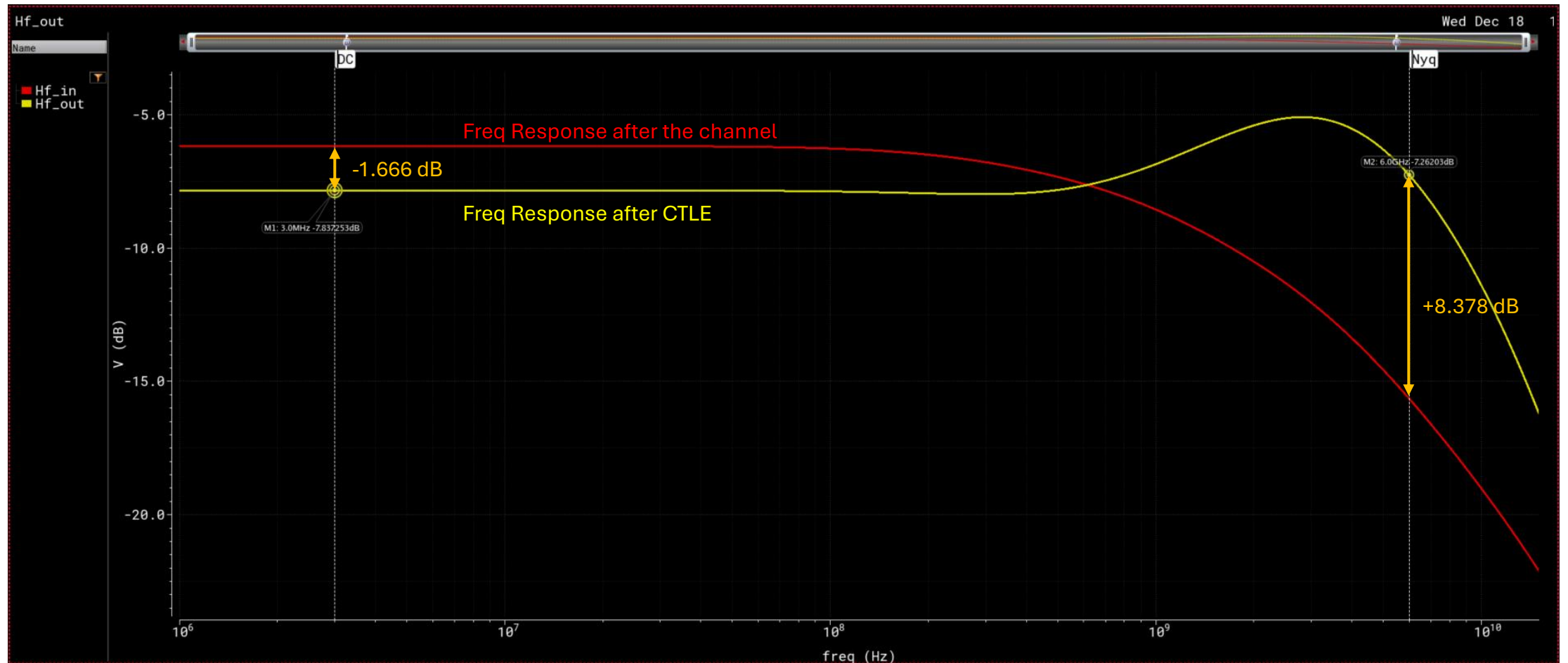
Final Results

→ Frequency Response of CTLE: (Simulated Values)



Final Results

→ Frequency Response of Channel + CTLE:



Final Results

→ Eye Diagrams:



Final Results

➔ Eye Diagram Comparison:

	Before CTLE (After Channel)	After CTLE
Eye Height (Max)	194.8 mV	698.5 mV
Eye Width (Max)	41.65 ps	77.73 ps
Eye SNR	2.51 dB	14.08 dB

Conclusion

- This project shows the design procedure & the testbench setup details used for the design of an Active RX CTLE Equalizer for a 12 Gb/s NRZ input & a channel of 12-inch FR4.