23 August 2023

Lab 06

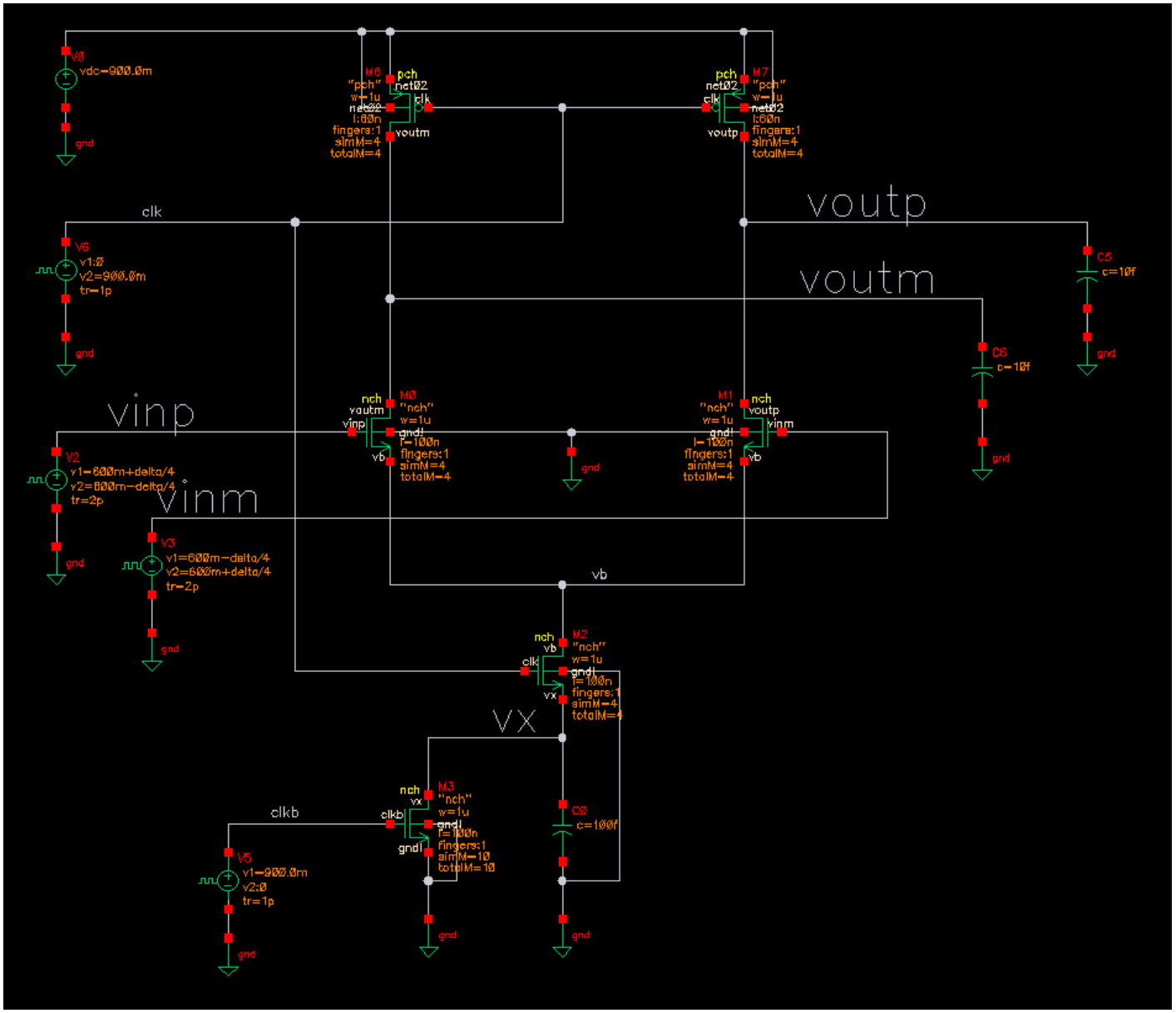
Charge Steering FF

Intended Learning Objectives

- Learn about CS Concept (small input)
- Learn about CS Concept (large input)

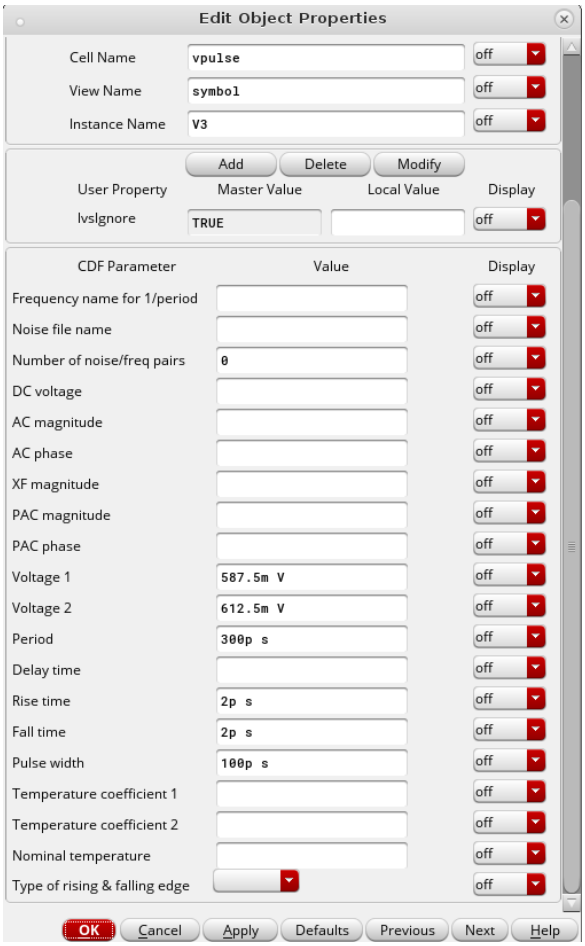
Part one

1. Schematic of charge steering circuit:
   a. create the schematic shown below for the charge steering circuit with small input swing (50 mVpp) and (vdd=900 mV).

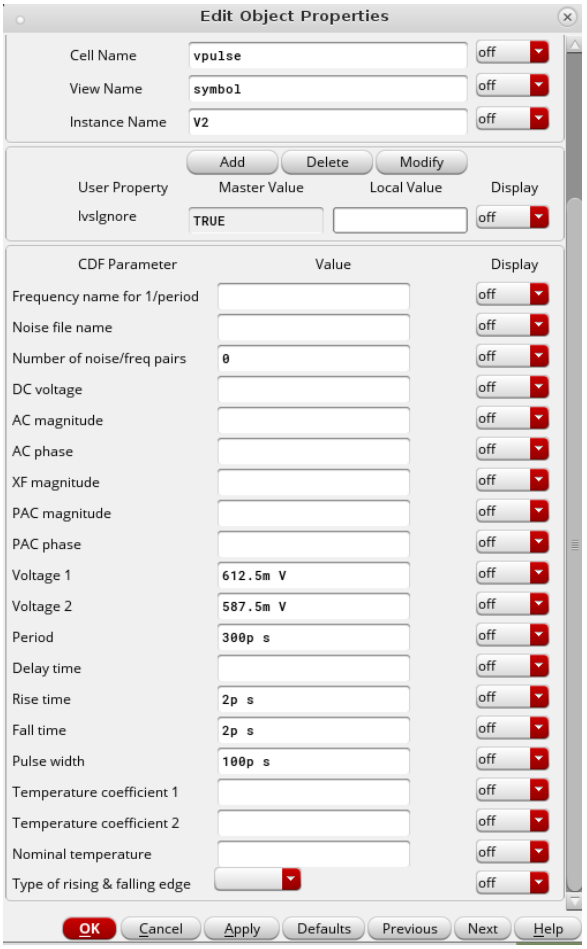


   b. the setting of the input sources and input clock (10GHz) is shown below:

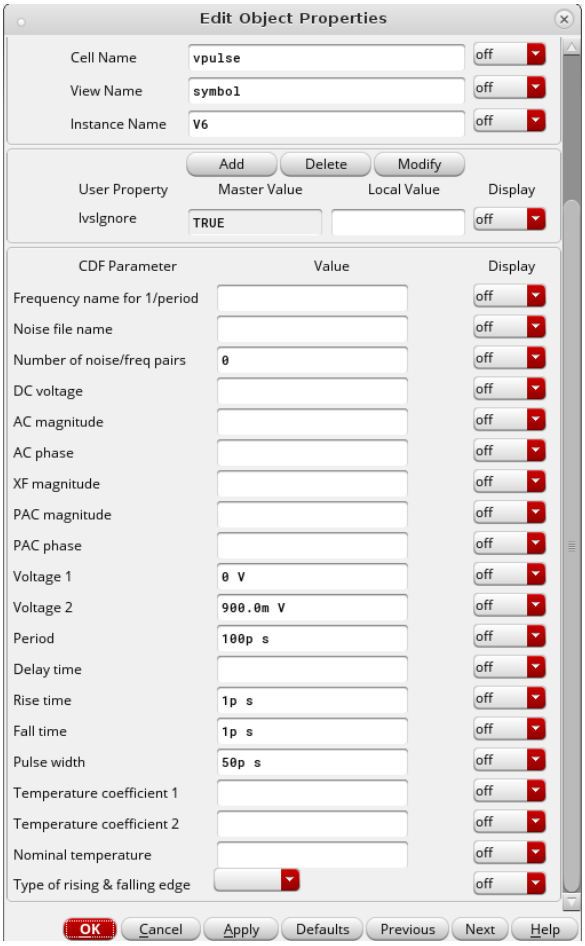
Vinm



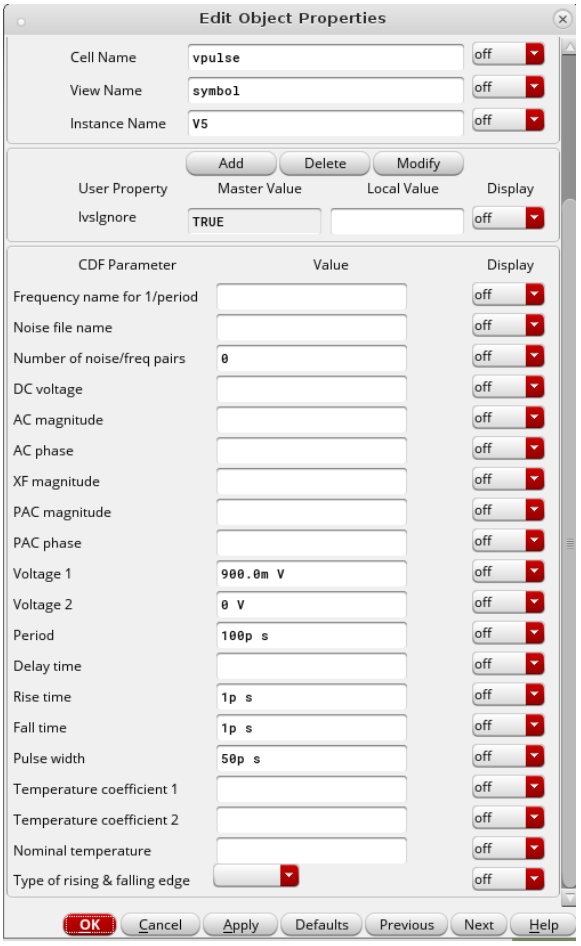
Vinp



clk

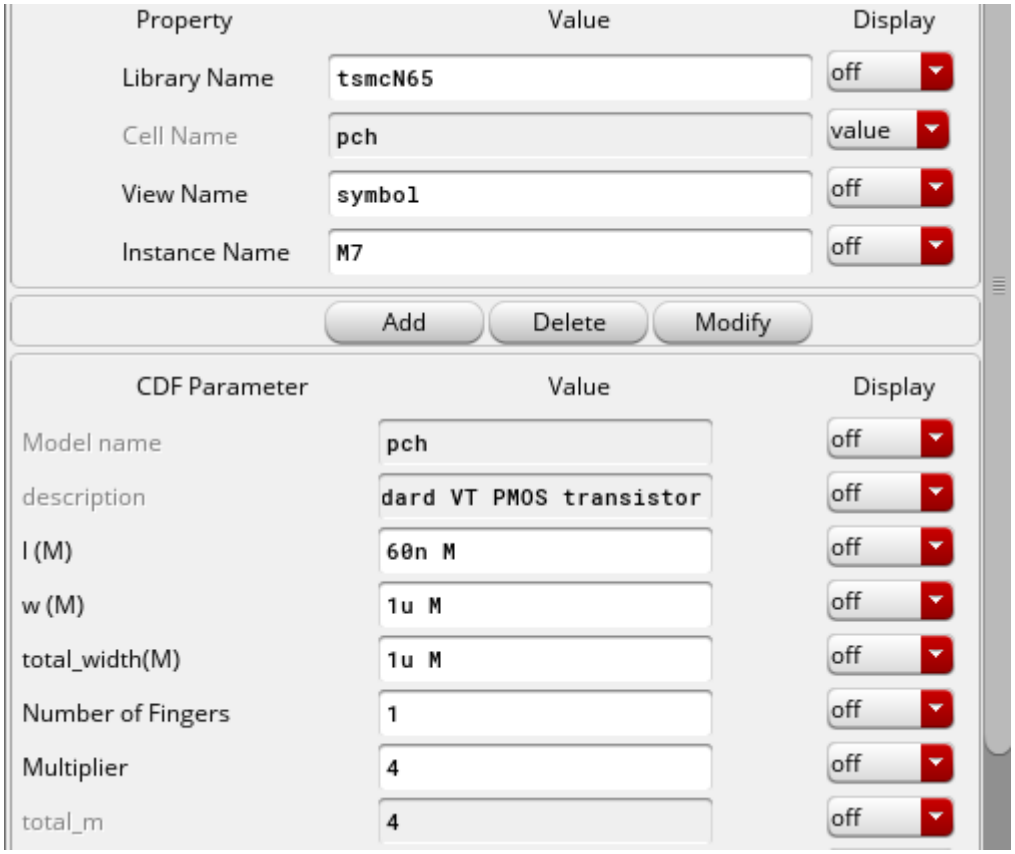


clkb

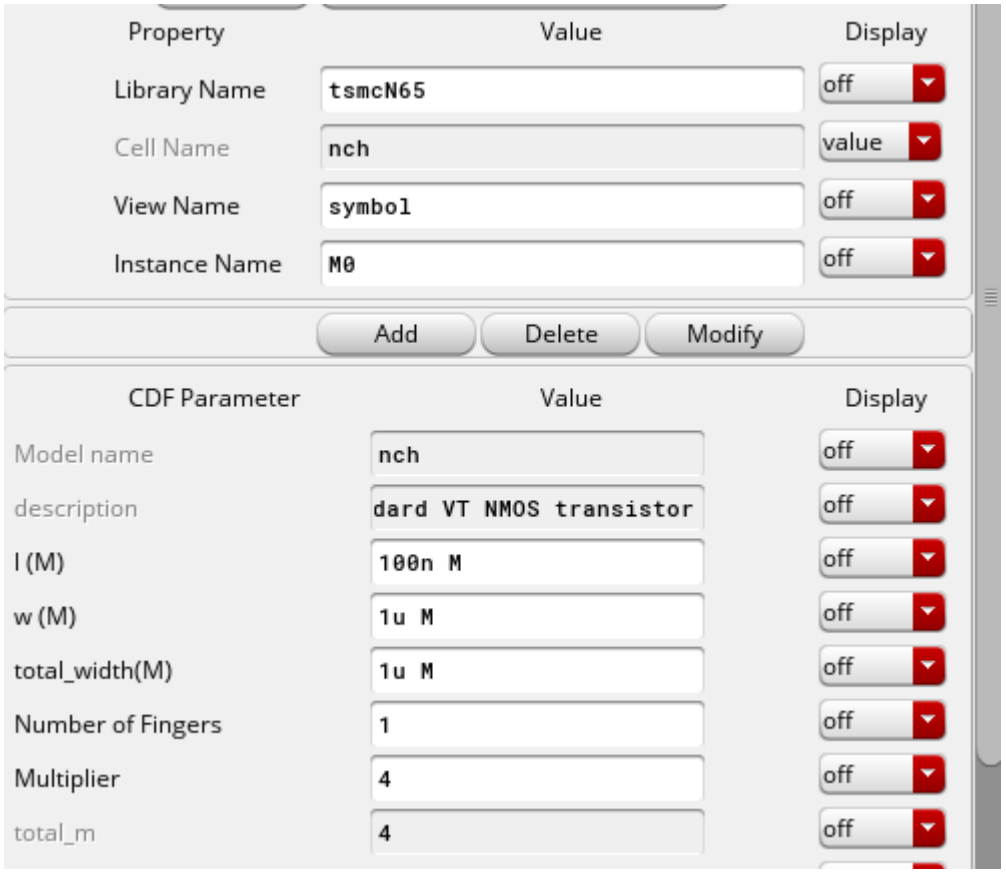


c. The setting of the transistors and CT, CD: CT=100fF , CD=10fF (Modes the external loading)

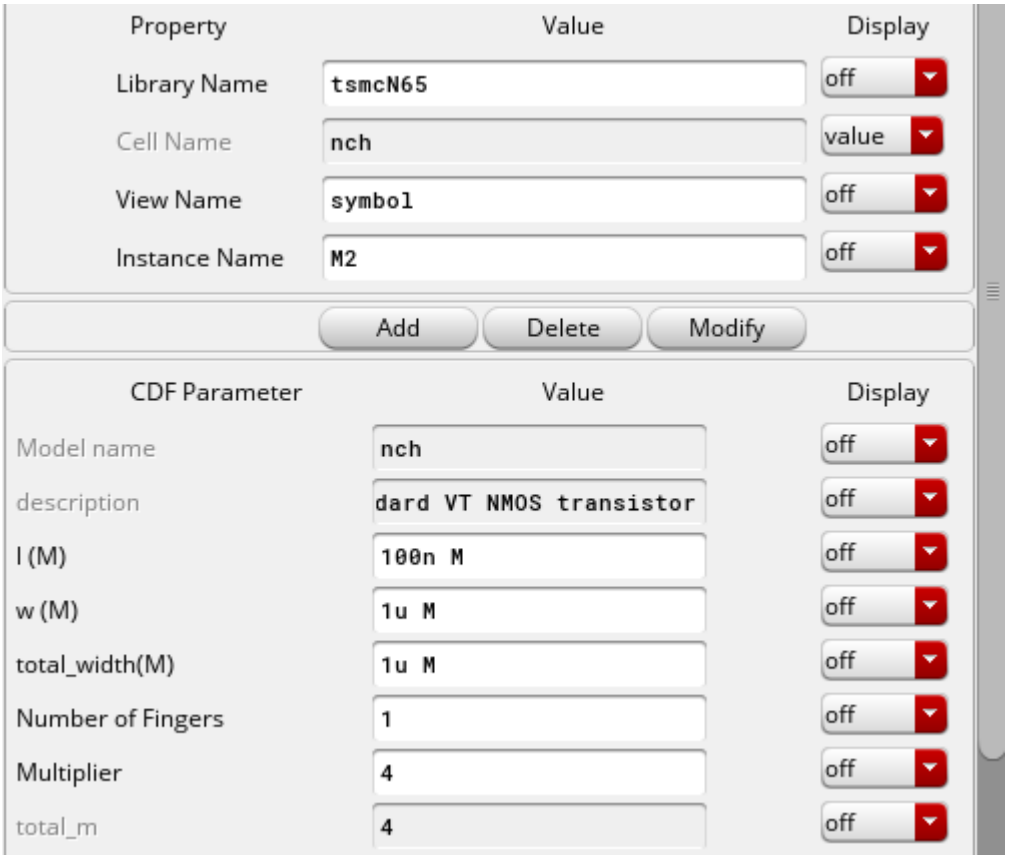
M6&M7:



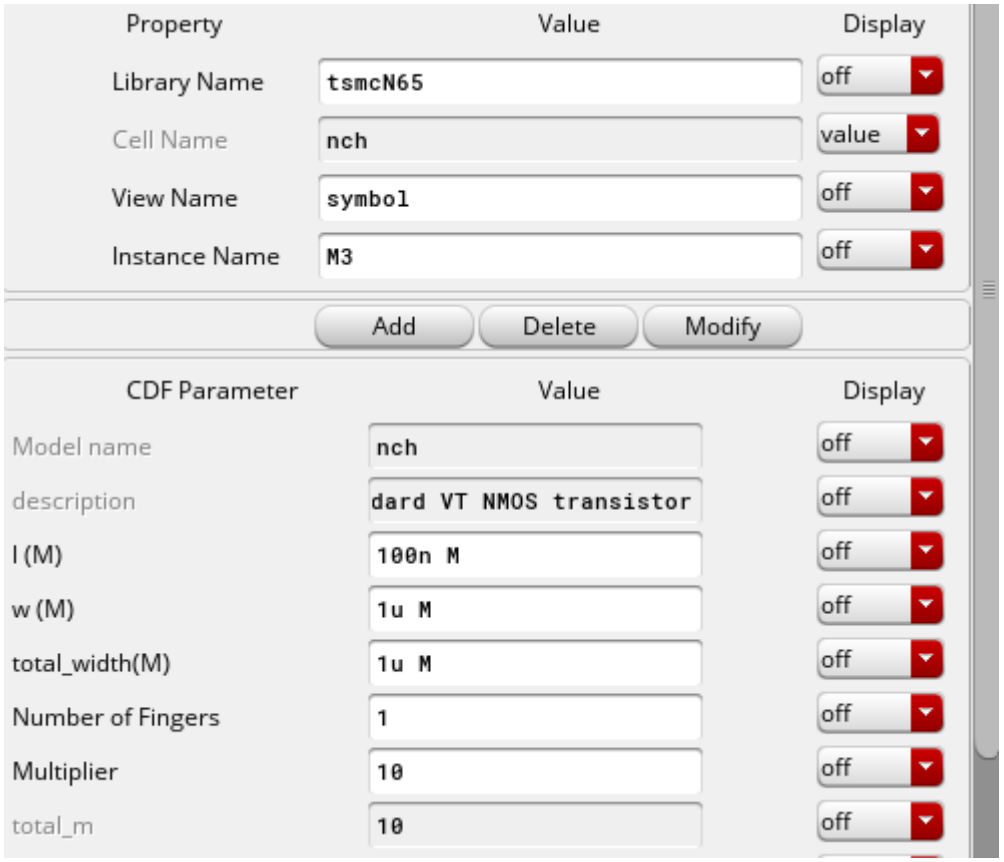
M0&M1:



M2:



M3:



Q1: comment on the size of M6&M7 and the trade off with the gain?

2- Transient simulation:

Run transient simulation for 500ps and plot the following:

a. Vinp-diff:

b. VX:

Q2: comment on the swing at Vx node?

c. Plot Voutp & Voutm:

Q3: comment on the behavior of the two signals?

d. Plot Vout-diff:

e. Calculate Power consumption:

Q4: Mention the effect of increasing CT on the power consumption and the reason for that?

Part two

1- Same schematic but with large input swing (500mVpp):

a. Plot Vinp-diff:

b. Plot VX:

c. Plot Voutp & Voutm:

Q5: For the Voutp&Voutm, make a comparison between the low swing and large swing inputs "compare with part one"?

d. Plot Vout-diff:

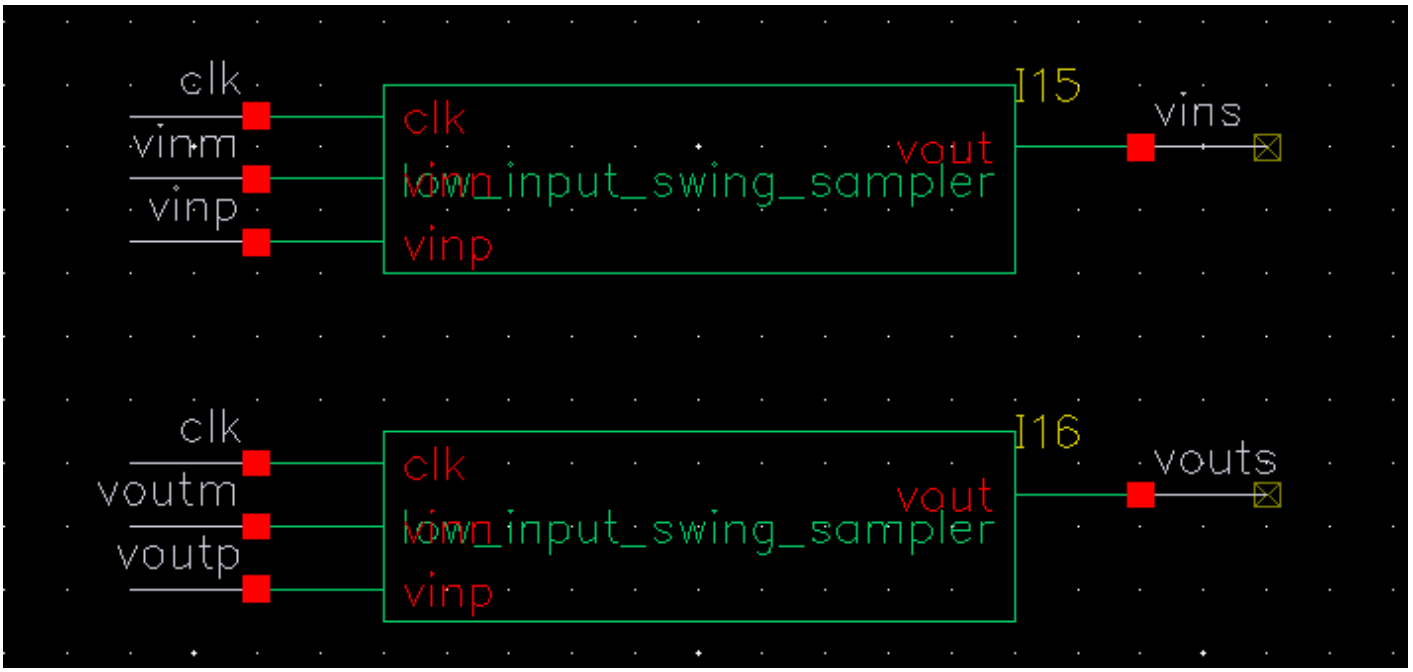
e. Calculate Power consumption :

Part three

- Plot Vout VS Vin for different values of the input swing and plot the Gain:
  first we need to add samplers to remove the reset phase effect to calculate the gain
  Veriloga code for the sampler:

```
// VerilogA for charge_steering_lab, low_input_swing, veriloga

`include "constants.vams"
`include "disciplines.vams"

module low_input_swing_sampler(vinp,vinn,clk,vout);
input vinn,vinp,clk;
output vout;
electrical vinn, vinp, vout, clk;
real vdiff =0;
parameter trise = 1p;



analog begin
@(initial_step("tran", "pss")) begin

vdiff = 0;

end
@(cross(V(clk) - 0.45, -1))

vdiff = V(vinp)-V(vinn);

V(vout) <+ transition (vdiff,0,trise);
end

endmodule
```

- symbol and the connection:



- setting of the input sources:

Voltage 1	600m+delta/4 V	off
Voltage 2	600m-delta/4 V	off
Period	300p s	off
Delay time		off
Rise time	2p s	off
Fall time	2p s	off
Pulse width	100p s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge		off

Voltage 1	600m-delta/4 V	off
Voltage 2	600m+delta/4 V	off
Period	300p s	off
Delay time		off
Rise time	2p s	off
Fall time	2p s	off
Pulse width	100p s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge		off

- sweep delta from 0 to 500mV with 50mV step.

a. Plot Vins:

b. Plot Vouts:

c. Plot Vout VS Vin @200ps:

d. Plot Gain @200ps: