Rx DFE (1-tap)

12 Gbps

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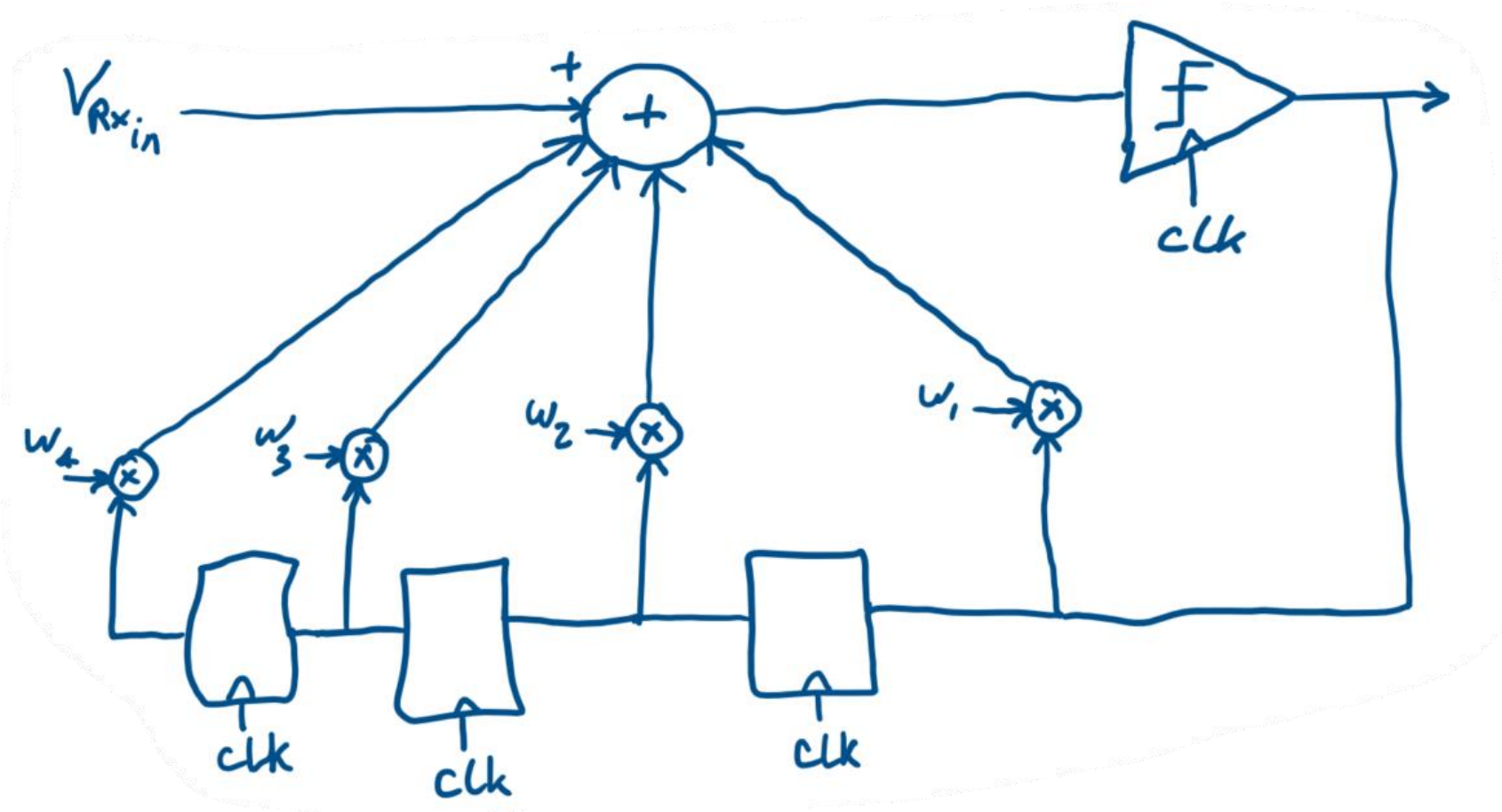
Outline

1. Design Implementation
2. Tests & Simulations
   a) Pulse Response
   b) Frequency response (DFE loop open)
   c) Eye Diagrams (DFE loop closed)
3. Summary

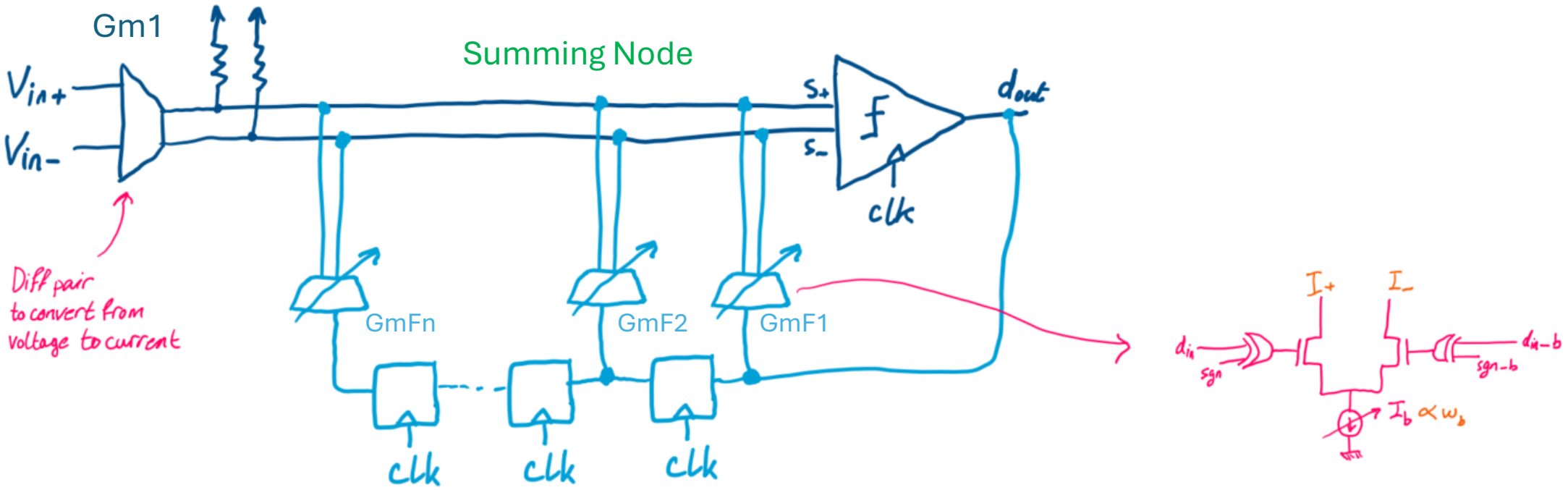
DFE Design Implementation

Concept



[1] From “EE 290C - High-Speed Electrical Interface Circuit Design” Course, Lec. 8, by Dr. Elad Alon

Implementation



[1] From “EE 290C - High-Speed Electrical Interface Circuit Design” Course, Lec. 8, by Dr. Elad Alon

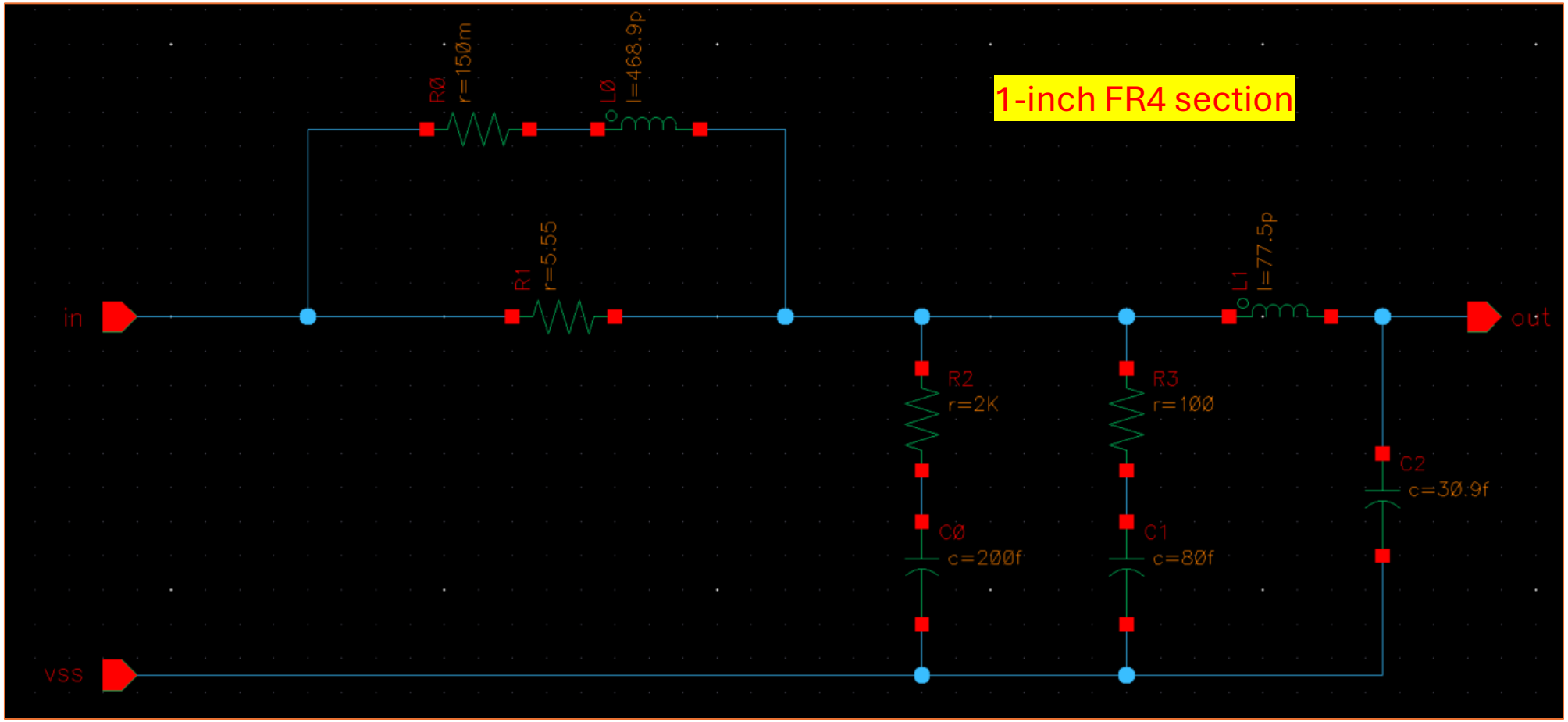
Tests & Simulations

Design Parameters

Parameter	Value
Data Rate	12 Gb/s
VDD (for CTLE & DFE)	1.2 V
Input $V_{SWING\ (PK2PK)}$ [From TX side]	0.4 V
Input V_{CM} [From TX side]	0.75 V
Channel	14-inch FR4
Output V_{CM}	0.6 V

CTLE design used is based on this project:
https://github.com/muhammadaldacher/SERDES-Design-of-RX-Continuous-time-linear-equalizer

Channel = 14 x 1-inch FR4 section

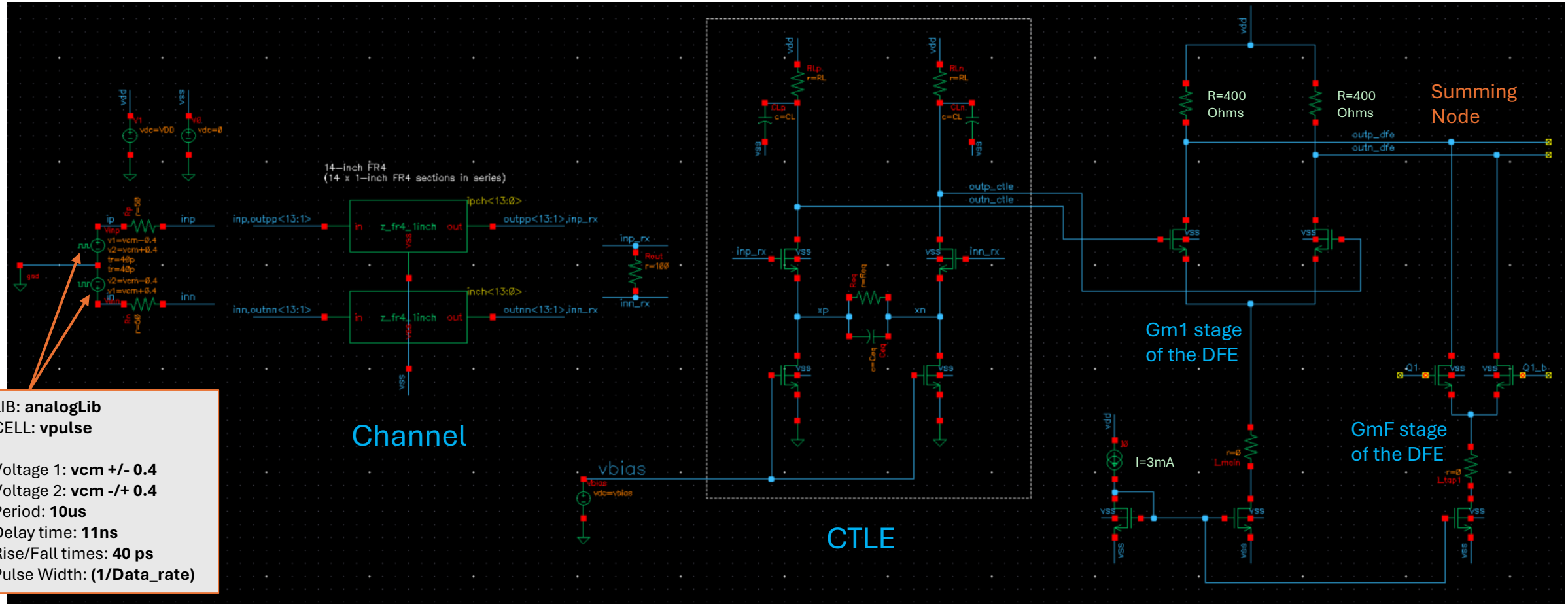


a) Pulse Response

This test is to see how much the post-cursors' values are compared to the main cursor value

a) Pulse Response:

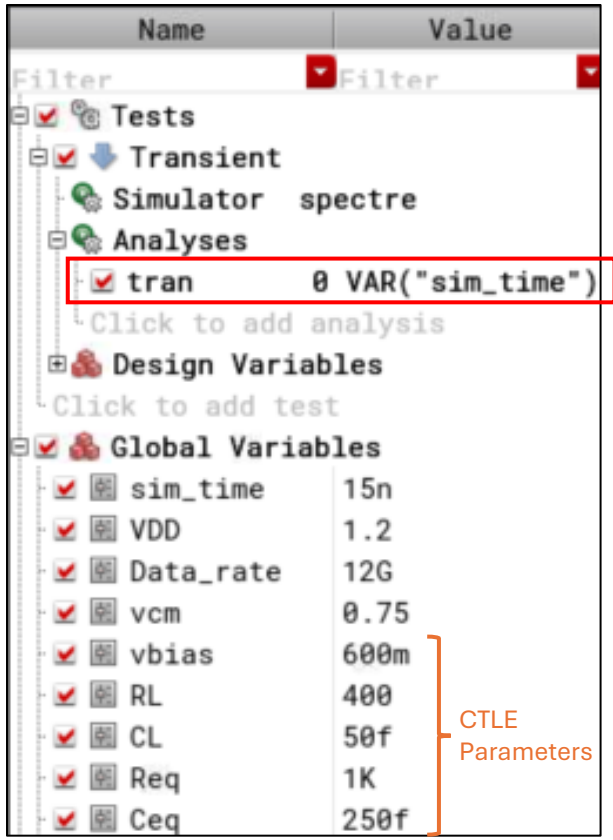
Testbench



LIB: **analogLib**
CELL: **vpulse**

Voltage 1: **vcm +/- 0.4**
Voltage 2: **vcm -/+ 0.4**
Period: **10us**
Delay time: **11ns**
Rise/Fall times: **40 ps**
Pulse Width: **(1/Data_rate)**

a) Pulse Response: Setup



a) Pulse Response:

Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
	signal	/vcm	point
	signal	/ip	point
	signal	/in	point
	signal	/inp	point
	signal	/inn	point
	signal	/inp_rx	point
	signal	/inn_rx	point
	signal	/outp_ctle	point
	signal	/outn_ctle	point
	signal	/outp_dfe	point
	signal	/outn_dfe	point
*** PK2PK ***	expr		point
Vchin_pk2pk	expr	(VT("/inp") - VT("/inn"))	point
Vchout_pk2pk	expr	((VT("/inp_rx") - VT("/inn_rx")) + 0.4)	point
Vctleout_pk2pk	expr	(VT("/outp_ctle") - VT("/outn_ctle"))	point
Vdfeout_pk2pk	expr	(VT("/outp_dfe") - VT("/outn_dfe"))	point
** Main Cursor **	expr		point
Data_rate	expr	VAR("Data_rate")	point
UI	expr	(1 / Data_rate)	point
t_cursor_main	expr	xmax(Vchout_pk2pk)	point
cursor_main	expr	value(Vchout_pk2pk t_cursor_main)	point
** Post & Pre Cursors **	expr		point
t_cursor_pre_1	expr	(t_cursor_main - UI)	point
t_cursor_post_1	expr	(t_cursor_main + UI)	point
t_cursor_post_2	expr	(t_cursor_main + (2 * UI))	point
cursor_pre_1	expr	value(Vchout_pk2pk t_cursor_pre_1)	point
cursor_post_1	expr	value(Vchout_pk2pk t_cursor_post_1)	point
cursor_post_2	expr	value(Vchout_pk2pk t_cursor_post_2)	point
percent_pre_1	expr	((cursor_pre_1 / cursor_main) * 100)	point
percent_post_1	expr	((cursor_post_1 / cursor_main) * 100)	point
percent_post_2	expr	((cursor_post_2 / cursor_main) * 100)	point

Pk2Pk Output of Channel (We add $V_{swing(PK2PK)}$ to shift the whole curve to above 0)

Pk2Pk Output of CTLE

Pk2Pk Output of DFE Gm1 stage (Summing Node)

Time of Main Cursor

Value of Main Cursor

Times of Pre & Post Cursors

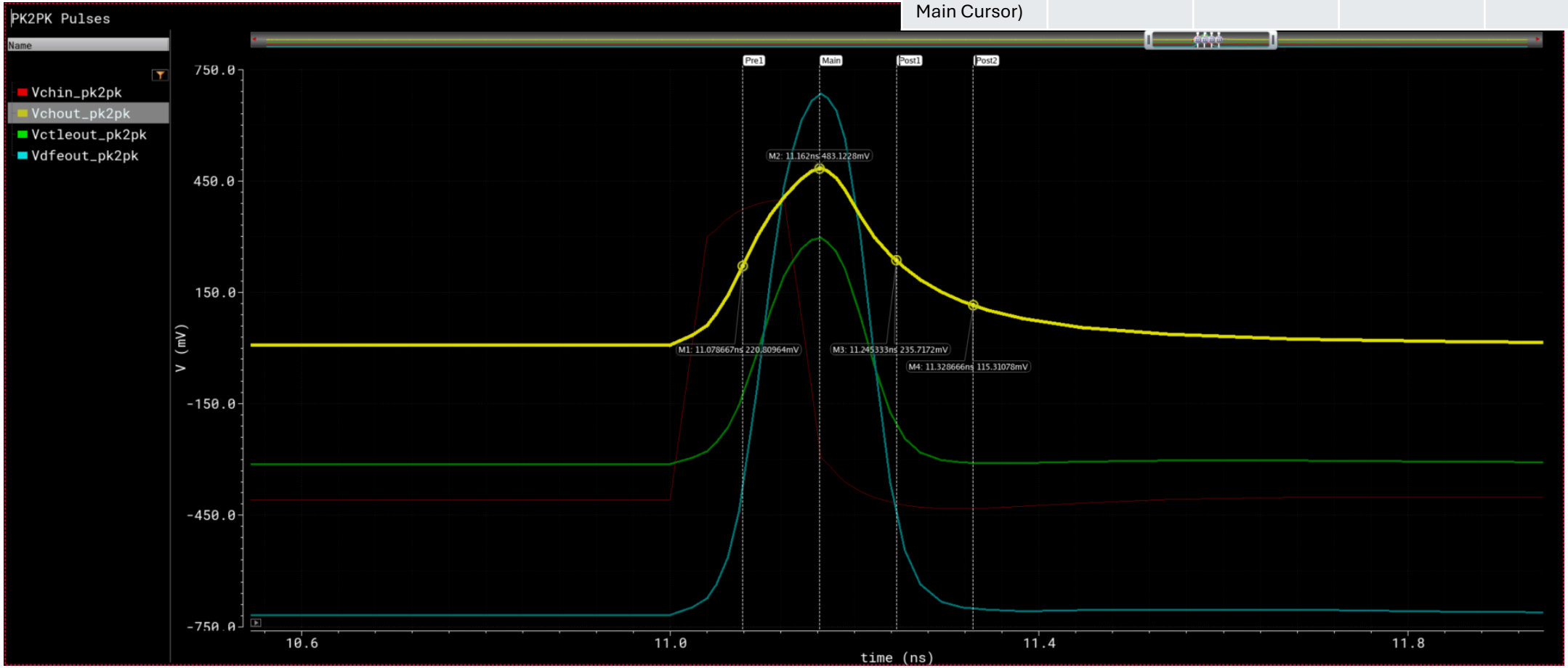
Values of Pre & Post Cursors

Percentages of Pre & Post Cursors (with respect to the main cursor)

Note:
DFE is used to cancel Post-Cursors only

a) Pulse Response: Waveforms

	Channel Outputs			
	Pre-Cursor 1	Main-Cursor	Post-Cursor 1	Post-Cursor 2
Time	11.07866 ns	11.162 ns	11.24533 ns	11.32866 ns
Voltage	220.81 mV	483.12 mV	235.72 mV	115.31 mV
Percentage (compared to Main Cursor)	46 %	100 %	48.8 %	23.9 %

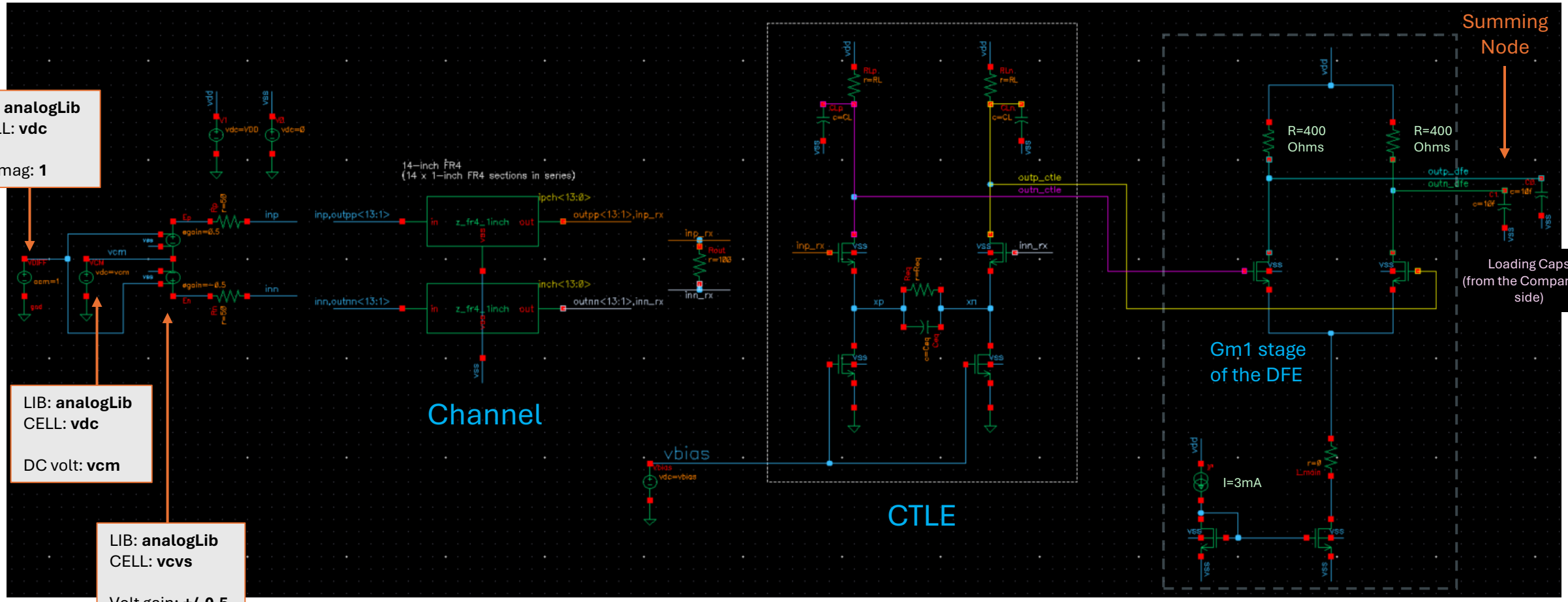


b) Frequency Response

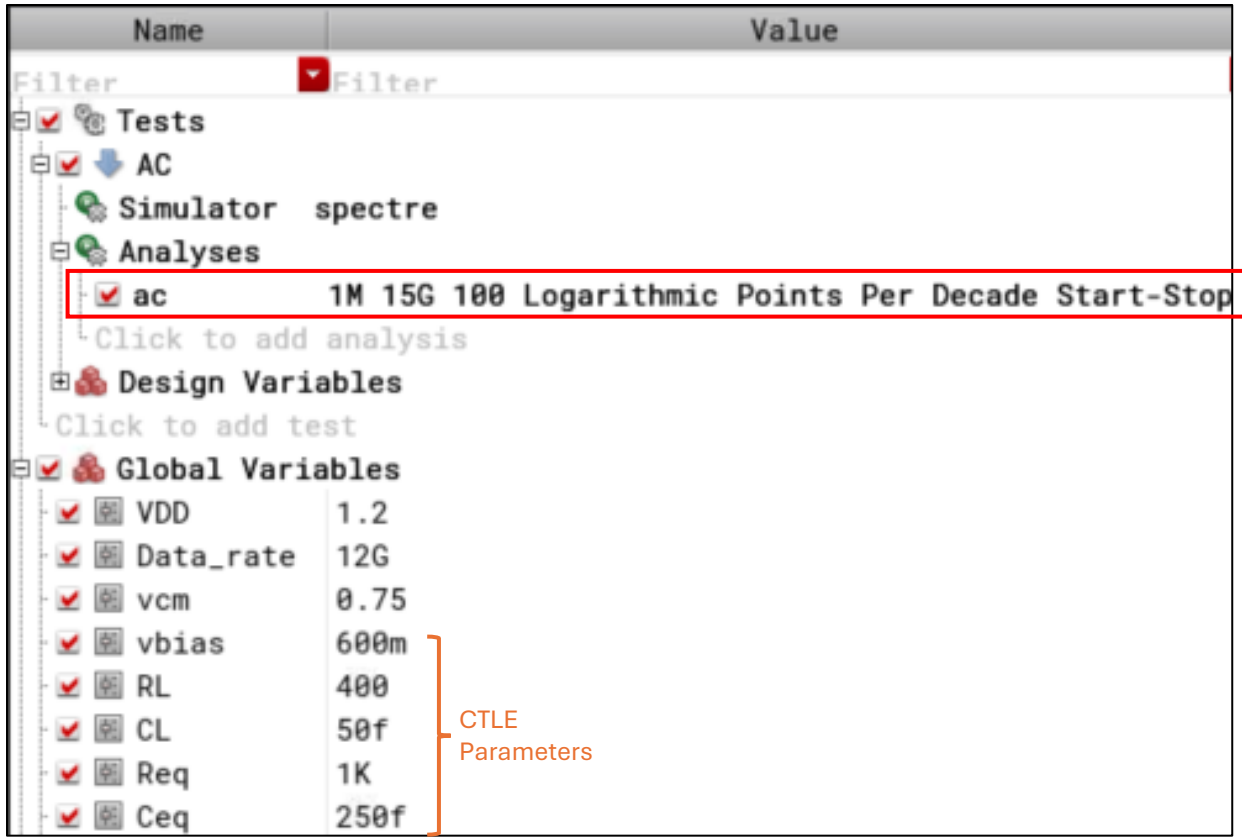
This test is to design the Gm1 stage of the DFE.

(DFE’s loop is open)

b) Frequency Response: Testbench



b) Frequency Response: Setup



b) Frequency Response: Measurements

Name	Type	Details	EvalType
Hf_gm1	expr	dB20(((VF("/outp_dfe") - VF("/outn_dfe")) / (VF("/outp_ctle") - VF("/outn_ctle"))))	point
Hf_ch	expr	dB20((VF("/inp_rx") - VF("/inn_rx")))	point
Hf_ctle	expr	dB20((VF("/outp_ctle") - VF("/outn_ctle")))	point
Hf_dfe	expr	dB20((VF("/outp_dfe") - VF("/outn_dfe")))	point
Hf_at_DC	expr	value(Hf_dfe 0)	point
Hf_at_Nyq	expr	value(Hf_dfe (VAR("Data_rate") / 2))	point

Gain of DFE Gm1 stage

Gain from inputs to Channel outputs

Gain from inputs to CTLE outputs

Gain from inputs to DFE Gm1 outputs

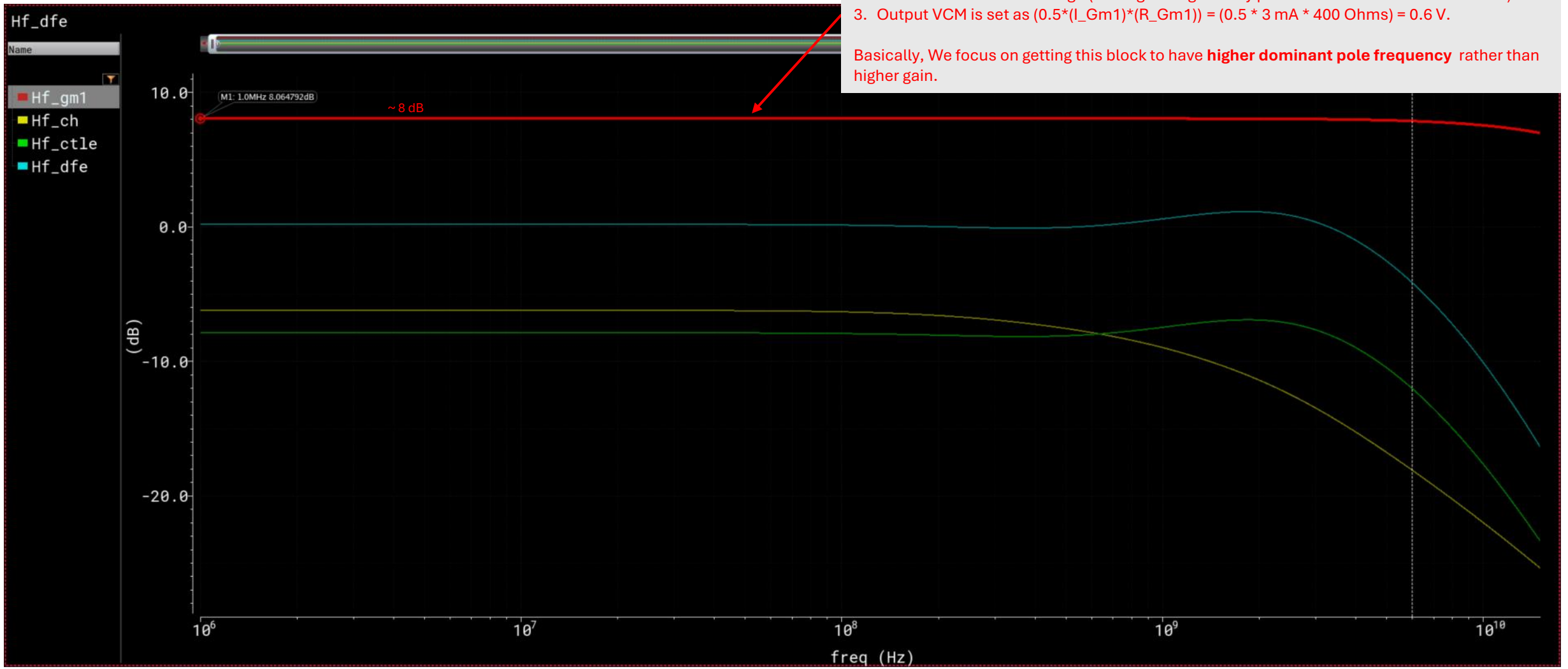
Total Gain (Loss) at DC

Total Gain (Loss) at Nyquist (6 GHz)

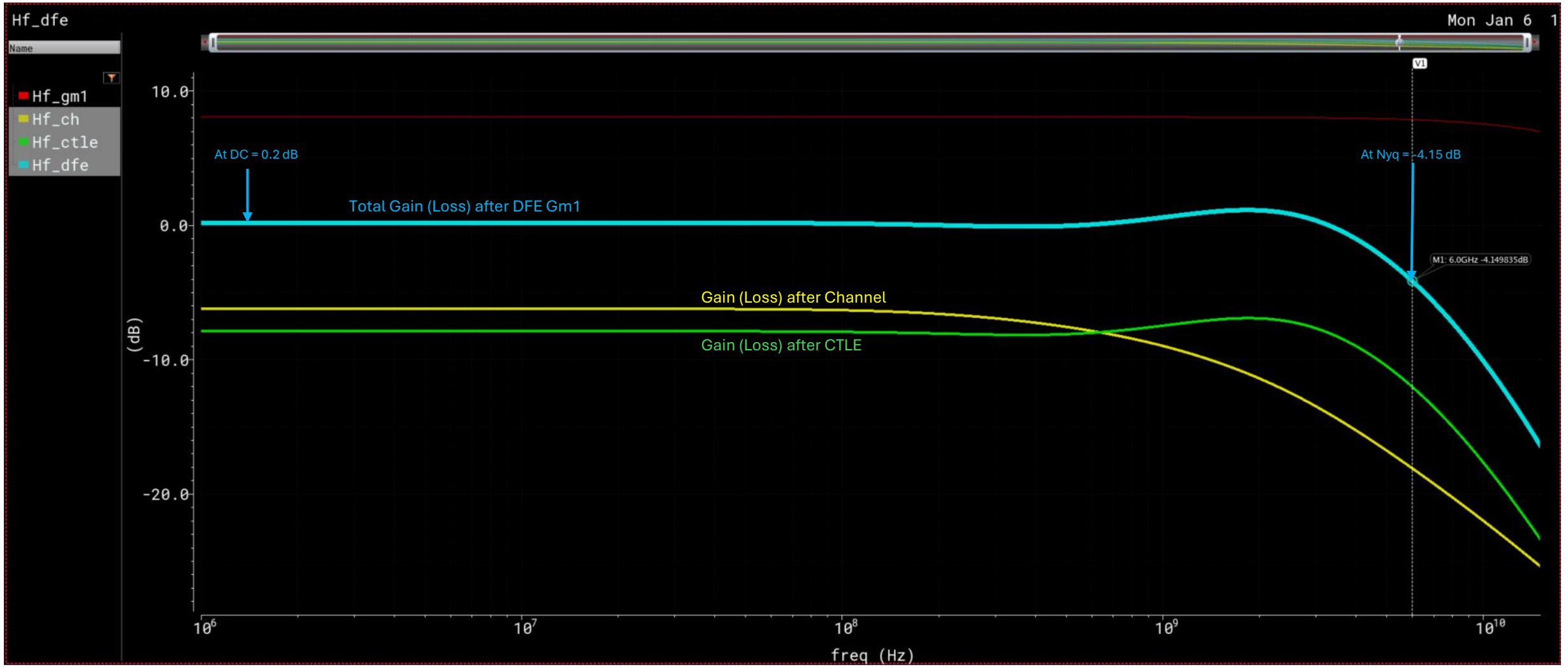
b) Frequency Response: Results

Designing the Gm1 stage:
1. Frequency response should be flat across the frequency range of interest (above Nyquist).
2. Gain doesn't need to be high (Too high of a gain may put some of the devices out of SAT).
3. Output VCM is set as (0.5*(I_Gm1)*(R_Gm1)) = (0.5 * 3 mA * 400 Ohms) = 0.6 V.

Basically, We focus on getting this block to have **higher dominant pole frequency** rather than higher gain.



b) Frequency Response: Results



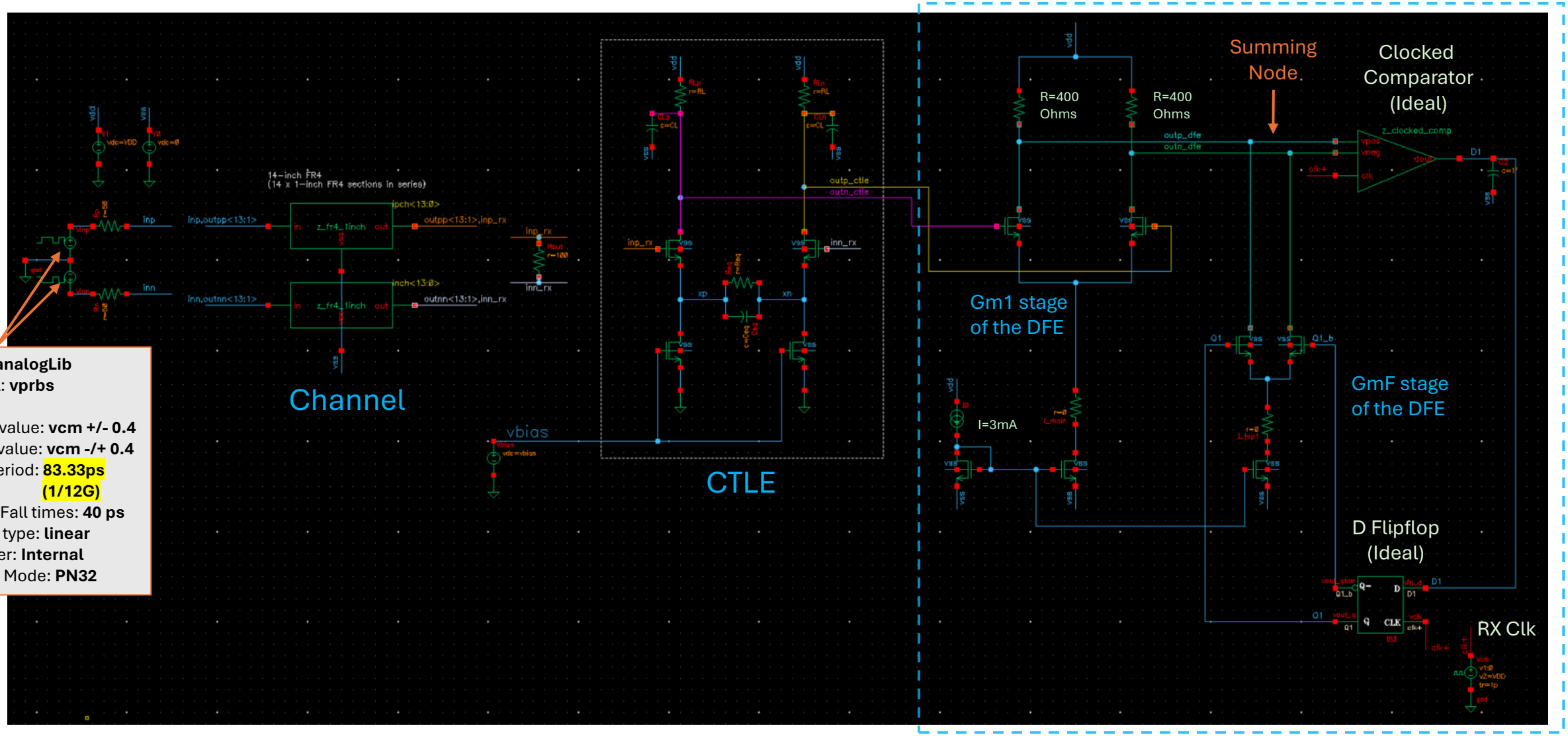
c) Eye Diagrams

This test is to check the performance with different values for DFE taps

(DFE’s loop is closed + Only using 1 tap)

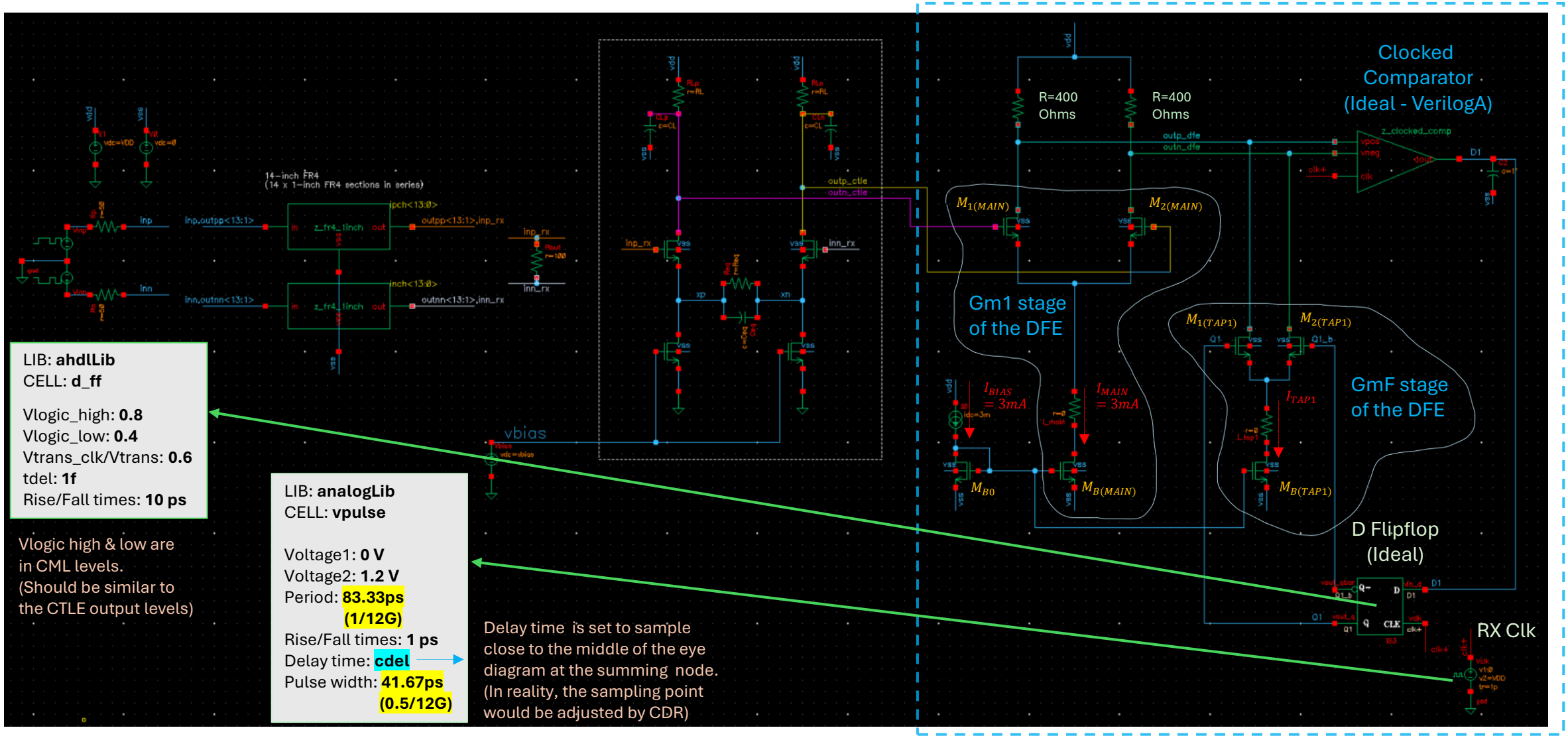
c) Eye Diagrams:

Testbench



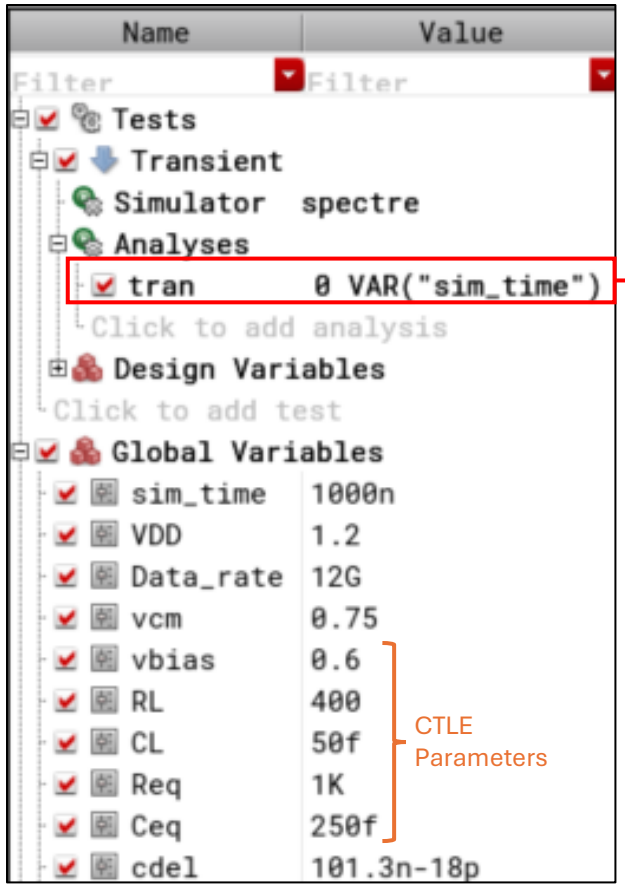
c) Eye Diagrams:

Testbench



c) Eye Diagrams:

Setup



c) Eye Diagrams:

Measurements

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
	signal	/vcm	point
	signal	/inp	point
	signal	/inn	point
	signal	/inp_rx	point
	signal	/inn_rx	point
	signal	/outp_ctle	point
	signal	/outn_ctle	point
	signal	/outp_dfe	point
	signal	/outn_dfe	point
	signal	/D1	point
	signal	/Q1	point
	signal	/Q1_b	point
	signal	/clk+	point
	signal	/clk-	point
*** PK2PK ***	expr		point
Vchin_pk2pk	expr	(VT("/inp") - VT("/inn"))	point
Vchout_pk2pk	expr	(VT("/inp_rx") - VT("/inn_rx"))	point
Vctleout_pk2pk	expr	(VT("/outp_ctle") - VT("/outn_ctle"))	point
Vdfeout_pk2pk	expr	(VT("/outp_dfe") - VT("/outn_dfe"))	point
*** EYE ***	expr		point
EYE_ch_out	expr	eyeDiagram(Vchout_pk2pk 5e-07 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
EYE_ctle_out	expr	eyeDiagram(Vctleout_pk2pk 5e-07 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
EYE_dfe_out	expr	eyeDiagram(Vdfeout_pk2pk 5e-07 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
*** Currents ***	expr		point
/I_main/MINUS_I	signal _	/I_main/MINUS	point
/I_tap1/MINUS_I	signal _	/I_tap1/MINUS	point

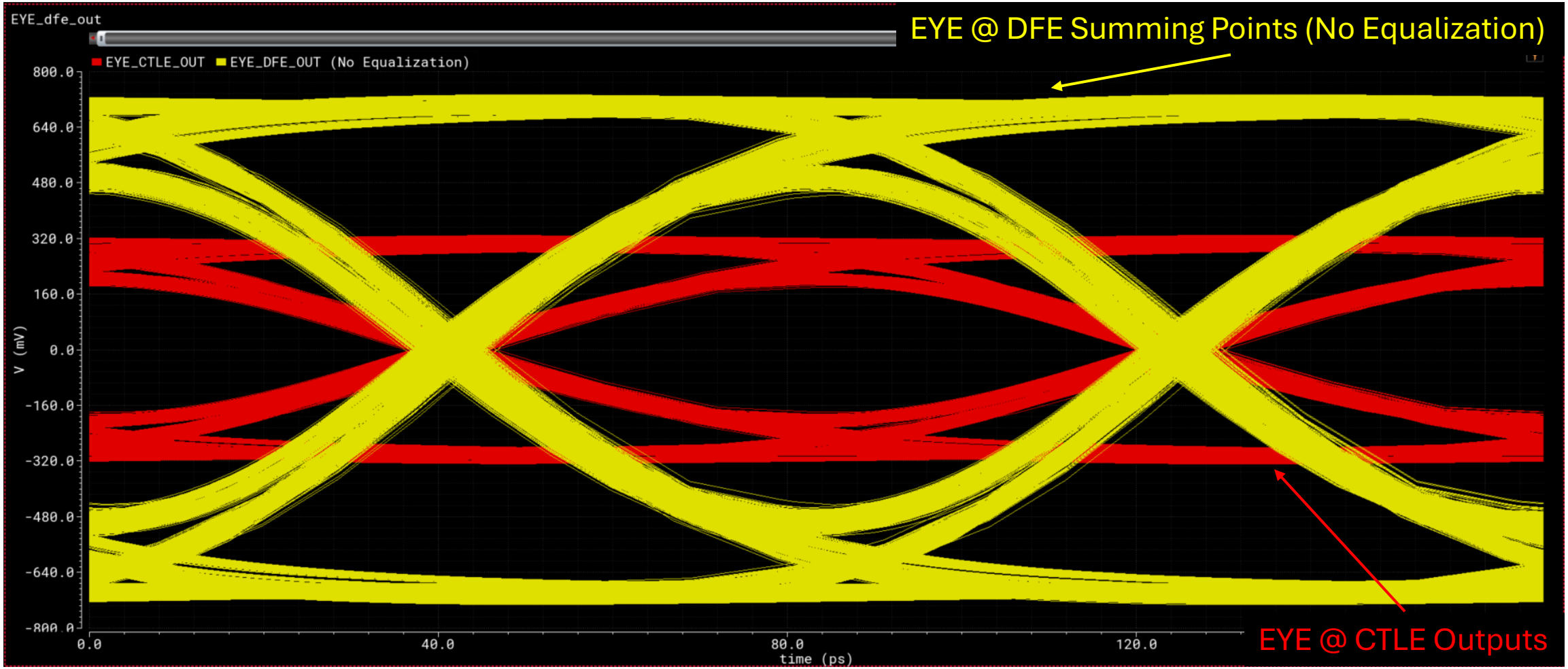
Peak-to-Peak Values

Eye Diagrams

c) Eye Diagrams:

Results (Eye Diagrams)

1) No Equalization



c) Eye Diagrams:

Results (Eye Diagrams)

$$I_{TAP1} = 5\% * I_{MAIN} = 150uA$$

$$W_{MB(TAP1)} = 5\% * W_{MB(MAIN)}$$
$$W_{M1,2(TAP1)} = 5\% * W_{M1,2(MAIN)}$$

2) DFE 1-tap Equalization: (tap1 = 5%)

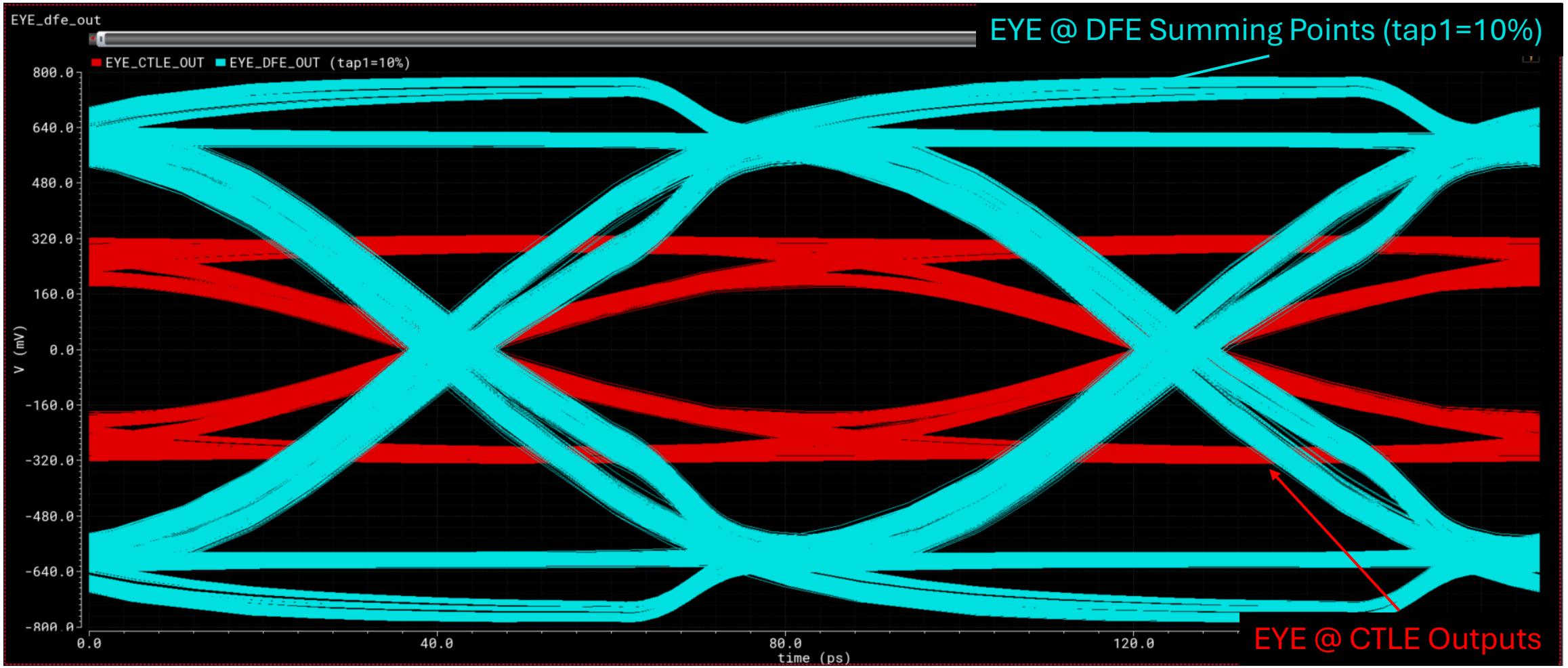
c) Eye Diagrams:

Results (Eye Diagrams)

$$I_{TAP1} = 10\% * I_{MAIN} = 300uA$$

$$W_{MB(TAP1)} = 10\% * W_{MB(MAIN)}$$
$$W_{M1,2(TAP1)} = 10\% * W_{M1,2(MAIN)}$$

3) DFE 1-tap Equalization: (tap1 = 10%)



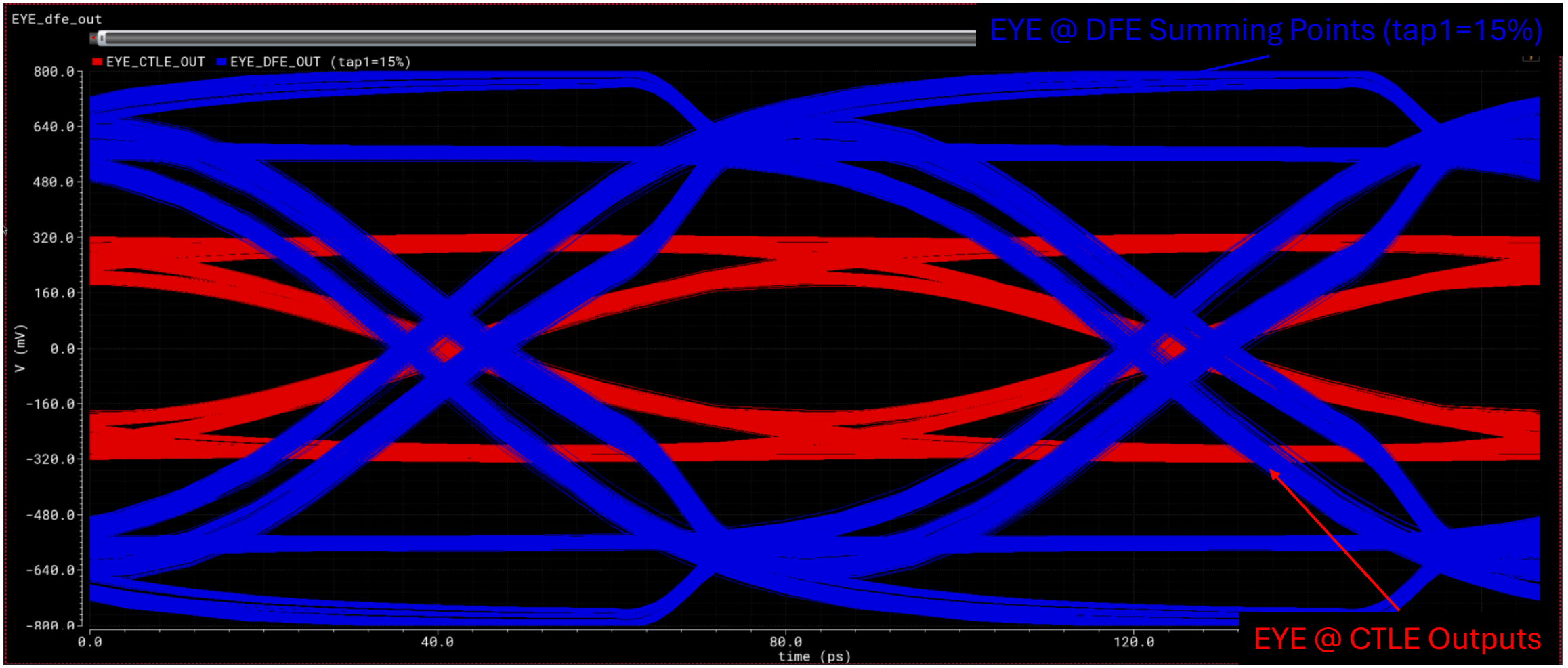
c) Eye Diagrams:

Results (Eye Diagrams)

$$I_{TAP1} = 15\% * I_{MAIN} = 450uA$$

$$W_{M_{B(TAP1)}} = 15\% * W_{M_{B(MAIN)}}$$
$$W_{M_{1,2(TAP1)}} = 15\% * W_{M_{1,2(MAIN)}}$$

4) DFE 1-tap Equalization: (tap1 = 15%)



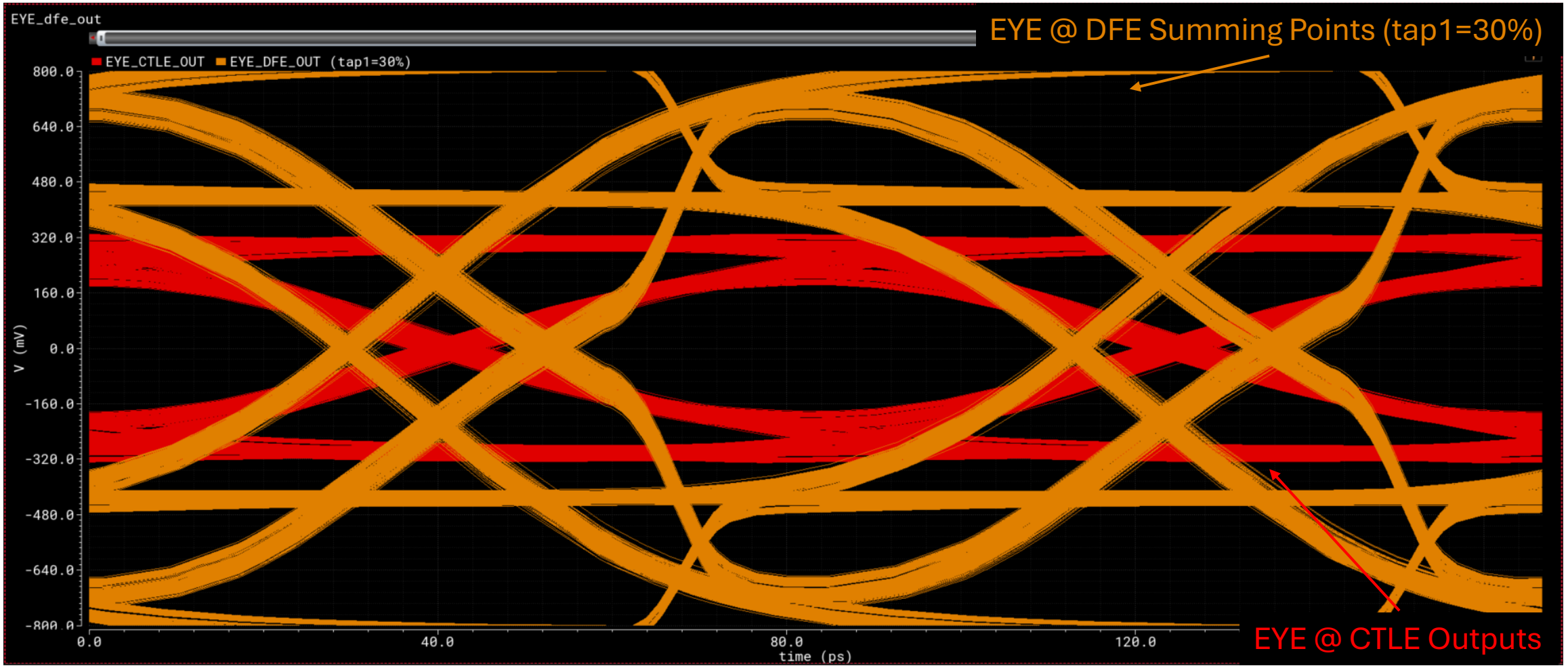
c) Eye Diagrams:

Results (Eye Diagrams)

$$I_{TAP1} = 30\% * I_{MAIN} = 900uA$$

$$W_{M_{B(TAP1)}} = 30\% * W_{M_{B(MAIN)}}$$
$$W_{M_{1,2(TAP1)}} = 30\% * W_{M_{1,2(MAIN)}}$$

5) DFE 1-tap Equalization: (tap1 = 30%)



c) Eye Diagrams:

Results (Eye Diagrams)

	DFE Out Eye Measurements				
	No Equalization	**tap1=5%**	**tap1=10%**	**tap1=15%**	**tap1=30%**
Max Eye Height	0.891 V	0.996 V	1.065 V	**1.037 V**	0.796 V
Max Eye Width	73.22 ps	**76.62 ps**	72.49 ps	67.98 ps	54.13 ps
Eye S/N	6.182 dB	7.321 dB	8.043 dB	**8.472 dB**	4.962 dB
Pk2Pk Jitter	10.58 ps	**7.20 ps**	11.39 ps	15.99 ps	29.87 ps

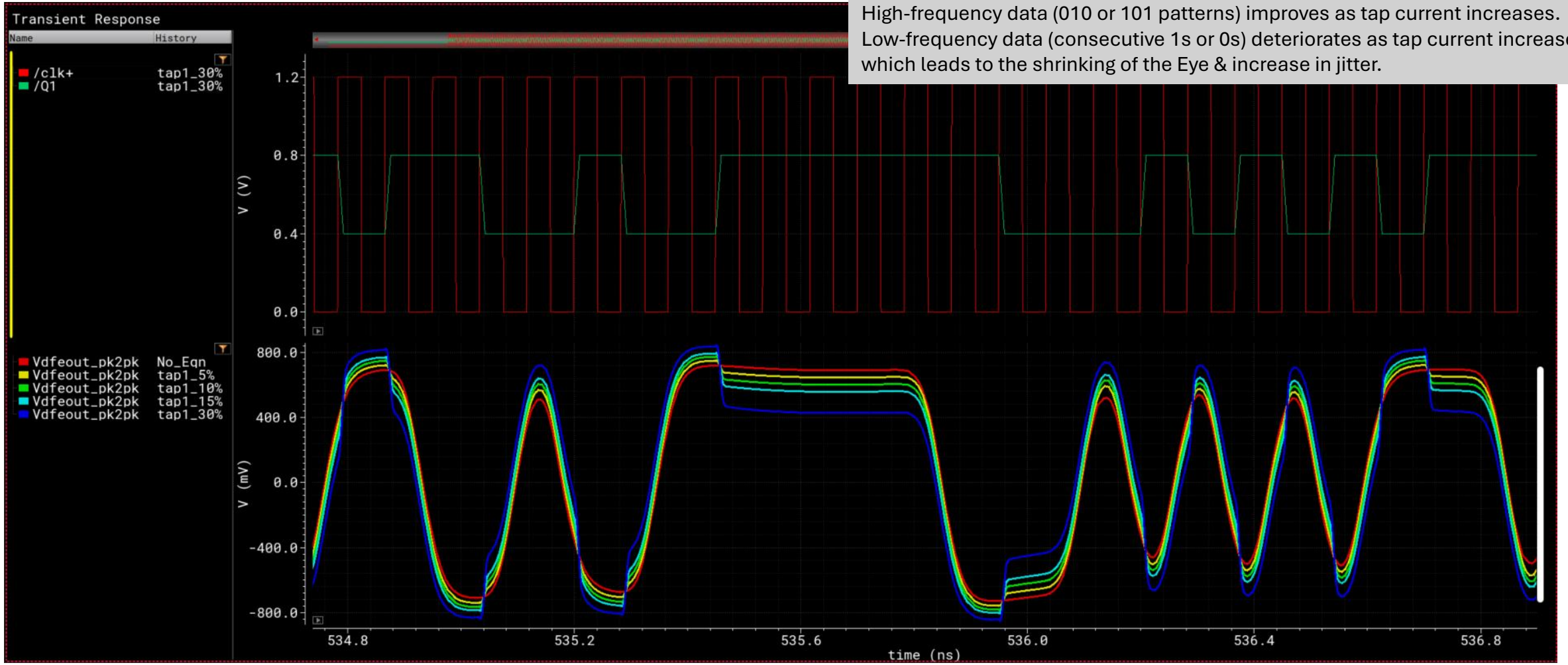
➔ All the Eye measurement parameters improve as the tap current increases from 0 (no equalization) up to a certain point, then the Eye starts to shrink & the jitter increases. That's because the DFE improves the high-frequency components of the data at the expense of the low-frequency components of the data. *

(Check Waveforms in next Slide)

[*] Y. Li and F. Yuan, "Adaptive data-transition decision feedback equalizer for serial links," *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, MA, USA, 2017, pp. 1609-161

c) Eye Diagrams:

Results (Transient Waveforms)

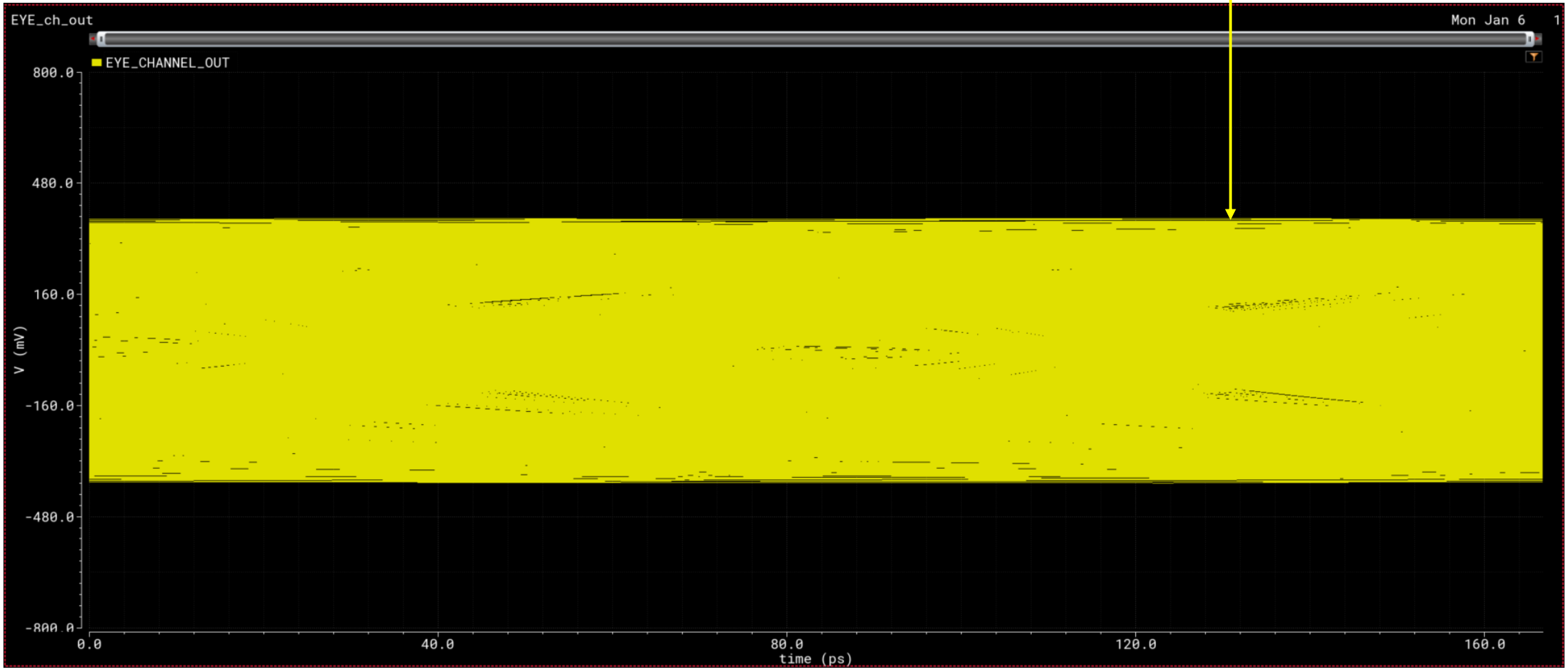


High-frequency data (010 or 101 patterns) improves as tap current increases. Low-frequency data (consecutive 1s or 0s) deteriorates as tap current increases, which leads to the shrinking of the Eye & increase in jitter.

Final Results & Remarks

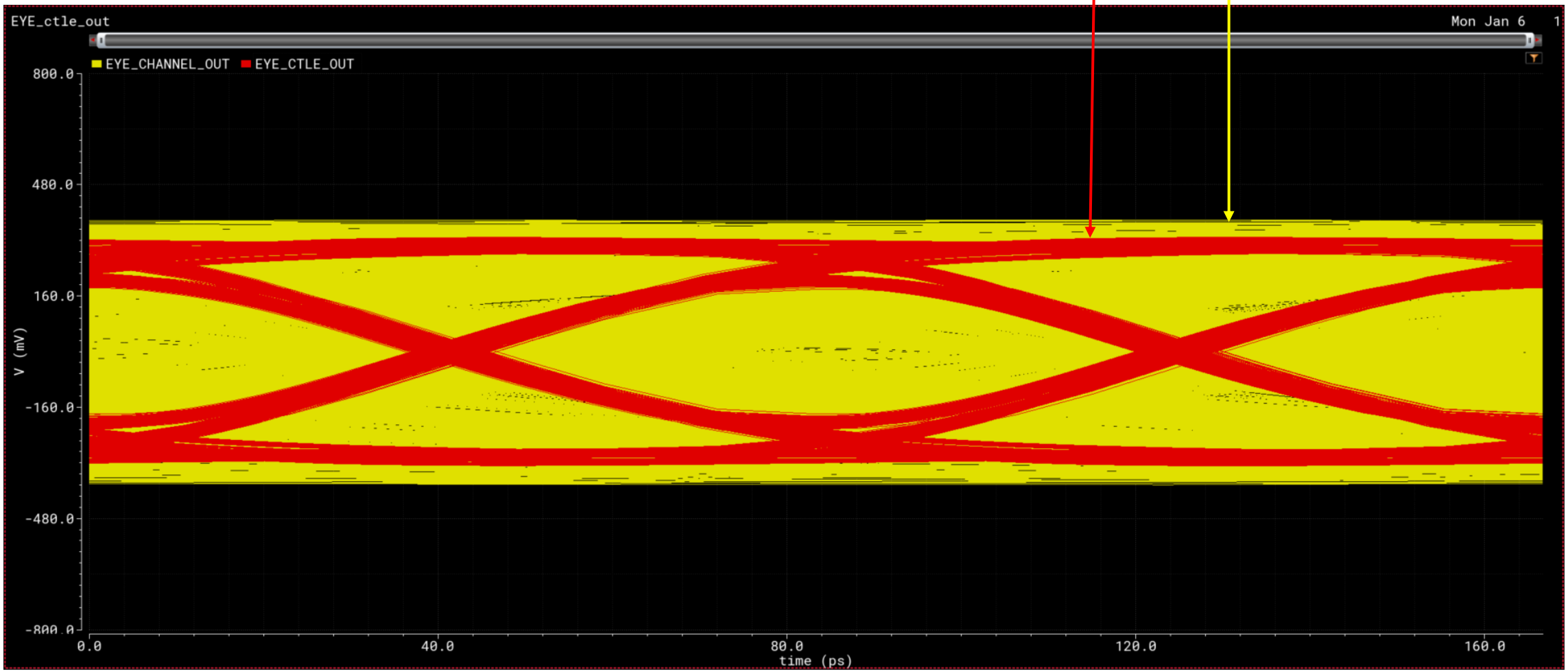
Final Results

➔ Eye Diagram @ Channel Outputs



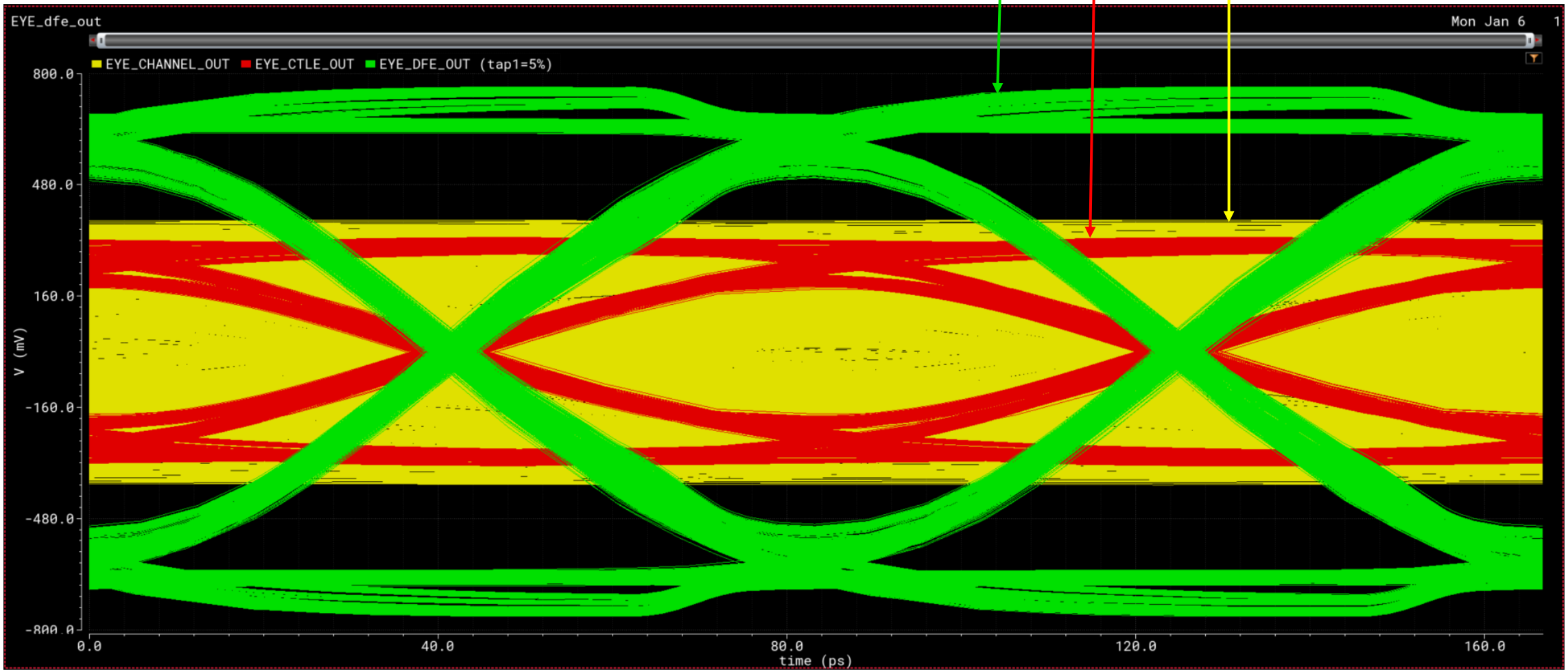
Final Results

➔ Eye Diagram @ CTLE Outputs



Final Results

➔ Eye Diagram @ DFE Outputs



Final Results

➔ Eye Diagram Measurements:

	Eye Measurements	
	After CTLE	**After DFE**
Max Eye Height	359 mV	996 mV
Max Eye Width	73.23 ps	76.62 ps
Eye SNR	5.63 dB	7.32 dB
Pk2Pk Jitter	10.26 ps	7.20 ps

Final Remarks

- The system may not need to use DFE (or higher-tap DFE) if CTLE can give an enough eye opening.

- Future Work:
  1. **Current-steering** fliflops should be carefully designed for the feedback path of the DFE. (Current-Steering FF lab)
  2. **Data-State DFE** can be used to improve high-freq data without affecting low-freq data. (Paper)
  3. **Loop unrolling** technique can be used to improve timing margins at higher speeds. (Lec Note)