Tx Driver - CML

1 Gbps

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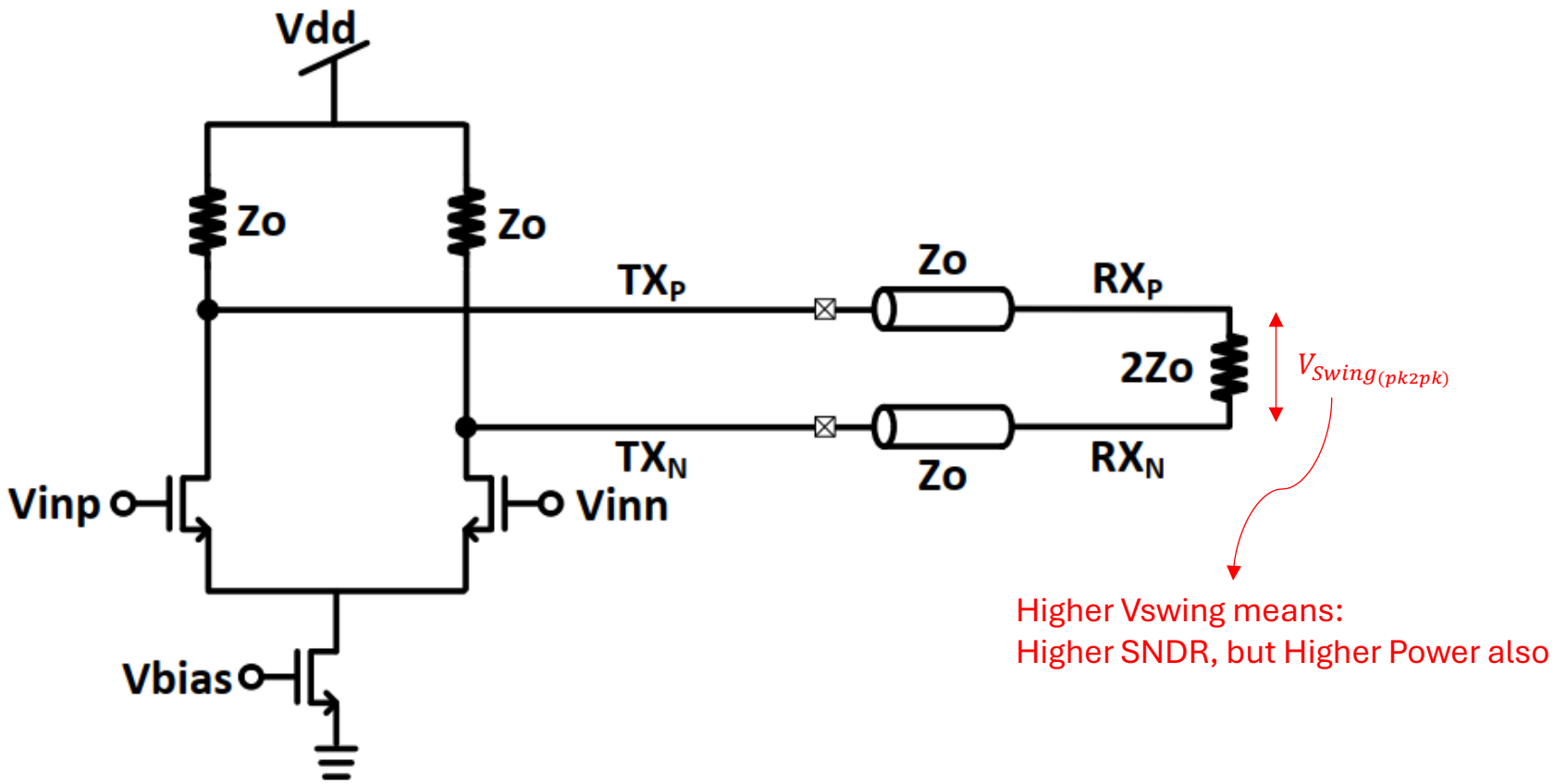
Current-Mode Logic (CML)

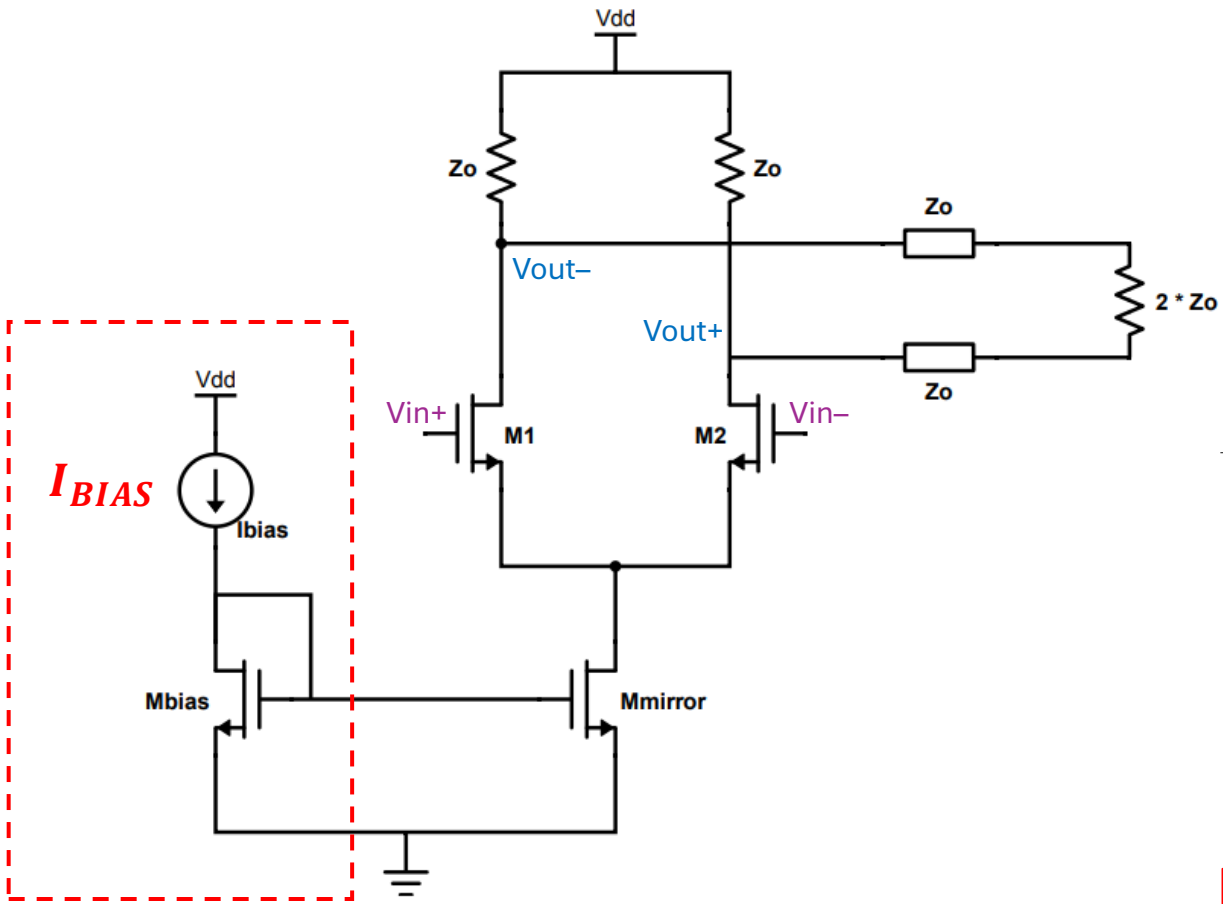


- Current Steering
- Both sides are terminated by 50Ω
- Basic structure in high-performance serial link

1) Without Replica

$$V_{Swing_{(pk2pk)}} = V_{out+} - V_{out-}$$

$$V_{Swing_{(pk2pk)}} = I_{BIAS} * Z_O$$



$$For\ V_{Swing_{(pk2pk)}} = 500\ mV:$$

$$I_{BIAS} = \frac{500\ mV}{50\ \Omega} = \mathbf{10\ mA}$$

Device Sizing:

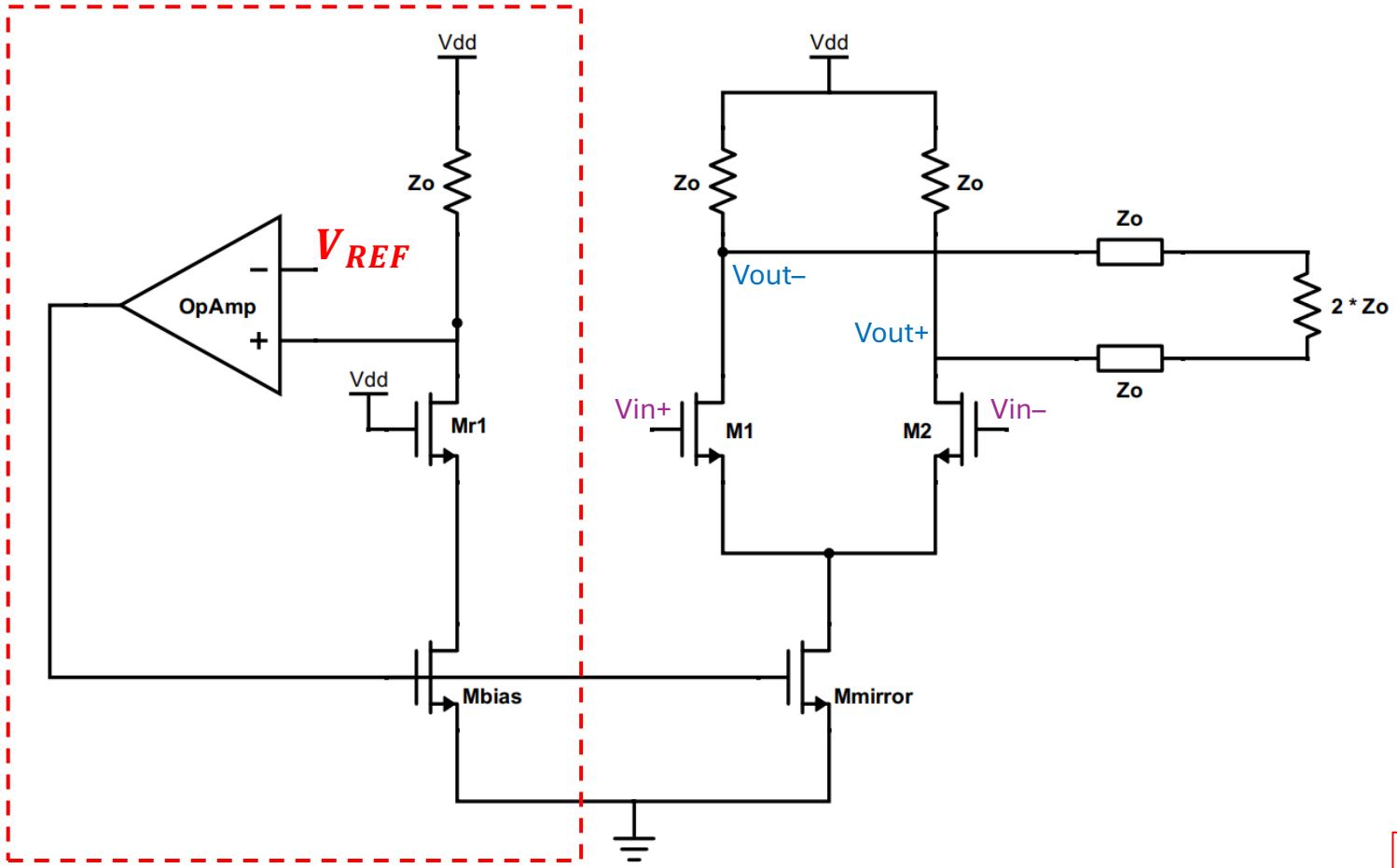
- Input devices (M1 & M2) act as switches, so we should increase W (reducing R_{ON}) to improve headroom.
- Bias devices (Mbias & Mmirror) should have large L to reduce channel length modulation. Also we need to increase their W to reduce their V_{GS} & V_{OV}.

M1 = M2 :	$L = L_{MIN}$,	m=100x
Mbias = Mmirror :	$L = 4 * L_{MIN}$,	m=200x

2) With Replica

$$V_{Ref} = V_{DD} - I_{BIAS} * Z_O$$

$$V_{Swing_{(pk2pk)}} = V_{DD} - V_{REF}$$



$For\ V_{Swing_{(pk2pk)}} = 500\ mV$:

$V_{REF} = 1V - 250\ mV$
$= \mathbf{750mV}$

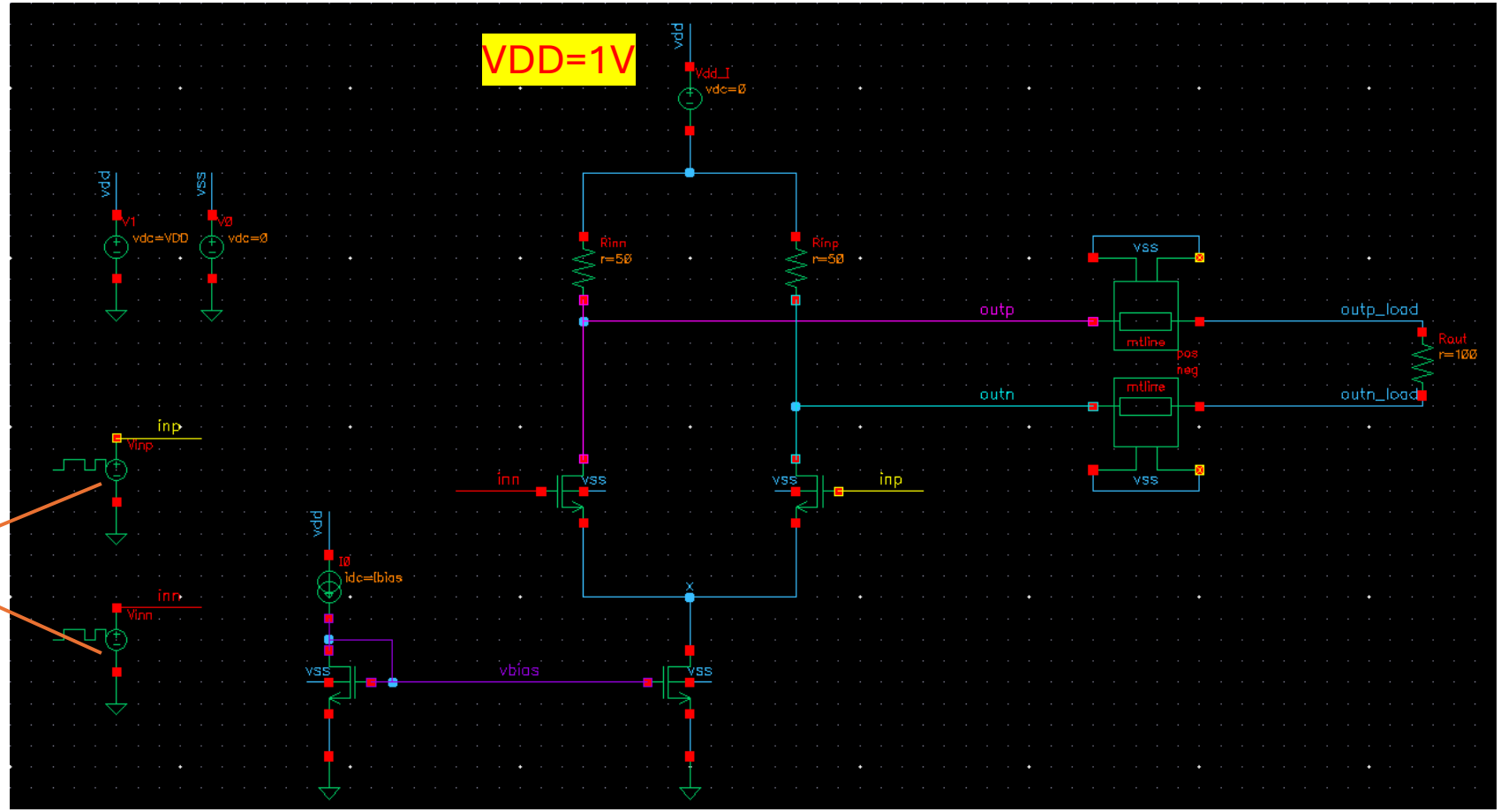
M1 = M2 = Mr1 : L = L_{MIN} , m=100x
Mbias = Mmirror : L = 4 * L_{MIN} , m=200x

Testbenchs & Setups

- VDD = 1V
- Data-Rate = 1 Gb/s
- VSWING = 0.5V (pk2pk)
- IBIAS = 10mA

Testbench

A) Without Replica

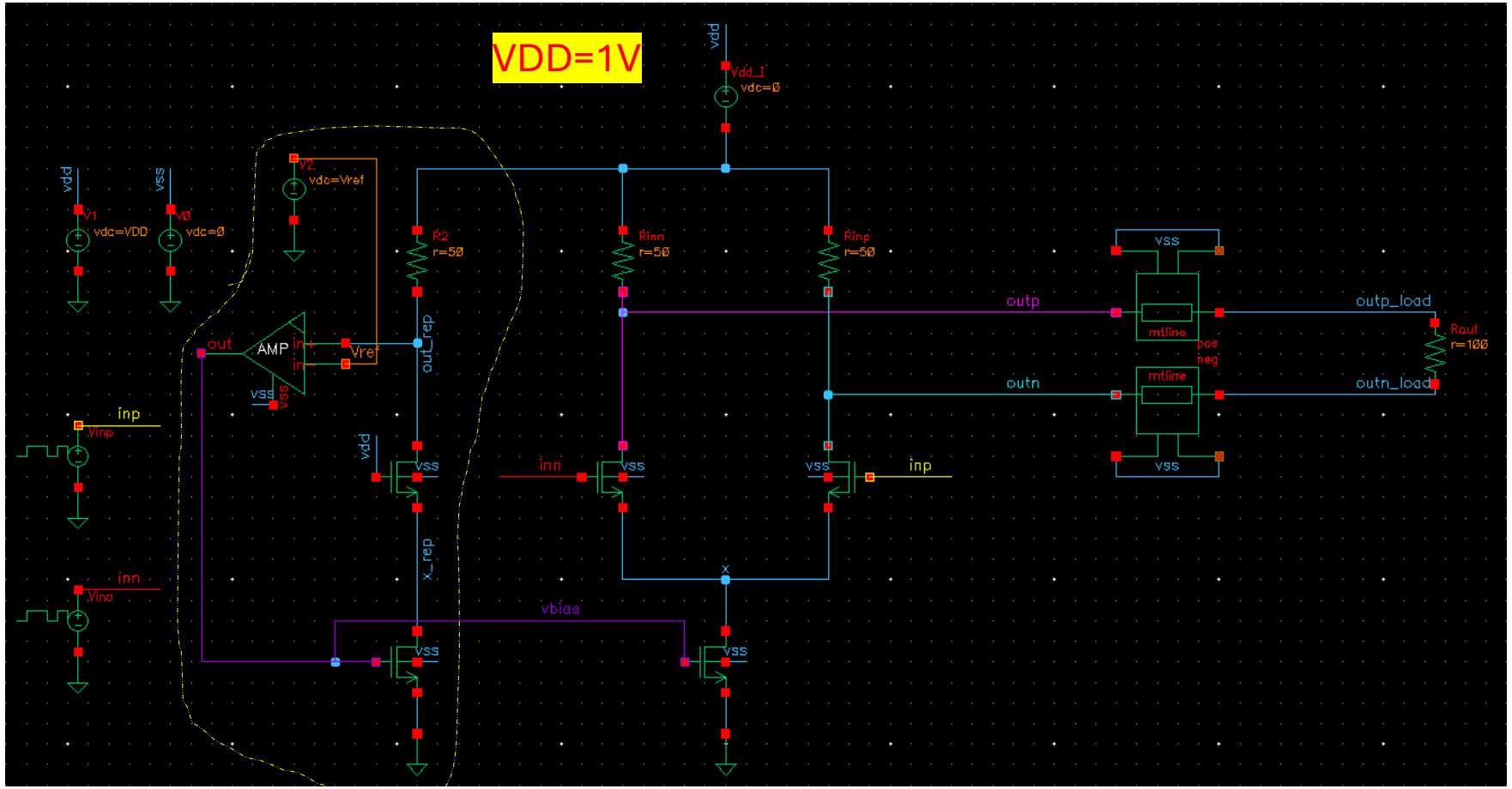


LIB: **analogLib**
CELL: **vprbs**

Zero value: **0 V** / 1 V
One value: **1 V** / 0 V
Bit period: **1 ns**
Rise/Fall times: **20 ps**
Edge type: **linear**
Trigger: **Internal**
LFSR Mode: **PN32**

Testbench

B) With Replica

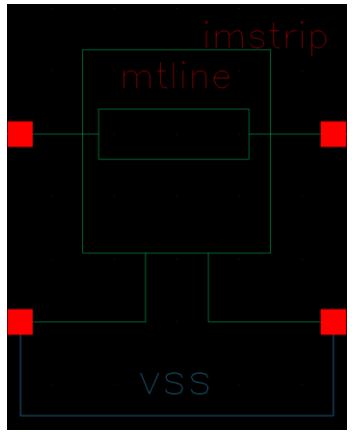


Channel Settings (mtline)

➔ For Zo = 50 Ohms:

$$Z_0 \approx \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98\,H}{0.8\,W + T}\right)$$

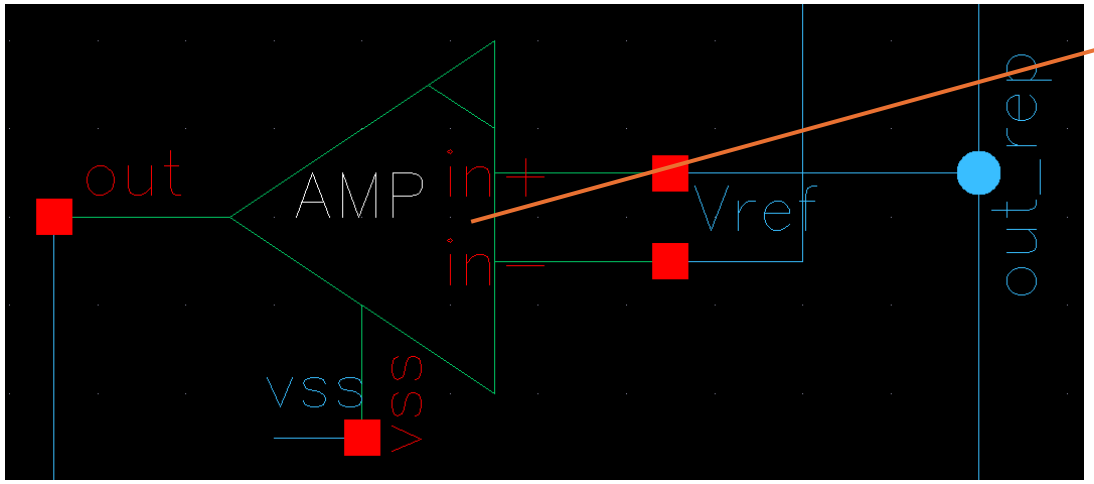
Dielectric_const = ε_r = 4.8
Dielectric_thickness = H = 360u
Line_width = W = 625u
Line_thickness = T = 17.78u

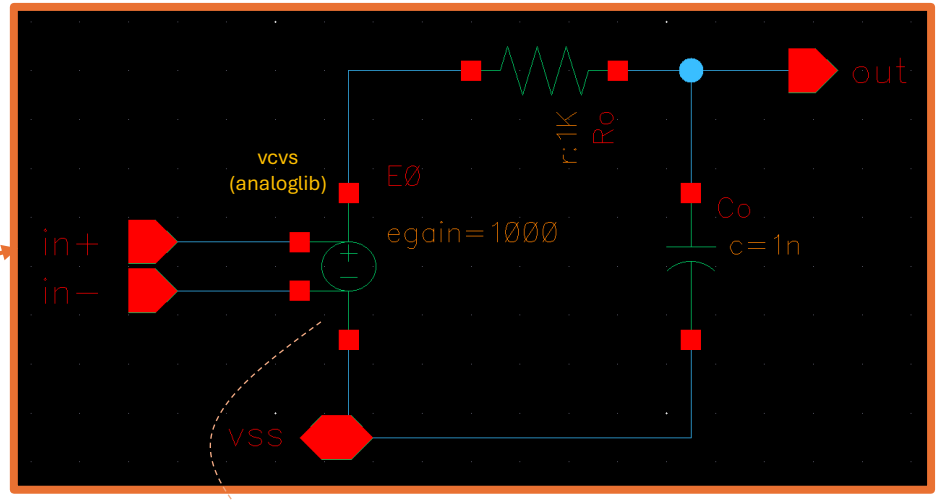


Library Name	analogLib
Cell Name	mtline

CDF Parameter	Value
Num of lines (excluding ref	1
Model name	
Physical length	100m M
Multiplicity factor	1
Max signal frequency	
Type of Input	FieldSolver
Generate noise?	no
Transmission line type	microstrip
Model type	wideband
Rel dielectic const of laye	4.8
Dielectric layer thickness	360u
Signal line width	625u
Signal line thickness	17.78u
Signal line spacing	

Ideal OpAmp

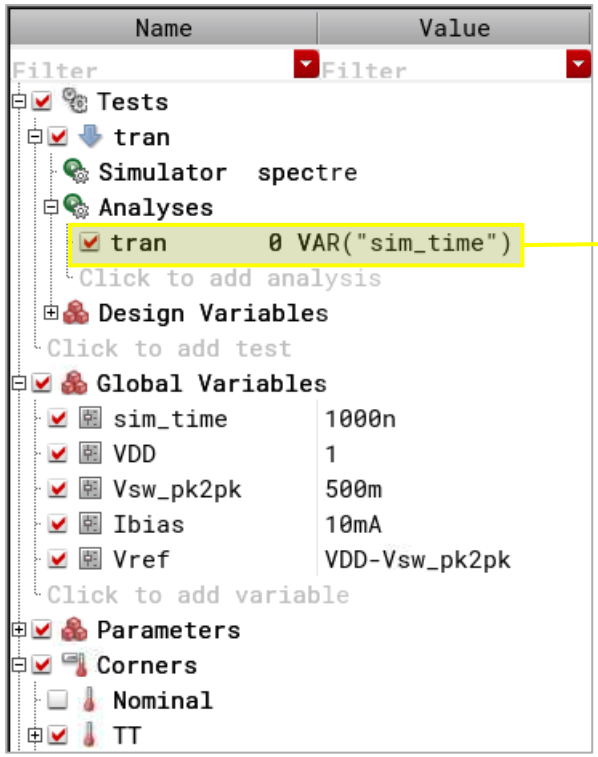


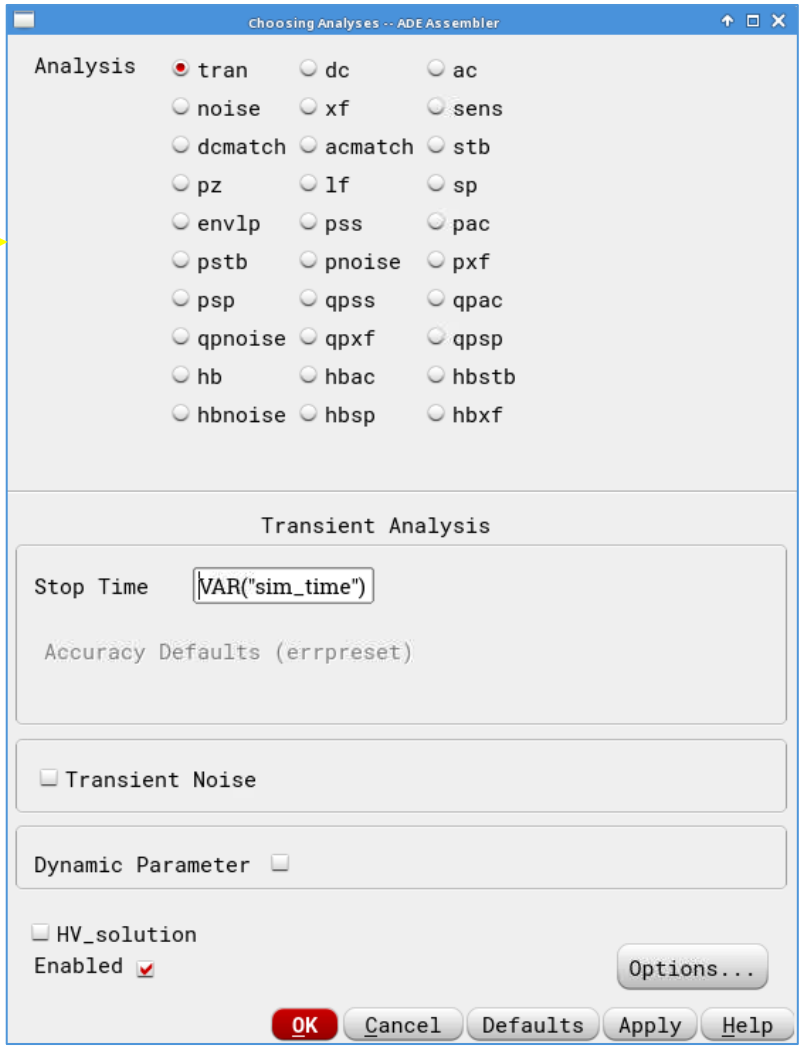


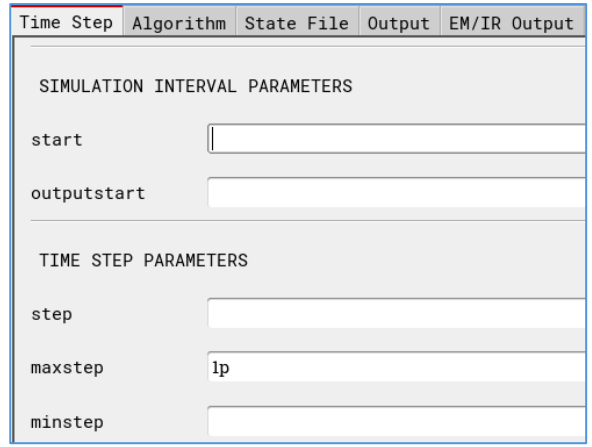
Library Name	analogLib
Cell Name	vcvs

CDF Parameter	Value
Type of transfer char	Linear / PWL
Smoothing Factor	
Voltage gain	1000
Multiplier	
Maximum Output Voltage	1
Minimum Output Voltage	0

Simulation Setup

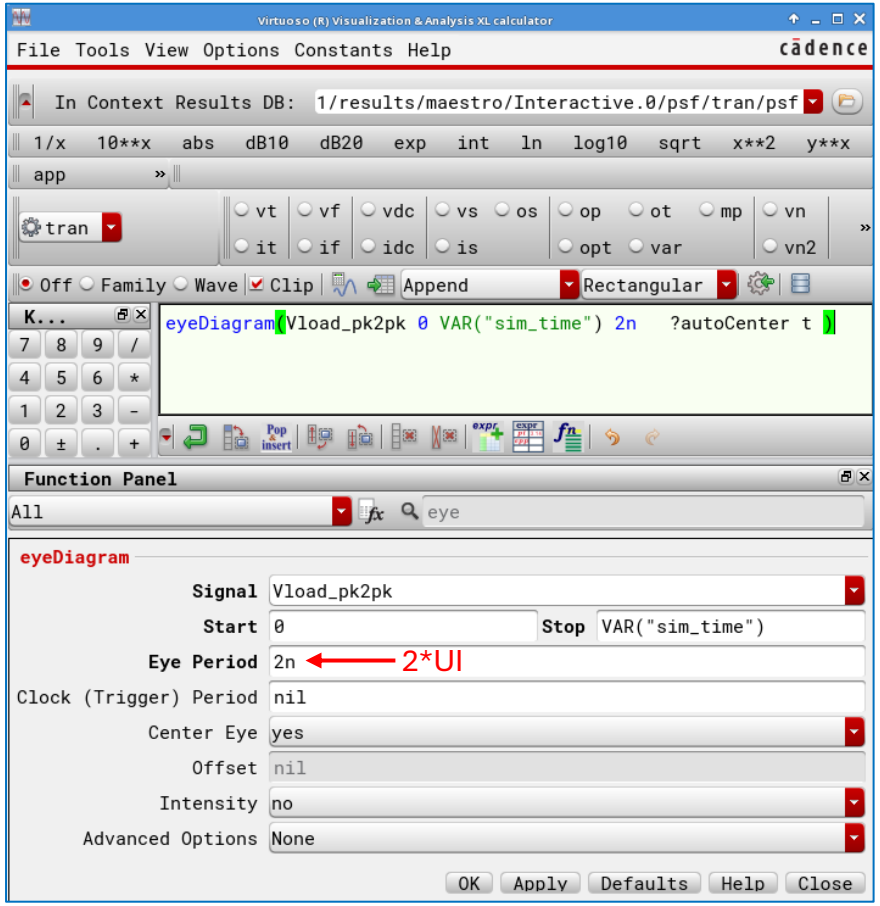






Measurements

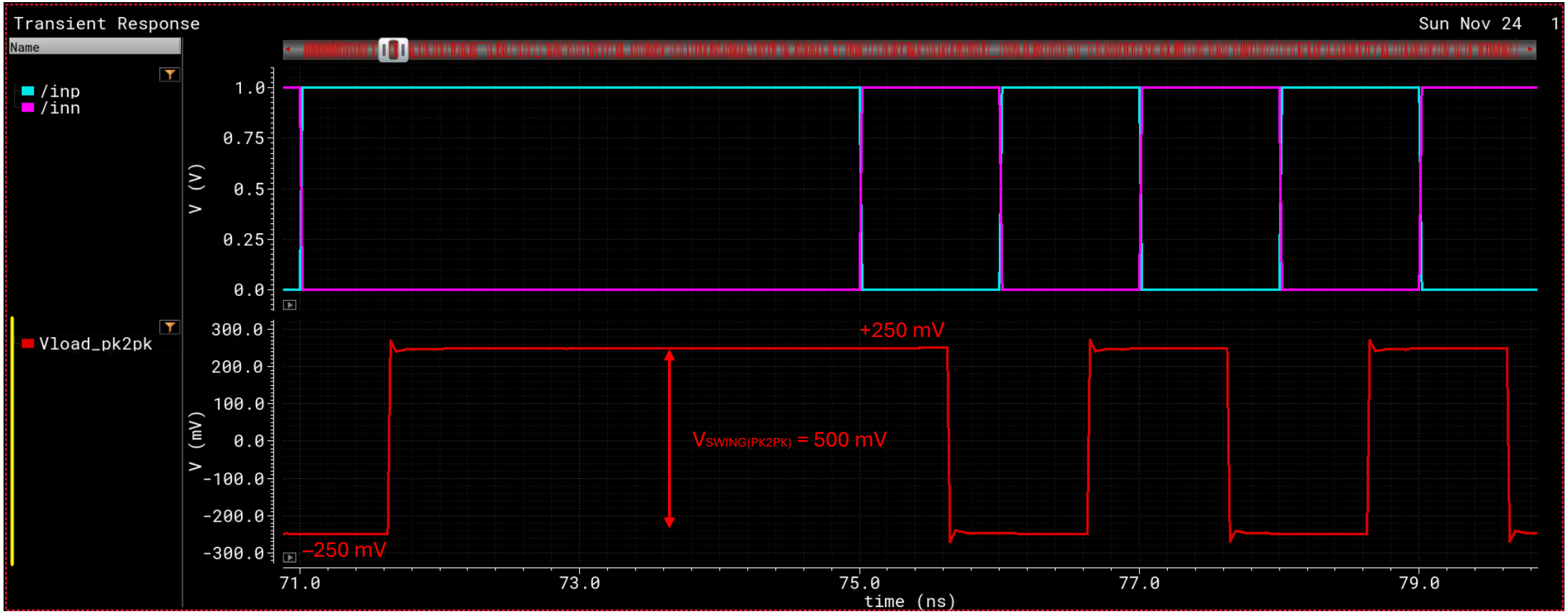
Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
*** Voltages ***	expr		point
	signal	/inp	point
	signal	/inn	point
	signal	/outp	point
	signal	/outn	point
	signal	/outp_load	point
	signal	/outn_load	point
	signal	/x	point
	signal	/vbias	point
	signal	/Vref	point
	signal	/out_rep	point
	signal	/x_rep	point
*** Currents ***	expr		point
/Vdd_I/PLUS_I	signal …	/Vdd_I/PLUS	point
/Rout/PLUS_I	signal …	/Rout/PLUS	point
*** Outputs ***	expr		point
Vtxout_pk2pk	expr	(VT("/outp") - VT("/outn"))	point
Vtxout_eye	expr	eyeDiagram(Vtxout_pk2pk 0 VAR("sim_time") 2e-09 ?autoCenter t)	point
Vload_pk2pk	expr	(VT("/outp_load") - VT("/outn_load"))	point
Vload_eye	expr	eyeDiagram(Vload_pk2pk 0 VAR("sim_time") 2e-09 ?autoCenter t)	point



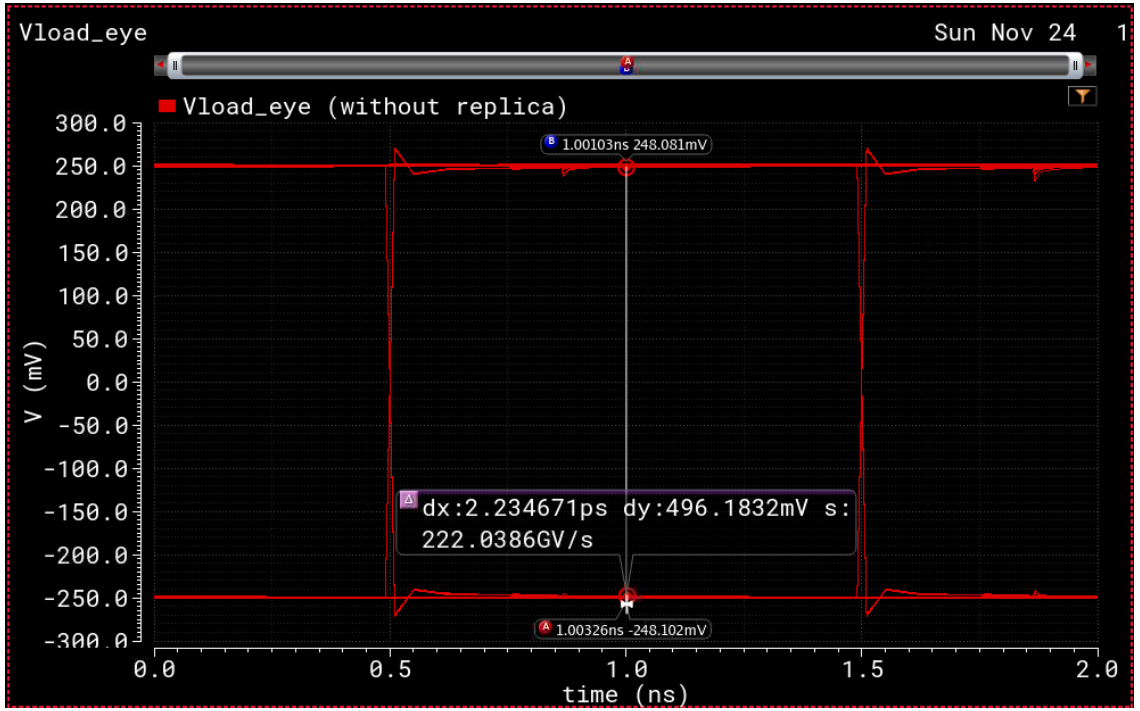
eyeDiagram(VT("/outp_load")-VT("/outn_load") 0 VAR(“sim_time") 2n ?autoCenter t)

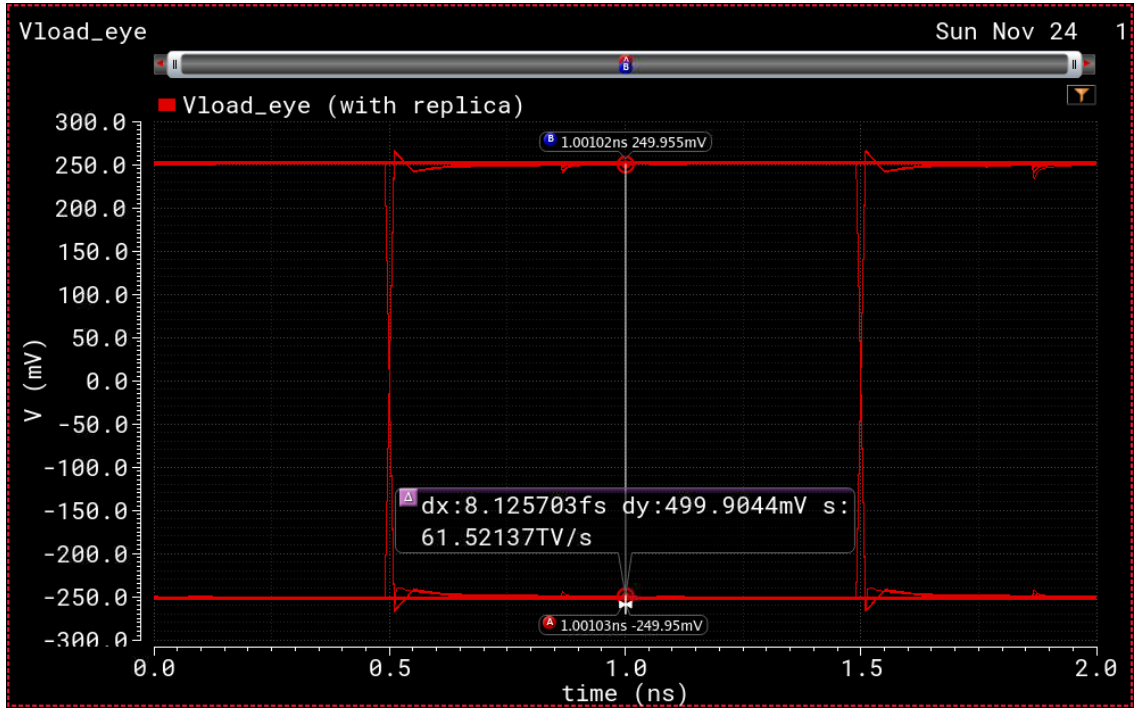
Simulations & Results

Waveforms


Transient Response
Sun Nov 24
1
Name
/inp
/inn
Vload_pk2pk
V (V)
1.0
0.75
0.5
0.25
0.0
V (mV)
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
+250 mV
VSWING(PK2PK) = 500 mV
−250 mV
71.0
73.0
75.0
77.0
79.0
time (ns)

Waveforms (Eye-Diagrams)





No Replica:

$V_{SW(pk2pk)}$ = 496.18 mV

With Replica:

$V_{SW(pk2pk)}$ = 499.9 mV

➔ More Accurate Swing, at the expense of an extra branch + additional power drawn by the OpAmp

(For more info on how to measure Eye Diagrams)

Current Consumption

- Total current drawn = 20 mA

  (10 mA from main driver + 10 mA from current branch/Replica)